PACIFIC: The readout ASIC for the SciFi Tracker of the LHCb detector

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Physikalisches Institut, Heidelberg Universitat
SciFi collaboration

Scintillator Fibre Tracker (SciFi) collaboration, several institutes on different aspects:

- Fibre procurement and Quality Assurance (QA).
- Mat construction.
- Modules construction.
- Sensors R&D and procurement (QA).
- Electronics.
- Mechanics and services.
LHCb detector upgrade during 2019-2020:

- Factor 5 higher luminosity
- Triggerless 40MHz readout.

Upgraded Tracking system:

- Vertex detector:
  - Si strips → pixels
- Upstream Tracker:
  - new larger coverage Si strips
- Inner (Si) and Outer (Straws):
  - Scintillating Fibre Tracker
SciFi Overview

- **Scintillating Fibre Tracker:**
  - Light detector, $< 1\% X_0/\text{layer}$
  - Large area, total of $6 \times 5 \text{m}^2$
  - XUVX planes on each station
  - Full detector is 3 stations
  - Total radiation up to 35kGy

- **Requirements:**
  - Hit efficiency $\approx 99\%$
  - High granularity $250 \mu\text{m}$
  - Hit resolution $< 100 \mu\text{m}$
Fibres type

- Polystyrene core
- Double cladding

CERN-LHCb-PUB-2015-011:
- Emission peak 460nm
- Attenuation length 3.5m
- Radiation degrades transmission:
  - 35kGy → 40% reduction in full length
Mat assembly

Custom winding machine:

Threaded wheel to align:

Mat alignment:
Module assembly

- 8 fibre mats assembled into a module.
- Support panel with $200\mu m$ carbon fibre and 20mm Nomex core.
- Alignment precision of $50\mu m$ in 5m!
SciFi Module

– Total of **128 modules of** $0.5 \times 5m^2$.
– Each module consists on eight fibre mats.
– Each fibre mat is $240 \times 13cm^2$.
– Mats with 6 layers of fibres:

– Fibres readout by SiPM array:

– $64 + 64$ channels array (2 dies).
– $60 \times 60\mu m^2$ cells, 104 pixels / channel.

Signal spread, 16-20 phe. Clustering needed:
Fibres signal generation and transmission

- Signal shape and time of arrival depends on interaction point:

  ![Signal shape and transmission diagram]

  - Mirror effect
  - Monte Carlo simulation as function of interaction point
ReadOut Box (ROB) formed by:

- SiPM array on Flex cable.
- PACIFIC(x4) carrier board.
- FPGA(x2) cluster board.
- Master board:
  - Power regulation (DC/DC)
  - Data concentrator FPGA
  - Data links GBT (x8 links)

- Half ROB:
  8xSiPM Flex +
  4xPACIFIC Carrier +
  4xClustering +
  1xMaster Board
PACIFIC design

Low Power ASIC for the SCIentillating FIBre TrACker readout.
Design collaboration between different institutes and countries:

- Universitat de Barcelona (Barcelona, Spain)
- Instituto de Fisica Corpuscular (Valencia, Spain)
- Physikalisches Institut (Heidelberg, Germany)
- Laboratoire de Physique de Clermont (Clermont Ferrand, France)
PACIFIC: Initial goals

Initial specifications of ASIC:

- 128 channels readout.
- Sensor bias adjustable channel by channel.
- Low input impedance.
- No components needed between sensors and ASIC.
- Shaper to fit both manufacturers timing.
- Double peak resolution of 25ns (no dead time).
- 6 bit ADC per channel.
- Clustering on ASIC.
- 1W maximum power.
PACIFIC: Realistic/corrected goals

✗ 64 channels readout.
✓ Sensor bias adjustable channel by channel.
✓ Low input impedance.
✓ No components needed between sensors and ASIC.
✓ Shaper to fit both manufacturers timing (two different shapers).
✓ Double peak resolution of 25ns (no dead time) (double gated integrator).
✗ 6 bit ADC per channel ($6 \times 128 \times 40 \text{MHz} = 30 \text{Gbps/ASIC}$), changed to 3 non-linear Flash ADC.
✗ Clustering on ASIC (algorithm not clear, not enough time).
✗ 0.5W maximum power.
✗ 15ns of ”correct” integration for different time of arrival with 10% of maximum spill-over.
PACIFIC: Analog Channel processing

Preamplifier, Shaper, Integrator, Track and Hold and Digitization
PACIFIC: Other stuff on chip

- Common biasing:
  - Voltage references
  - Current references
  - DACs
  - Monitoring ADC
  - Power on Reset
  - SLVS Receivers / Drivers

- Digital blocks:
  - Encoding and serialization of data:
    (4 channels, 320 MHz clock).
  - Slow control (I2C).
  - Hamming encoding:
    Digital mitigation of SEUs in configuration registers.
PACIFICr5 floorplan

- 16 channels groups
- 32 channels left/right
- I2C in central area
- Central left for common bias
- Central right for ADC/debug
- Main power rails from top to bottom
- Differential outputs at top and bottom
<table>
<thead>
<tr>
<th>Year</th>
<th>IBM 130nm</th>
<th>TSMC 130nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>2013</td>
<td>PACIFICr0</td>
<td>PACIFICr5</td>
</tr>
<tr>
<td>PACIFICr1</td>
<td>PACIFICr2 / 2b</td>
<td>PACIFICr3</td>
</tr>
<tr>
<td>Preamp from AMS 0.35</td>
<td>8 channels</td>
<td>64 channels</td>
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<tr>
<td>Three analog channels</td>
<td>Common bias I2C</td>
<td>Common bias I2C</td>
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<tr>
<td>Different test structures</td>
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<td>I2C, ADC, local DACs 8b Single ended output</td>
</tr>
<tr>
<td>First I2C</td>
<td>2x Common bias I2C</td>
<td>64 channels</td>
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<tr>
<td></td>
<td></td>
<td>Common bias I2C, ADC, local DACs 8b Differential out LVDS</td>
</tr>
</tbody>
</table>

To improve:
- Uniformity
- Integration/shaping
- Track and Hold slew rate
- Add local thresholds
- Uniformity / trimming
- Baseline holder
- Track and Hold
- Comparators range
- Spillover

– PACIFICr5pq production submitted in January 2018.

Albert Comerma (comerma@physi.uni-heidelberg.de)
Highly usage of top Al routing for power distribution.
PACIFICr5 test board

- Same digital FPGA based motherboard with USB connection.
- New Analog test board with removable cover.
PACIFICr5pq - VREF DAC

- PACIFIC production "soft start".
- Changed slope and offset to have smaller initial VREF.

**PACIFICr5**

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**PACIFICr5pq**

- PACIFIC production "soft start".
- Changed slope and offset to have smaller initial VREF.
PACIFICr5 - Local Threshold DACs

- Improved power distribution, even better uniformity.
PACIFICr5pq - Vanode control

- Step reduced to 40 mV range adjusted to usable range (120mV-720mV).
PACIFICr5 - Trimming

PACIFICr5 threshold scan for comparator 1 x 1

PACIFICr5 channels dispersion

C₀ BX₀

C₀ BX₁

C₁ BX₀

C₁ BX₁

C₂ BX₀

C₂ BX₁

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**PACIFICr5pq - Light s-curve**

**PACIFICr5p**

PACIFICr5 threshold scan for comparator 0 bx 0

**PACIFICr5q**

PACIFICr5 threshold scan for comparator 0 bx 0

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PACIFICr5 - Package

- Received 1482 PACIFICr5p/q.
- QR marking readable in socket.
- Several devices tested with socket.
- Devices on Carrier Boards.
## Test-beam @ CERN

**July 3\(^{rd}\) - 18\(^{th}\) @ CERN SPS H8**

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</thead>
</table>

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TWEPP 2018 – PACIFIC: SciFi Tracker readout ASIC at LHCb
Test-beam @ CERN

- First time with full system.
- Two half modules with full readout.
- Final DAQ (miniDAQ2).
- Raw and clustered data taking modes.
Test-beam @ CERN

- Efficiency taking telescope as reference with default configuration.
- Thresholds set at 1.5/2.5/4.5 phe.

February | online clustering | 1.5, 2.5, 4.5 | 0 mm

from Simon Nieswand
PACIFIC architecture validated

Low Power ASIC for the SCIntillator FIbres traCker

Channel processing chain:

- High bandwidth current input.
- Anode voltage control.
- Fast Shaper for tail adjustment.
- Double interleaved gated integrator.
- Track and hold.
- Digitization with 3 hysteresis comparators.
- Serialization and slow control.

- Successfully achieved desired performance in test-beam.
- Mass production test and assembly, \( \approx 23k \) devices.

Albert Comerma (comerma@physi.uni-heidelberg.de)
Thanks for your attention!
Backup slides
Silicon Photo Multipliers

- Peak PDE = 48% (3.5 V)
- Cross-talk = 3%
- Delayed cross-talk = 2.5%
- Afterpulses < 0.1%

DCR halved every -10°C
SCiFi (528k channels) - 4096 GBT links (max. 2.3 TB/s)
PACIFIC: Preamplifier

Functions:
- High Bandwidth
- Low input impedance
- Low Power
- Adjustable Gain
- Control on input DC
PACIFIC: Preamplifier output

- Trans-impedance amplifier for voltage output and BW limitation
PACIFIC: Shaper

Double adjustable pole-zero configuration:

- Reduce tail of signal (Pole).
- Remove undershoot (Zero).
- Baseline holder afterwards.
PACIFIC: Gated integrators

- Classical integrator.
- Double gated to avoid dead time.
- Passive Track and Hold at the output.
PACIFICr5q: Track and Hold optimization

- PACIFICr5q uses different T&H
- Bottom plate disconnect
- New control signals generated
- Standard cells block
- Slightly delayed switches ON/OFF
PACIFIC: Digitization

- Classical Hysteresis comparator (PMOS).
- Two sets of thresholds;
  - Common
  - Local
### PACIFICr5x-wb0Y - POR values

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<tr>
<th>DUT</th>
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<th>VREF</th>
<th>$V_{refDCFB}$</th>
<th>$VOTA_{fast}$</th>
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*After internal DACs correction*
SiPM connected to PACIFIC:

- Analog DEBUG outputs for Preamp, Shaper and TH.
- Synchronous light triggered on front of array.
- Threshold scan of one comparator to measure photons.

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PACIFICr5q - Spillover

- Spillover dependency on PACIFIC configuration.
- Testbeam data after clustering.

**Primary bXing**

![Graph showing efficiency vs channel for August and February settings.

**Tail bXing**

![Graph showing efficiency vs channel for August and February settings.]}
- Internal ADC calibration using external DAC/ADC.

V_{ADC} = -8.79e-04 \times \text{VALUE} + 1.25e-01
PACIFICr5 - Temperature sensor

- Used one point for temperature sensor calibration (±5% error expected).