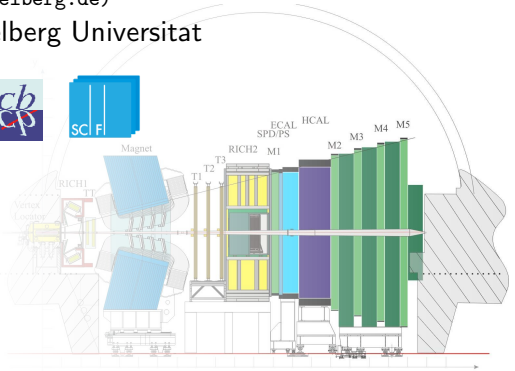
PACIFIC: The readout ASIC for the SciFi Tracker of the LHCb detector

Albert Comerma on behalf of the SciFi Collaboration

(comerma@physi.uni-heidelberg.de)

Physikalisches Institut, Heidelberg Universitat

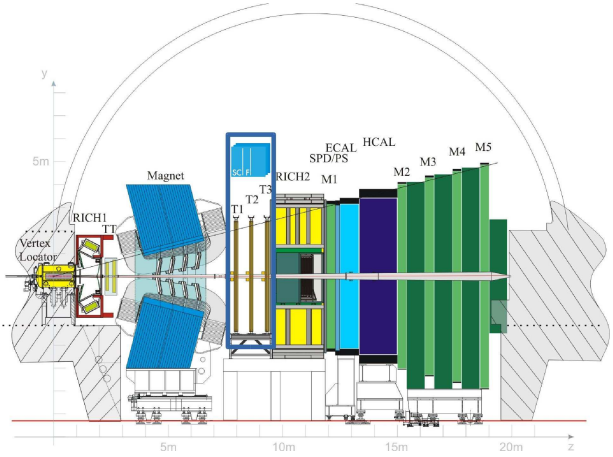


SciFi collaboration

Scintillator Fibre Tracker (SciFi) collaboration, several institutes on different aspects:

- Fibre procurement and Quality Assurance (QA).
- Mat construction.
- Modules construction.
- Sensors R&D and procurement (QA).
- Electronics.
- Mechanics and services.

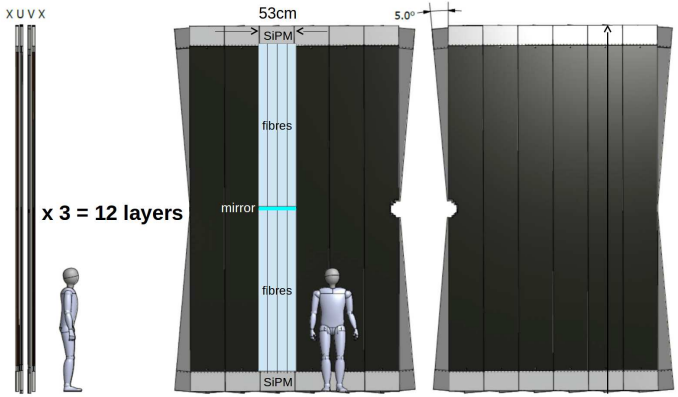
LHCb Tracker upgrade



- LHCb detector upgrade during 2019-2020:
  - Factor 5 higher luminosity
  - Triggerless 40MHz readout.
- Upgraded Tracking system:
  - Vertex detector:
    - → Si strips → pixels
  - Upstream Tracker:
    - → new larger coverage Si strips
  - Inner (Si) and Outer (Straws):
    - → **Scintillating Fibre Tracker**

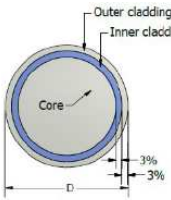
SciFi Overview

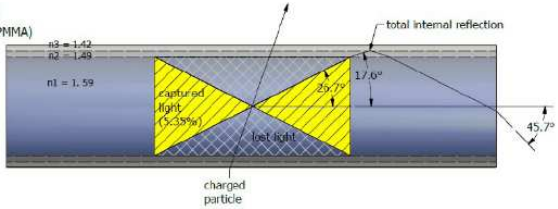
- Scintillating Fibre Tracker:
  - Light detector, $< 1\% X_0/layer$
  - Large area, total of $6 \times 5m^2$
  - XUVX planes on each station
  - Full detector is 3 stations
  - Total radiation up to 35kGy
- Requirements:
  - Hit efficiency $\approx 99\%$
  - High granularity $250\mu m$
  - Hit resolution $< 100\mu m$

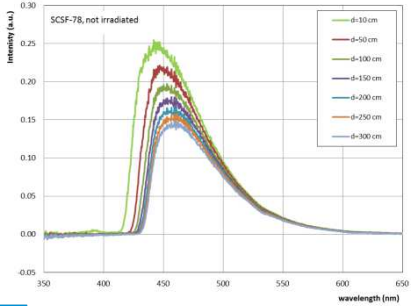


Fibres type

- Polystyrene core
- Double cladding





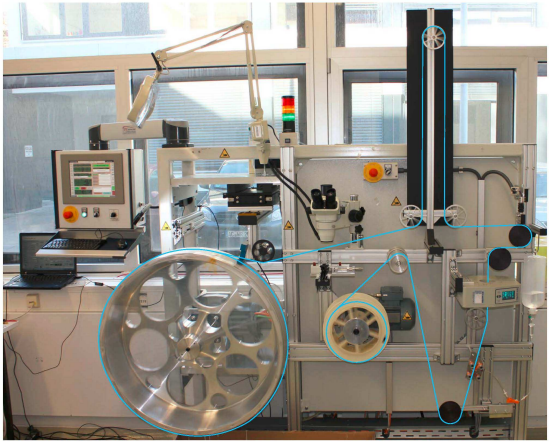


CERN-LHCb-PUB-2015-011:

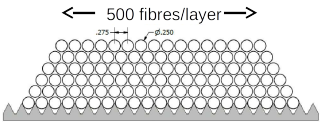
- Emission peak 460nm
- Attenuation length 3.5m
- Radiation degrades transmission:
  - 35kGy→40% reduction in full length

Mat assembly

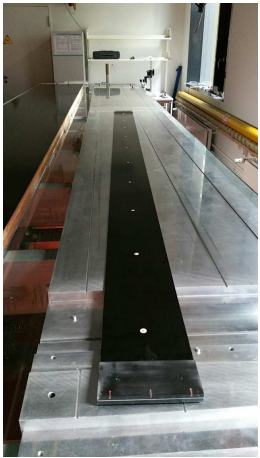
Custom winding machine:



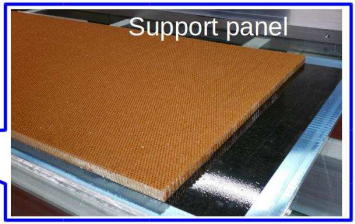
Threaded wheel to align:



Mat alignment:



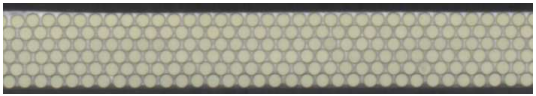
Module assembly



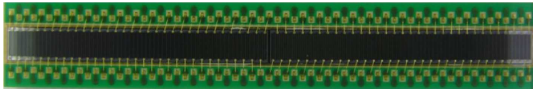
- 8 fibre mats assembled into a module.
- Support panel with $200\mu m$ carbon fibre and 20mm Nomex core.
- Alignment precision of $50\mu m$ in 5m!

SciFi Module

–Total of **128 modules of** $0.5 \times 5m^2$.
–Each module consists on eight fibre mats.
–Each fibre mat is $240 \times 13cm^2$.
–Mats with 6 layers of fibres:

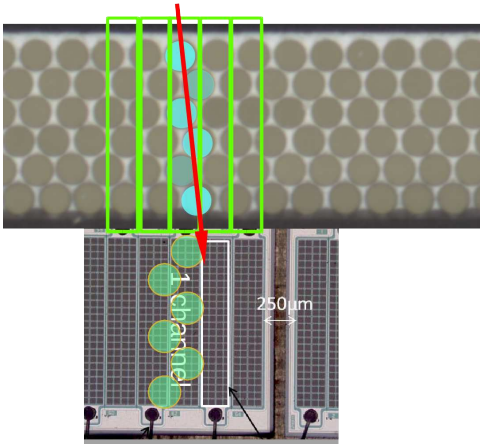


–Fibres readout by SiPM array:



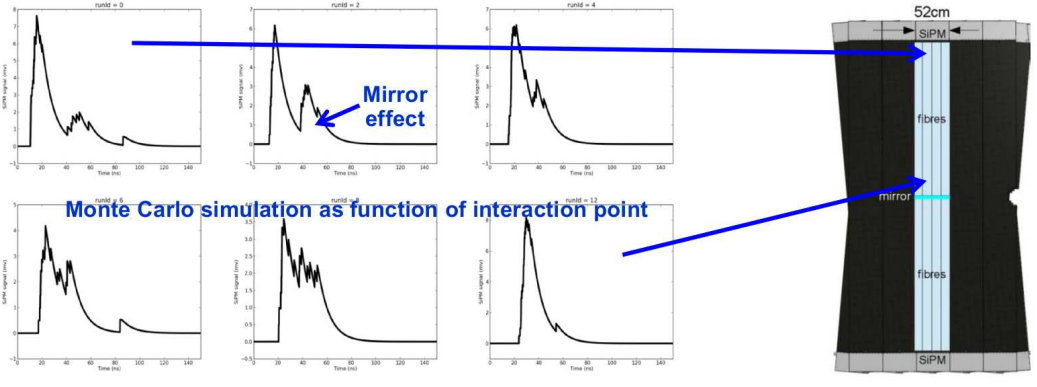
–64 + 64 channels array (2 dies).
–$60 \times 60\mu m^2$ cells, 104 pixels / channel.

Signal spread, 16-20 phe.
Clustering needed:



Fibres signal generation and transmission

- Signal shape and time of arrival depends on interaction point:



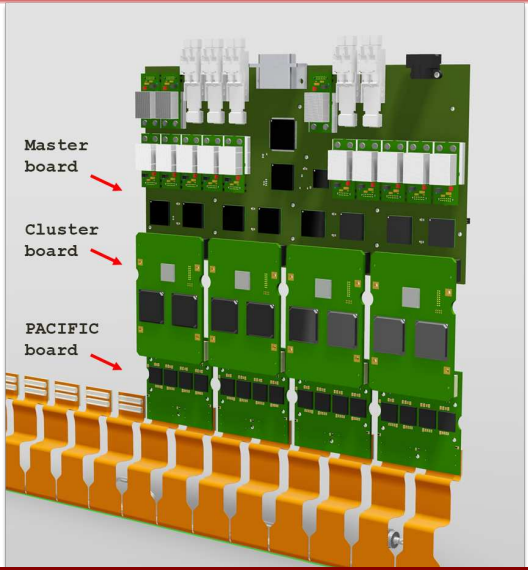
ReadOut Box

ReadOut Box (ROB) formed by:

- SiPM array on Flex cable.
- PACIFIC(x4) carrier board.
- FPGA(x2) cluster board.
- Master board:
  - Power regulation (DC/DC)
  - Data concentrator FPGA
  - Data links GBT (x8 links)

– Half ROB:

8xSiPM Flex +
4xPACIFIC Carrier +
4xClustering +
1xMaster Board



PACIFIC design

Low **P**ower **A**SIC for the S**CI**ntillating **FI**bre Tra**C**ker readout.
Design collaboration between different institutes and countries:

- Universitat de Barcelona
  (Barcelona, Spain)
- Instituto de Fisica Corpuscular
  (Valencia, Spain)
- Physikalisches Institut
  (Heidelberg, Germany)
- Laboratoire de Physique de Clermont
  (Clermont Ferrand, France)

PACIFIC: Initial goals

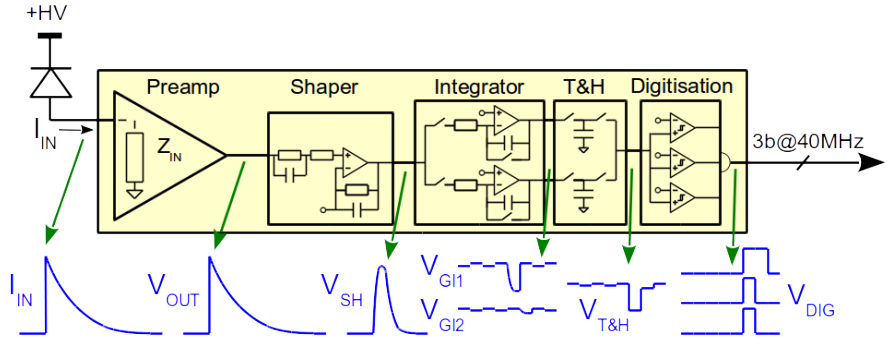
Initial specifications of ASIC:

- 128 channels readout.
- Sensor bias adjustable channel by channel.
- Low input impedance.
- No components needed between sensors and ASIC.
- Shaper to fit both manufacturers timing.
- Double peak resolution of 25ns (no dead time).
- 6 bit ADC per channel.
- Clustering on ASIC.
- 1W maximum power.

PACIFIC: Realistic/corrected goals

- × 64 channels readout.
- ✓ Sensor bias adjustable channel by channel.
- ✓ Low input impedance.
- ✓ No components needed between sensors and ASIC.
- ✓ Shaper to fit both manufacturers timing (two different shapers).
- ✓ Double peak resolution of 25ns (no dead time) (double gated integrator).
- × 6 bit ADC per channel (6bx128chx40MHz = 30Gbps/ASIC), changed to 3 non linear Flash ADC.
- × Clustering on ASIC (algorithm not clear, not enough time).
- × 0.5W maximum power.
- × 15ns of "correct" integration for different time of arrival with 10% of maximum spill-over.

PACIFIC: Analog Channel processing



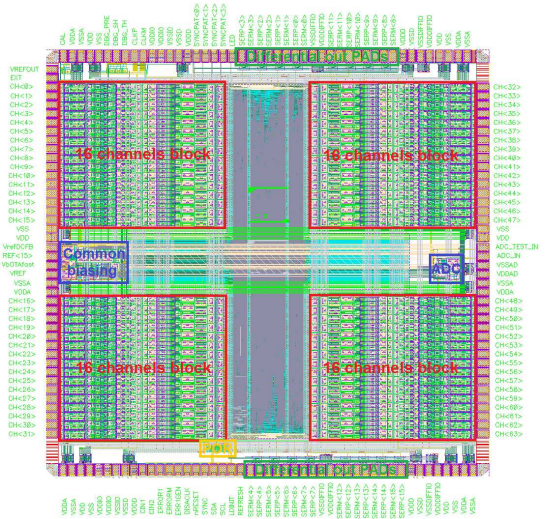
Preamplifier, Shaper, Integrator, Track and Hold and Digitization

PACIFIC: Other stuff on chip

- Common biasing:
  - Voltage references
  - Current references
  - DACs
  - Monitoring ADC
  - Power on Reset
  - SLVS Receivers / Drivers
- Digital blocks:
  - Encoding and serialization of data:
    (4 channels, 320 MHz clock).
  - Slow control (I2C).
  - Hamming encoding:
    Digital mitigation of SEUs in configuration registers.

PACIFICr5 floorplan

- 16 channels groups
- 32 channels left/right
- I2C in central area
- Central left for common bias
- Central right for ADC/debug
- Main power rails from top to bottom
- Differential outputs at top and bottom



IBM 130nm

2013

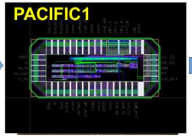
PACIFICr0

Preamplifier
from AMS 0.35

2014

PACIFICr1

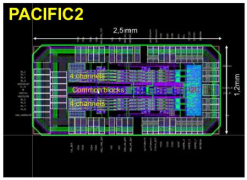
Three analog channels
Different test structures
First I2C



2014

PACIFICr2 / 2b

8 channels
Common bias
I2C



To improve:

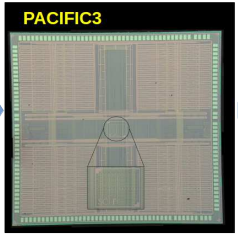
Uniformity
Integration/shaping

TSMC 130nm

2015

PACIFICr3

64 channels
2xCommon bias
I2C



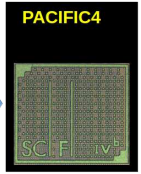
To improve:

Uniformity
Track and Hold slew rate
Add local thresholds

2016

PACIFICr4 / 4b

64 channels
Common bias
I2C, ADC, local DACs 8b
Single ended output



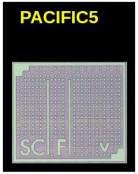
To improve:

Uniformity / trimming
Baseline holder
Track and Hold
Comparators range

2017

PACIFICr5

64 channels
Common bias
I2C, ADC, local DACs 8b
Differential out SLVS



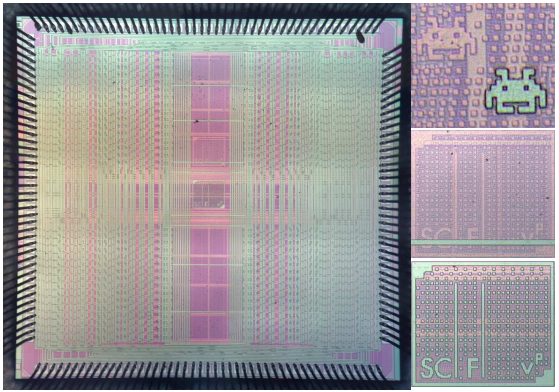
To improve:

Spillover

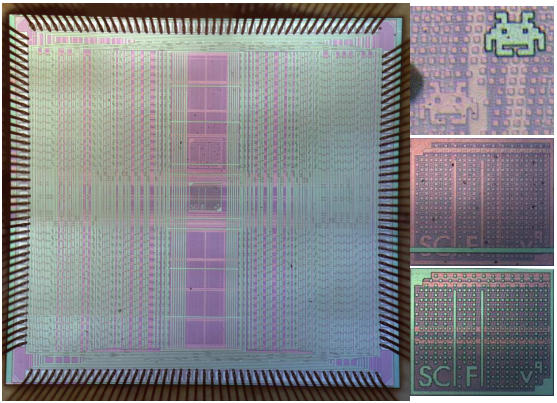
– **PACIFICr5pq production submitted in January 2018.**

PACIFICr5pq - Visual inspection

PACIFICr5p



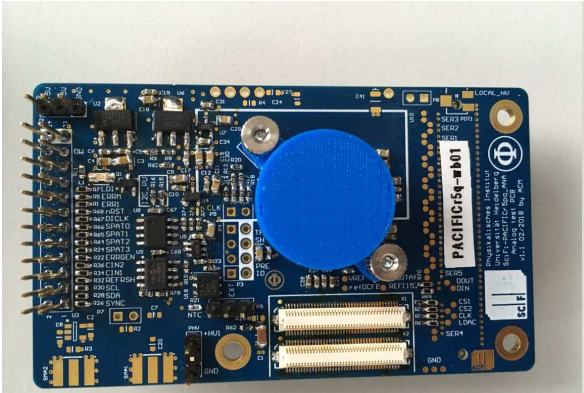
PACIFICr5q

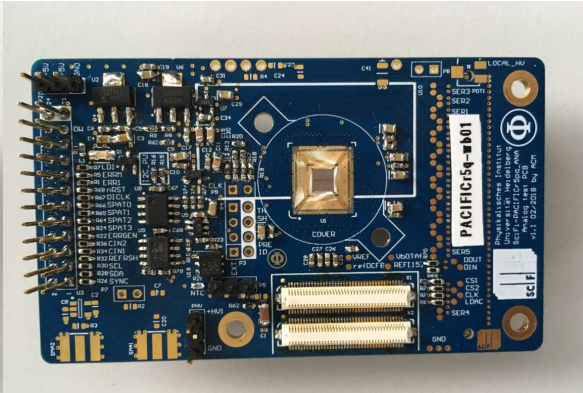


– Highly usage of top Al routing for power distribution.

PACIFICr5 test board

- Same digital FPGA based motherboard with USB connection.
- New Analog test board with removable cover.

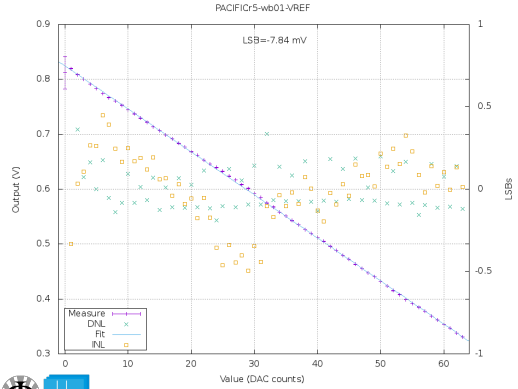




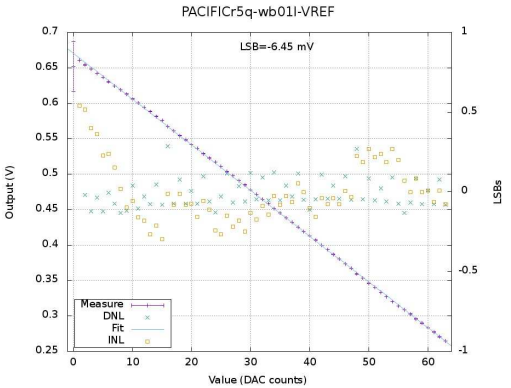
PACIFICr5pq - VREF DAC

- PACIFIC production "soft start".
- Changed slope and offset to have smaller initial VREF.

PACIFICr5



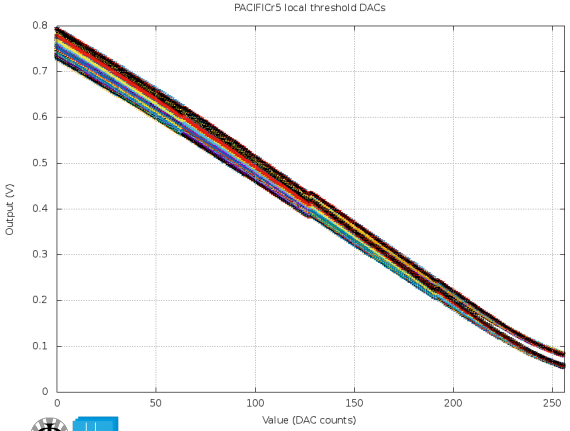
PACIFICr5pq



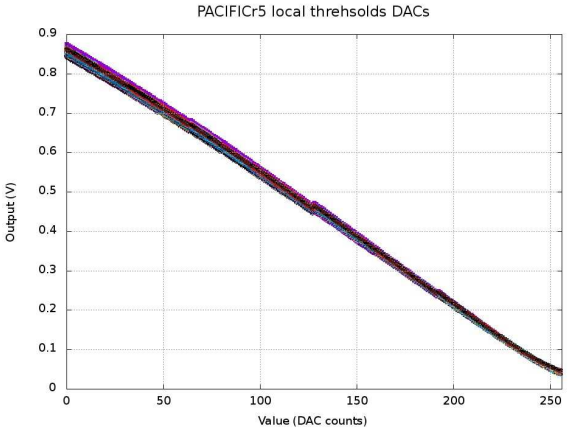
PACIFICr5 - Local Threshold DACs

- Improved power distribution, even better uniformity.

PACIFICr5



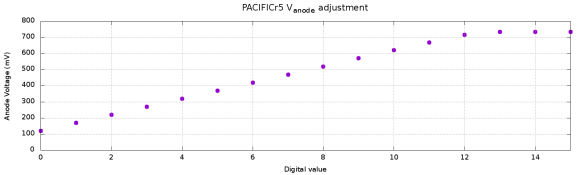
PACIFICr5pq

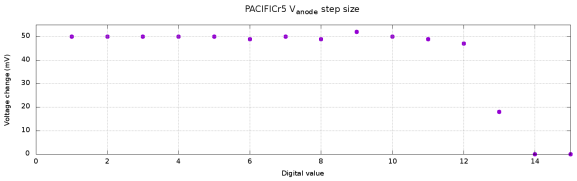


PACIFICr5pq - Vanode control

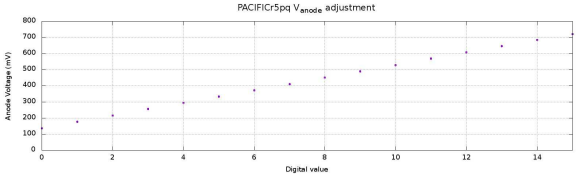
- Step reduced to 40 mV range adjusted to usable range (120mV-720mV).

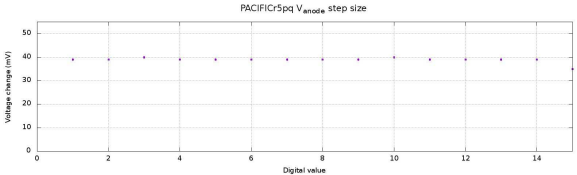
PACIFICr5



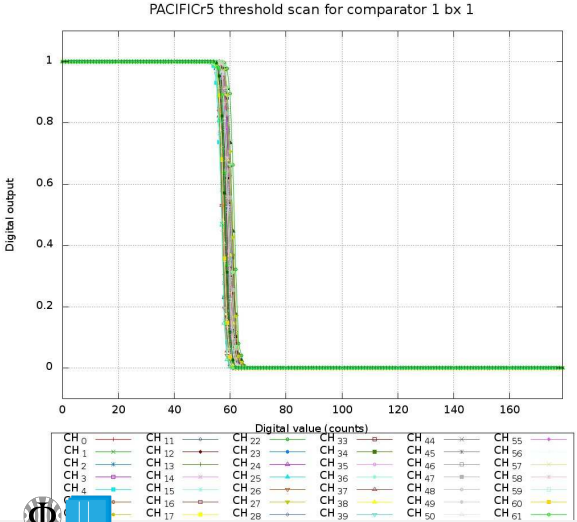


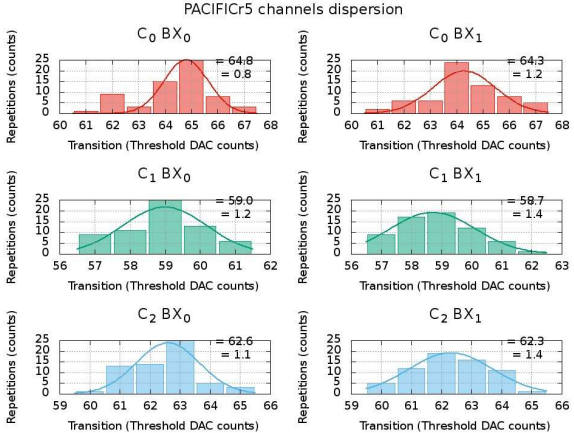
PACIFICr5pq





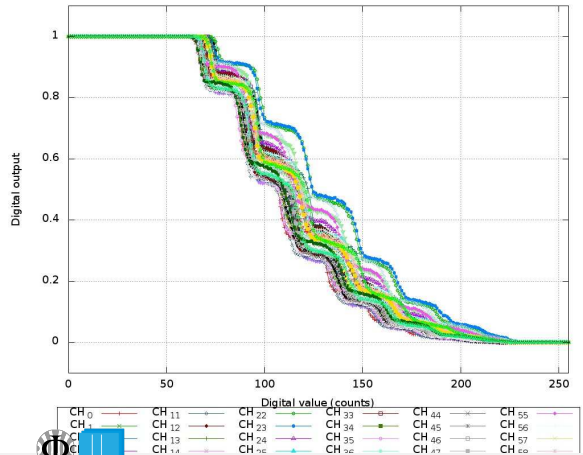
PACIFICr5 - Trimming



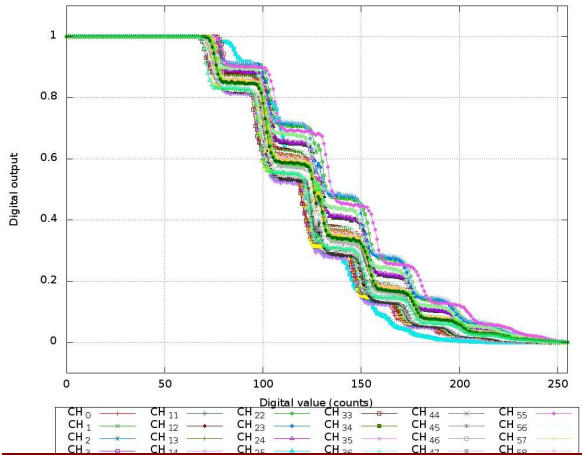


PACIFICr5pq - Light s-curve

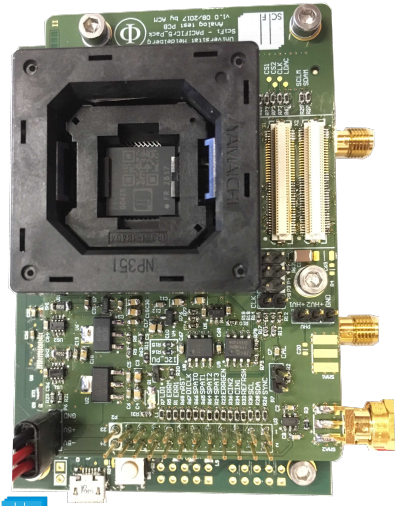
PACIFICr5p



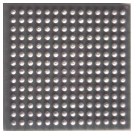
PACIFICr5q

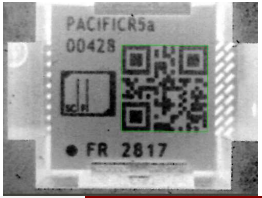


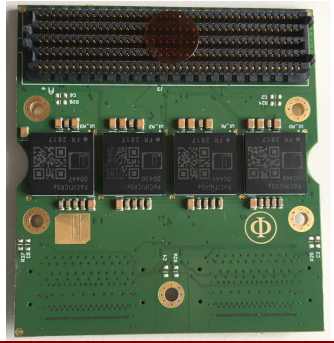
PACIFICr5 - Package



- Received 1482 PACIFICr5p/q.
- QR marking readable in socket.
- Several devices tested with socket.
- Devices on Carrier Boards.

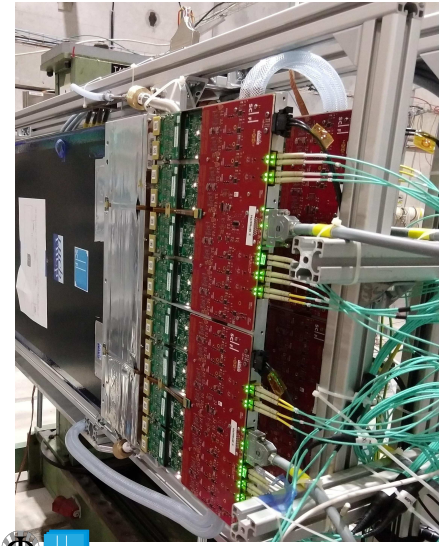




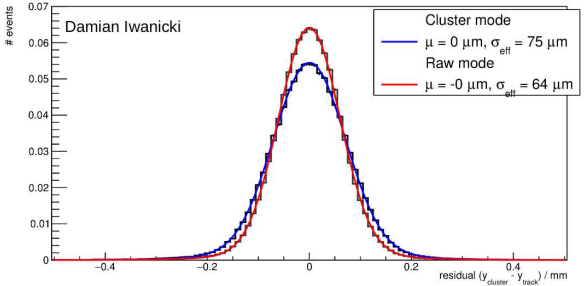


Test-beam @ CERN

Test-beam @ CERN

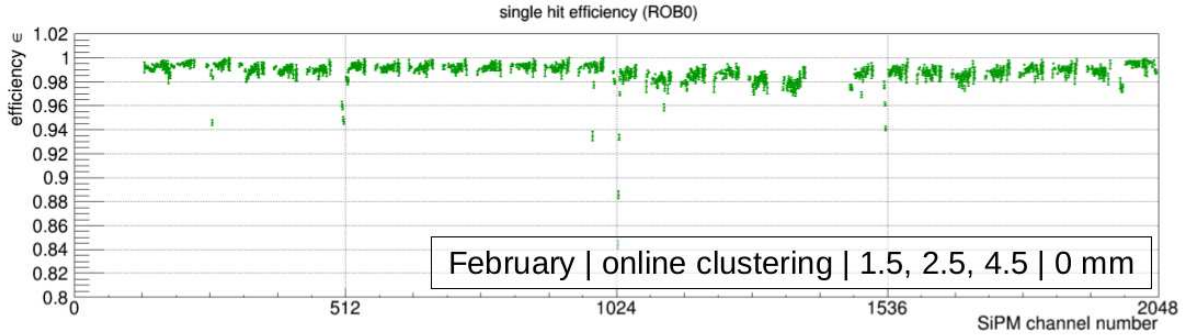


- First time with full system.
- Two half modules with full readout.
- Final DAQ (miniDAQ2).
- Raw and clustered data taking modes.



Test-beam @ CERN

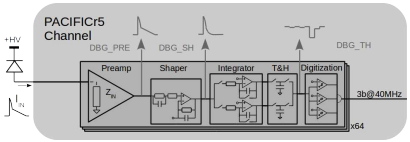
–Efficiency taking telescope as reference with default configuration.
–Thresholds set at 1.5/2.5/4.5 phe.

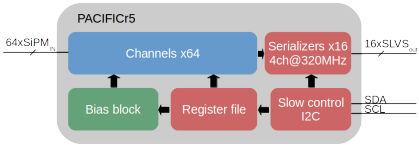


from Simon Nieswand

PACIFIC architecture validated

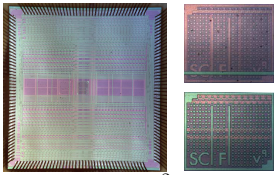
Low Power ASIC for the SCIntillator FIbres traCker





Channel processing chain:

- High bandwidth current input.
- Anode voltage control.
- Fast Shaper for tail adjustment.
- Double interleaved gated integrator.
- Track and hold.
- Digitization with 3 hysteresis comparators.
- Serialization and slow control.

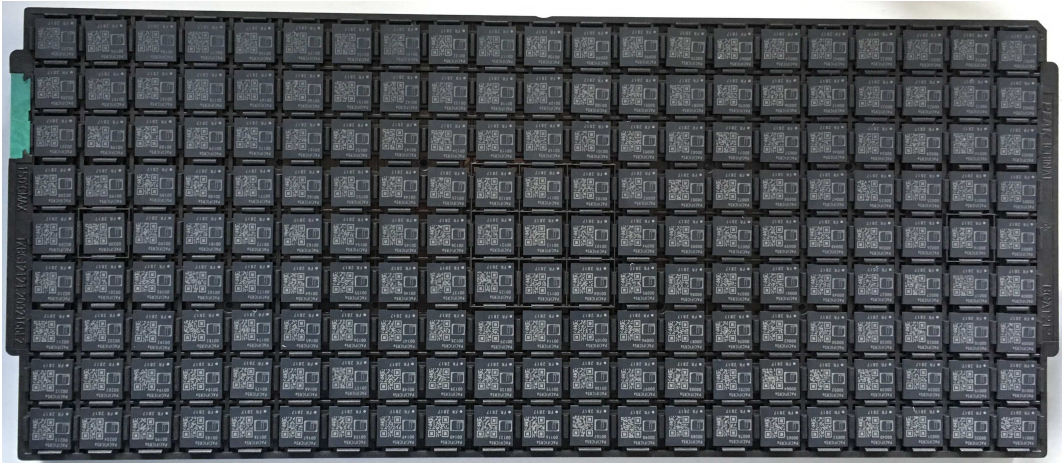


4x3.85mm^2

BGA package
$12 \times 12 mm^2$
196pins

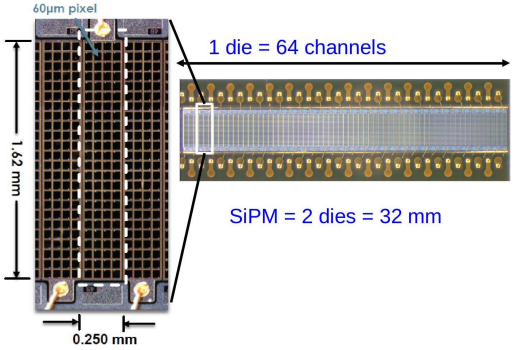
- **Successfully achieved desired performance in test-beam.**
- **Mass production test and assembly, $\approx$ 23k devices.**

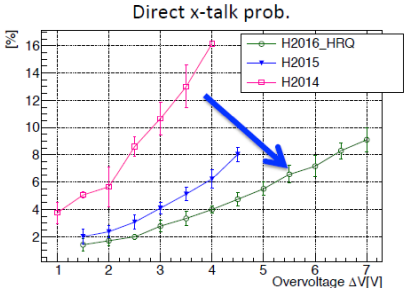
Thanks for your attention!

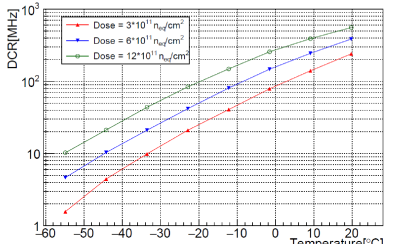


Backup slides

Silicon Photo Multipliers



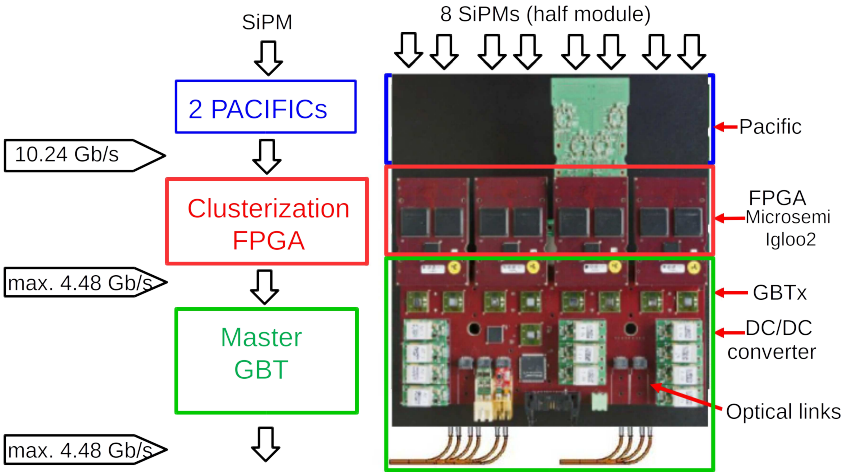




- Peak PDE = 48% (3.5 V)
- Cross-talk = 3%
- Delayed cross-talk = 2.5%
- Afterpulses < 0.1%

DCR halved every -10°C

Data throughput

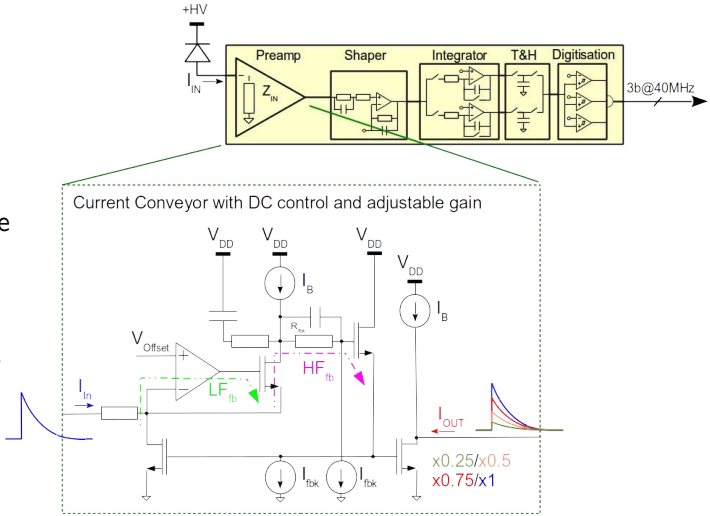


SCiFi (528k channels) - 4096 GBT links (max. 2.3 TB/s)

PACIFIC: Preamplifier

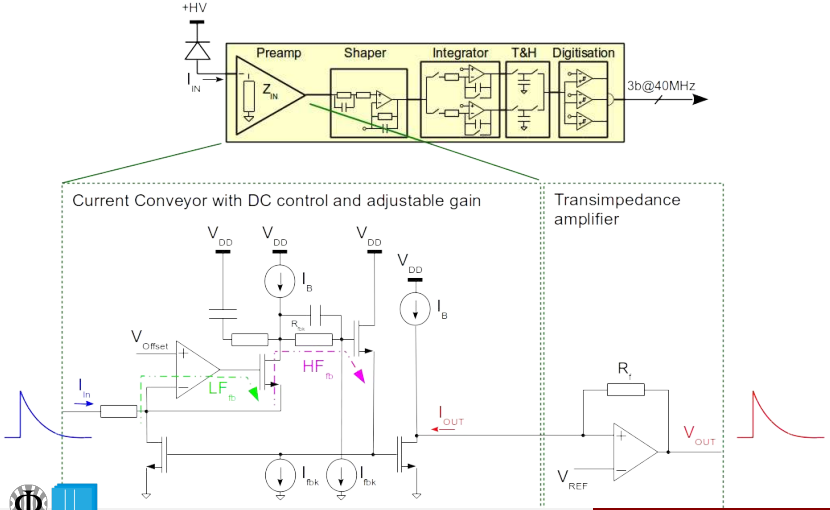
Functions:

- High Bandwidth
- Low input impedance
- Low Power
- Adjustable Gain
- Control on input DC



PACIFIC: Preamplifier output

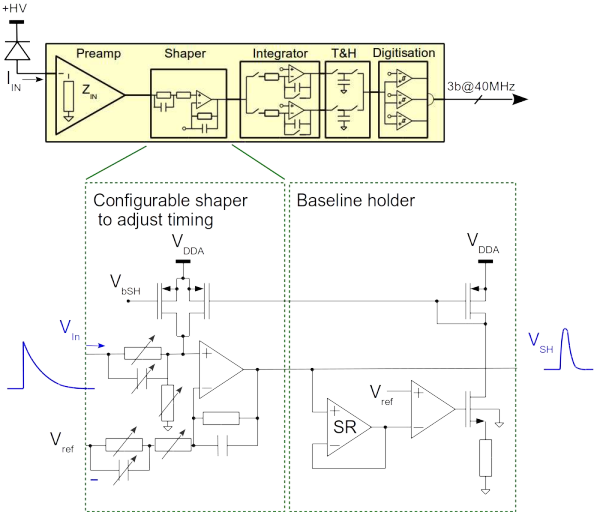
–Trans-impedance amplifier for voltage output and BW limitation



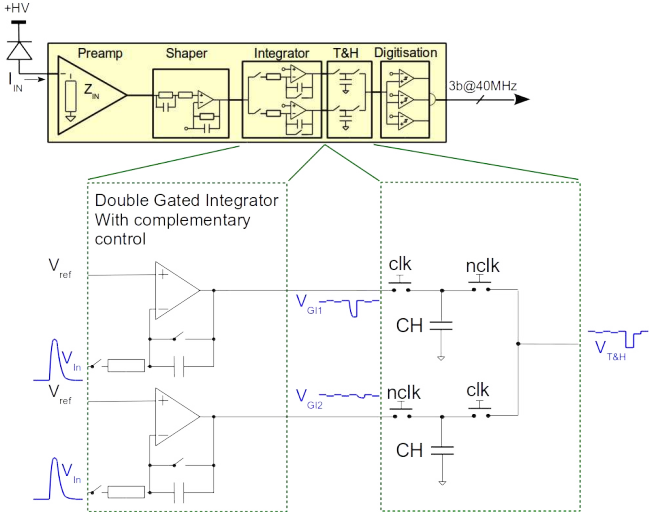
PACIFIC: Shaper

Double adjustable pole-zero configuration:

- Reduce tail of signal (Pole).
- Remove undershoot (Zero).
- Baseline holder afterwards.



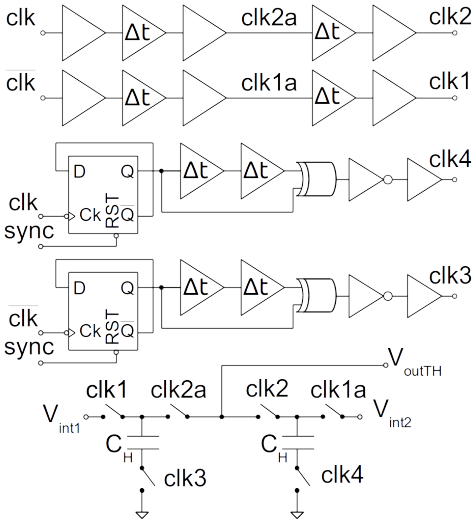
PACIFIC: Gated integrators



- Classical integrator.
- Double gated to avoid dead time.
- Passive Track and Hold at the output.

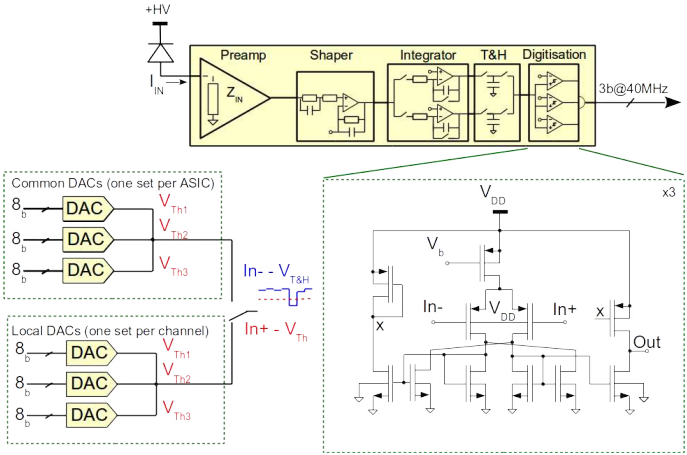
PACIFICr5q: Track and Hold optimization

- PACIFICr5q uses different T&H
- Bottom plate disconnect
- New control signals generated
- Standard cells block
- Slightly delayed switches ON/OFF



PACIFIC: Digitization

- Classical Hysteresis comparator (PMOS).
- Two sets of threhsolds;
  - Common
  - Local

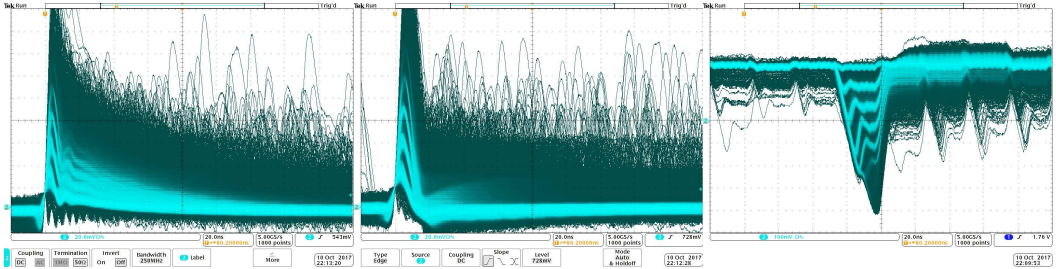


PACIFICr5x-wb0Y - POR values

DUT	$I_{CCTotal}$	VREF	$Vref_{DCFB}$	$VOTA_{fast}$	REF
PACIFICr5p-wb01	**416**	468	670	890	666
PACIFICr5p-wb02	**381**	451	655	882	644
PACIFICr5p-wb03	**448**	480	698	871	687
PACIFICr5q-wb01	**417**	470	686	874	665
PACIFICr5q-wb02	**429**	476	691	874	681
PACIFICr5q-wb03	**426**	480	678	878	678
PACIFICr5p-wb01*	**481**	502	701	877	714
PACIFICr5p-wb02*	**486**	503	699	860	715
PACIFICr5p-wb03*	**487**	497	698	870	709
PACIFICr5q-wb01*	**495**	504	704	862	712
PACIFICr5q-wb02*	**478**	497	700	867	711
PACIFICr5q-wb03*	**478**	500	700	871	707

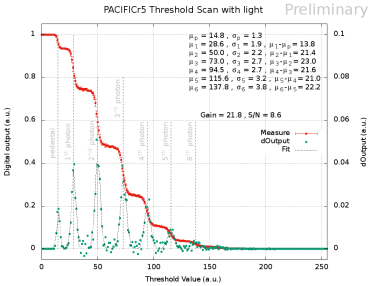
*After internal DACs correction

PACIFIC



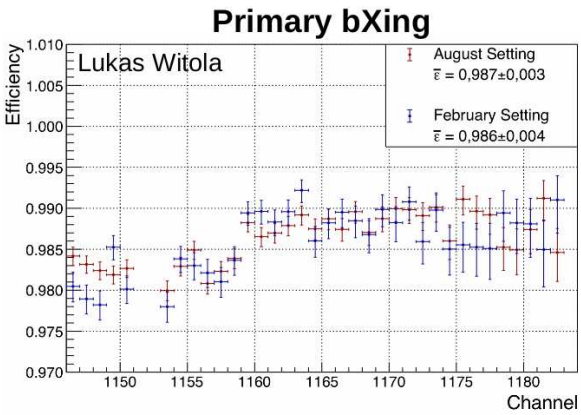
SiPM connected to PACIFIC:

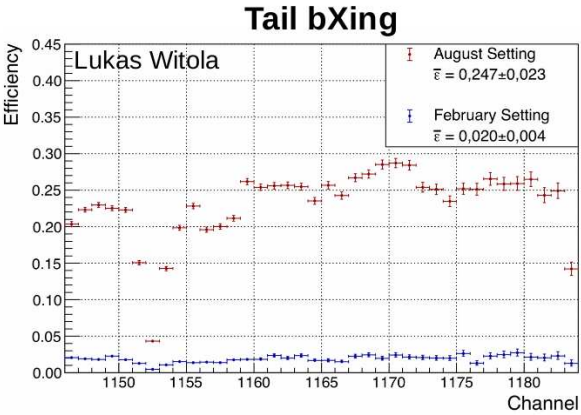
- Analog DEBUG outputs for Preamp, Shaper and TH.
- Synchronous light triggered on front of array.
- Threshold scan of one comparator to measure photons.



PACIFICr5q - Spillover

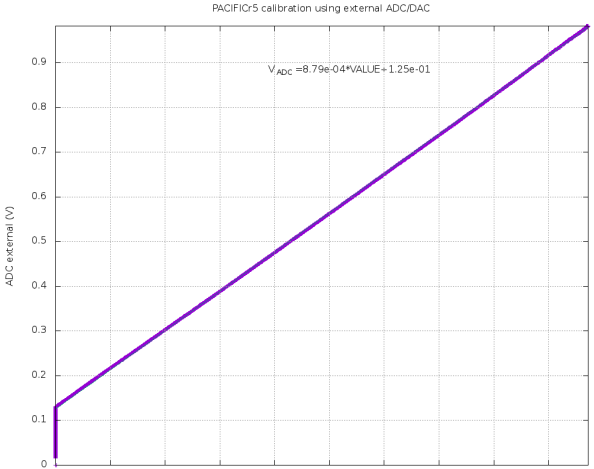
–Spillover dependency on PACIFIC configuration.
–Testbeam data after clustering.





PACIFICr5 - Internal ADC

- Internal ADC calibration using external DAC/ADC.



PACIFICr5 - Temperature sensor

- Used one point for temperature sensor calibration ($\pm 5\%$ error expected).