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PACIFIC: The readout ASIC for the SciFi Tracker of the LHCb detector

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PACIFIC is a 64 channel mixed-signal ASIC designed for the scintillating fiber (SciFi) tracker developed for the LHCb upgrade in 2019/20. It connects without interface to the 128 channel double die SiPM arrays sensing the fibers. The analog processing begins with a current conveyor followed by a tunable fast shaper and a gated integrator. The signal is digitized with a 2bit nonlinear flash ADC operating at 40MHz. The results of every two channels are serialized and transmitted at 320MSa/s over a differential SLVS data link. PACIFIC has been designed using a 130nm CMOS technology and power consumption kept below 10mW/channel.

Summary

During the Long Shutdown 2 (LS2) of LHC in 2019/20 and as a part of the LHCb upgrade, the Tracking Stations downstream from the magnet will undergo a detector technology change. A new tracker, built of 2.5m long and 250µm thick scintillating fibres sensed with silicon photomultipliers (SiPMs), will be installed to cope with the increased hit occupancy and radiation environment, allowing to increase the readout rate to 40MHz.
The low-Power ASIC for the sCIntillating FIbres traCker (PACIFIC) grants the 40MHz readout of the scintillating fibers with reduced dead time. It will connect directly to the anode of the SiPMs, performing the sensor signal analog processing and digitization of 64 channels. The power budget was limited to 10mW/channel. The 130nm CMOS process was chosen for its reduced featured size, low power and wide use in radiation-tolerant applications.
The input stage is a current mode amplifier composed of a current conveyor and a closed-loop trans-impedance amplifier. The current conveyor is based on a novel double feedback approach and optimized for SiPM arrays with anode connections. The double loop provides independent control over the anode voltage and the input impedance over the full bandwidth (>250MHz). This stage has a low power consumption (<2mW) and a selectable gain that assures a good single cell resolution for calibration.
The signal received by the ASIC extends over several LHC clock cycles, mainly due to the recovery of the SiPM. Additionally, the distribution of the time of arrival of the scintillation light spreads over 60% of the LHC clock cycle. The goal of the shaping stage is to reduce the pulse width to allow a 10ns integration, thus minimizing spillover and the effect of the signal arrival time on pulse height measurement. A tunable double pole-zero shaper allows to independently cancel the longer exponential decay related to different SiPM capacitances and quenching resistors, as well as the shorter time component, associated with parasitic capacitance and the amplifier input impedance. It is a closed-loop design based on an OTA with high gain-bandwidth product (>300MHz), low power consumption (<700µW), and high load-driving capability, for a fast rising edge. The output offset is controlled using an additional ultra low slew rate baseline restoration feedback loop.
The pulse is accumulated with a gated integrator based on an amplifier with sufficient gain-bandwidth product (>150MHz), low power consumption (<400µW), and high slew-rate (>100V/µs). The integration time was set close to the full clock period to cope with the dispersion of the signal time of arrival, so two integrators had to be interleaved to allow time for reset.
Three hysteresis comparators with tunable references complete the 2bit nonlinear flash ADC operating at 40MHz. Finally, a serializer generates a 320MS/s stream from the data of four channels.
Packaged devices production status and tests including latest prototypes test-beam campaigns results will be presented to demonstrate the high efficiency and low resolution achieved with the full combined system.

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