

Development of ultra-low power, rad-hard SAR ADCs in 130 nm CMOS technologies

Jakub Moroń¹

M. Firlej¹, T. Fiutowski¹, M. Idzik¹, S. Kulis², K. Świentek¹

1) AGH University of Science and Technology, Krakow, Poland

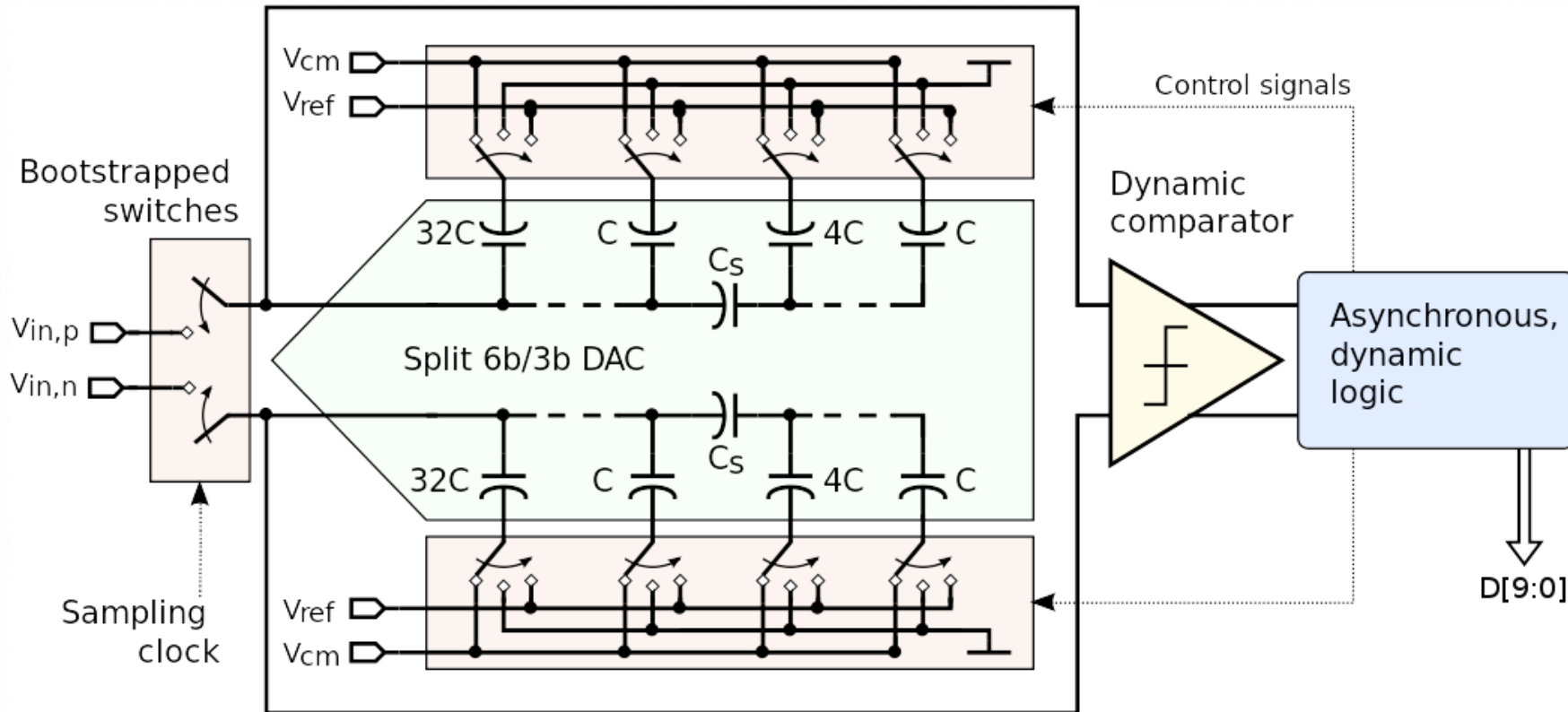
2) CERN

This work was supported by the European Union Horizon 2020 Research and Innovation programme under Grant Agreement no.654168 (AIDA-2020) and by the Polish Ministry of Science and Higher Education under Contract No. 3501/H2020/2016/2

This work was partially supported by the AGH-UST, statutory tasks No. 11.11.220.01/4 within subsidy of the Ministry of Science and Higher Education



- Architecture of 10-bit SAR ADC
 - Differences between prototypes
- Measurement results
 - Static and dynamic metrics, FOM and power consumption
- Irradiation tests
 - Setup
 - Results:
 - Process A
 - Process B, 1st prototype
 - Process B, 2nd prototype
- Summary



Architecture of 10-bit ADC

- Differential segmented/split DAC with MCS switching scheme - **ultra low power**
- Dynamic comparator - **no static power consumption**
- Asynchronous logic - no clock tree - **power saving, allows asynchronous sampling**

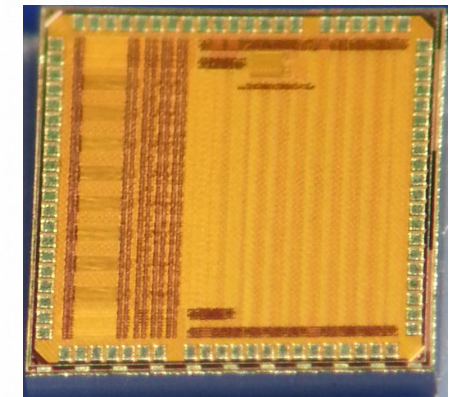
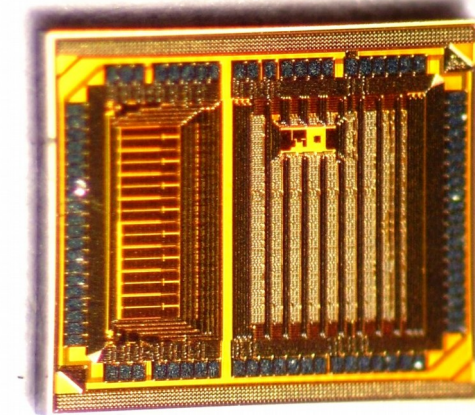
Design consideration:

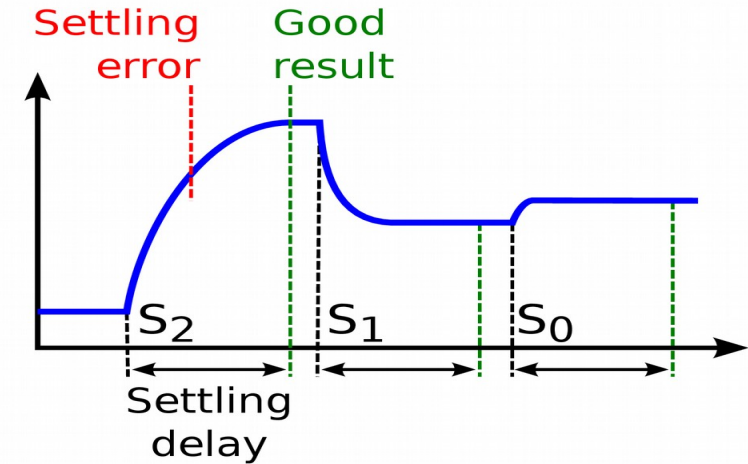
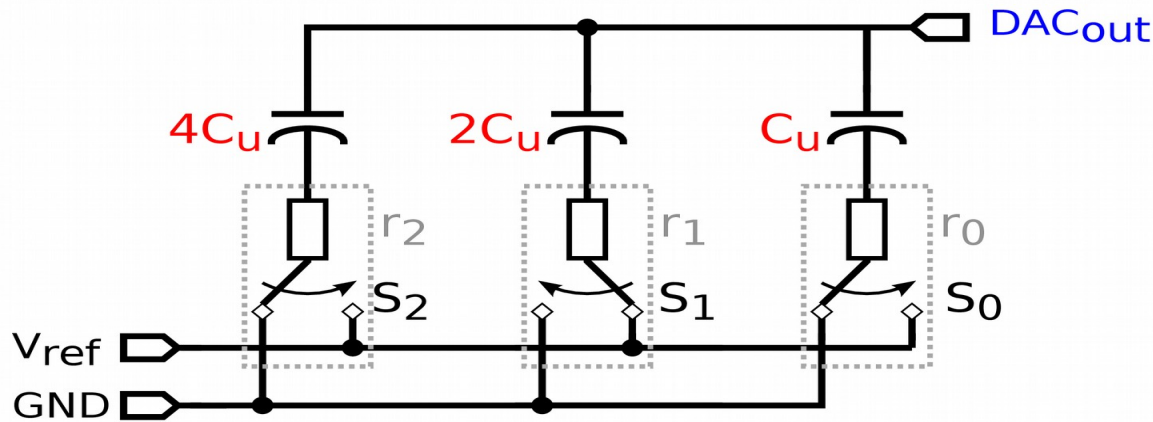
- Variable sampling rate (up to ~50 MSps)
- Power consumption <1 mW at 40 MSps, scalable with sampling rate

Three 8-channel ADC ASICs:

- **130 nm process A** (*fabricated in 2012*)
 - $C_u = 40.0$ fF, $C_{in} = 2.86$ pF, designed for $3\sigma_{DNL} < 1$ LSB
 - Fixed settling delay ratios → limited sampling rate

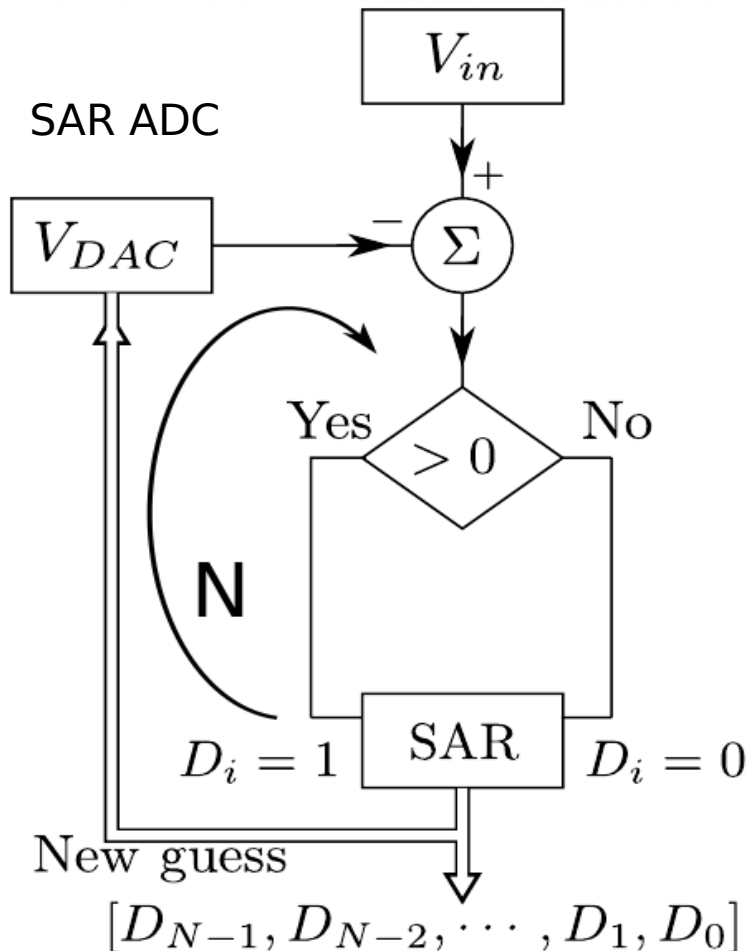
- **130 nm process B**
 - $C_u = 26.2$ fF, $C_{in} = 1.68$ pF, designed for $3\sigma_{DNL} < 0.5$ LSB
 - **1st prototype (FAB14)** (*fabricated in 2014*)
 - Fixed settling delays → limited sampling rate
 - Only nominal (10-bit) resolution
 - **2nd prototype (FAB6)** (*fabricated in 2015*)
 - Configurable settling delays → improved linearity and sampling rate
 - Configurable resolution





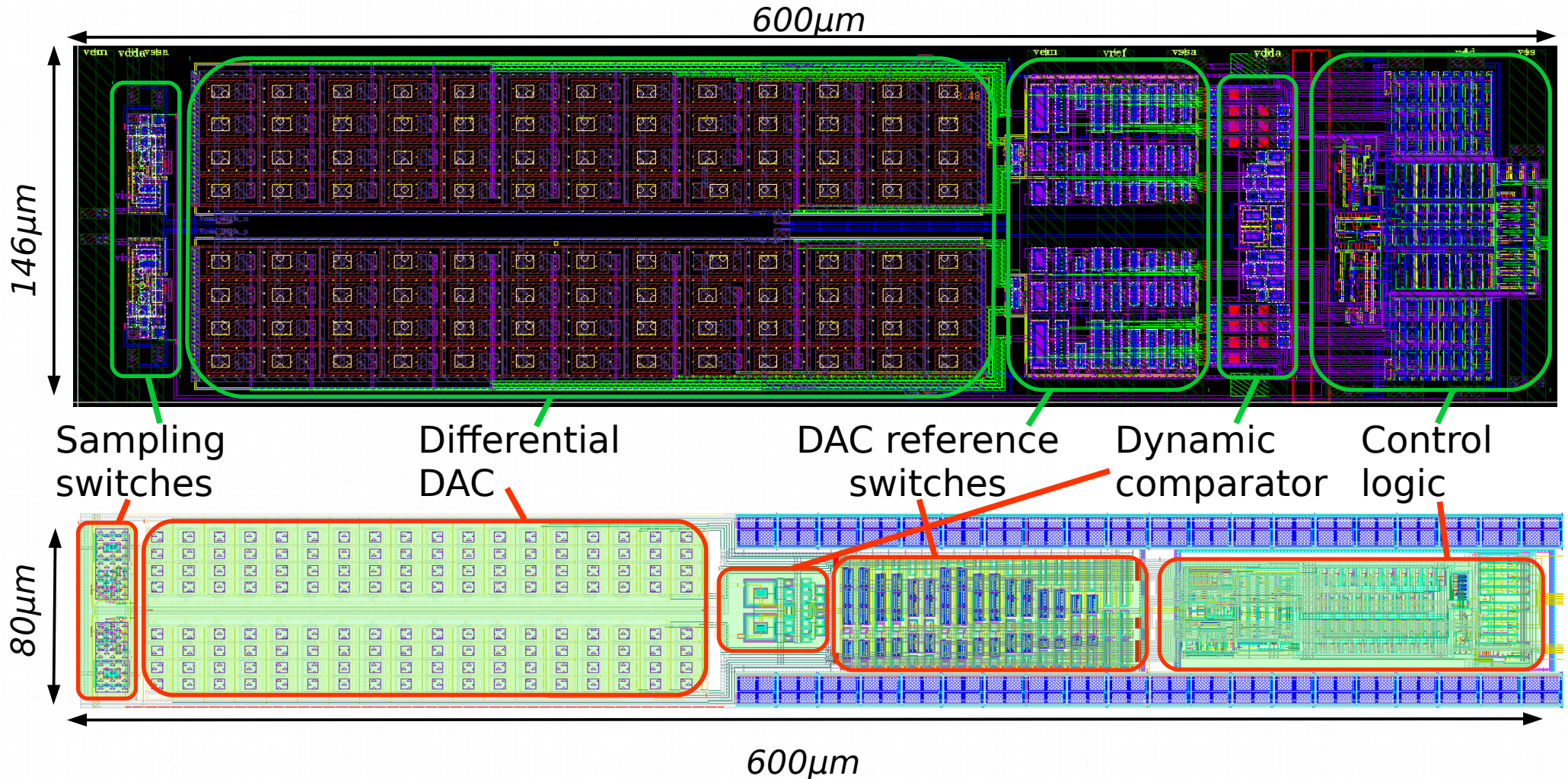
- Making settling time equal for each bit almost impossible
- Constant settling delay for each bit → a lot of time wasted...
- Two versions of variable settling delay implemented in different prototypes

Prototype	Bit no.	9	8	7	6	5	4	3	2	1
Process A, Process B, 1 st	Group	A [9-8]		B [7-5]			C [4-1]			
	Delay	$t_c + \Delta t_A$ (fixed)		$t_c + \Delta t_B$ (fixed)			Adjustable t_c			
Process B, 2 nd	Group	A [9]	B [8-7]		C [6-5]		D [4-1]			
	Delay	Adjustable t_A	Adjustable t_B		Adjustable t_C		Adjustable t_D			



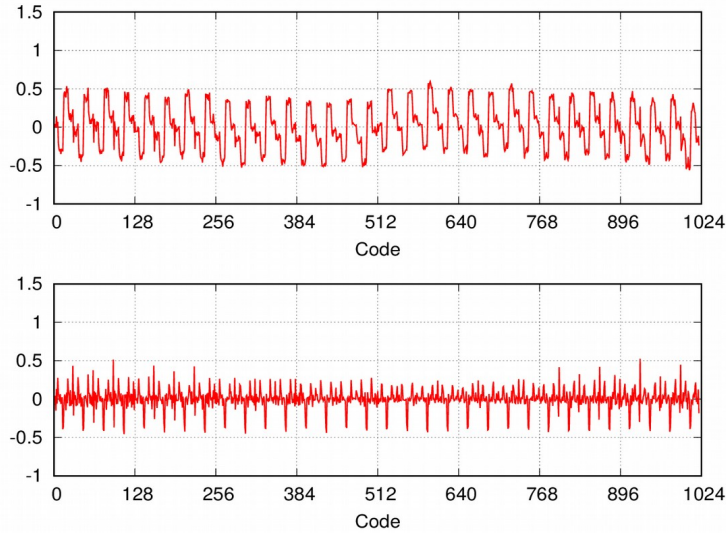
- In SAR ADC the same circuitry is used in loop N-times for N-bit resolution
- If conversion is interrupted earlier (e.g. after K-times), ADC resolution is limited to K-bit
- Configurable resolution implemented in 2nd prototype in process B
- Resolution can be reduced from 10b up to 5b with one bit step (**nominal 10b, 9b, 8b, 7b, 6b, 5b**)
- **Unused bits (e.g. LSb for 9-bit resolution) are masked to zero in output data register**

Process A - 8 channels ASIC submitted and fabricated in **2012**



Process B - two 8-channels ASICs submitted and fabricated in **2014 (1st prototype)** and **2015 (2nd prototype)**

Process A



$$-0.46 < \mathbf{DNL} < 0.53$$

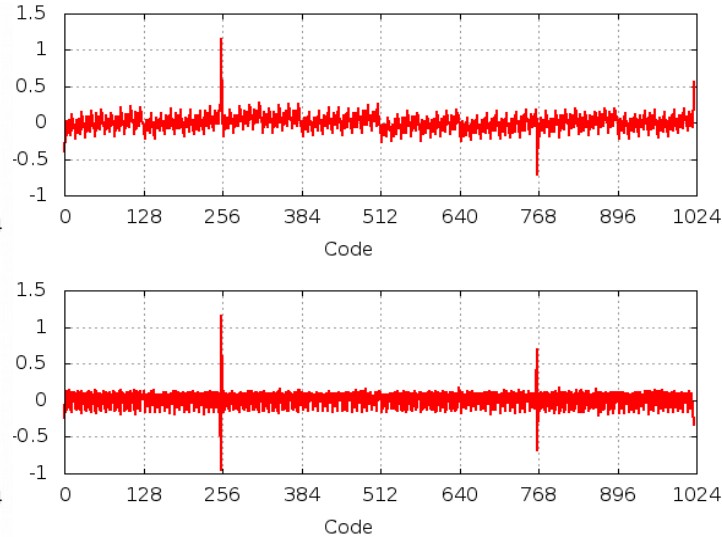
$$-0.56 < \mathbf{INL} < 0.60$$

$$\text{Static } \mathbf{ENOB} = 9.4$$

$$\text{Max sampling rate} \\ \leq \mathbf{40 \text{ MSps}}$$

Process B

1st prototype



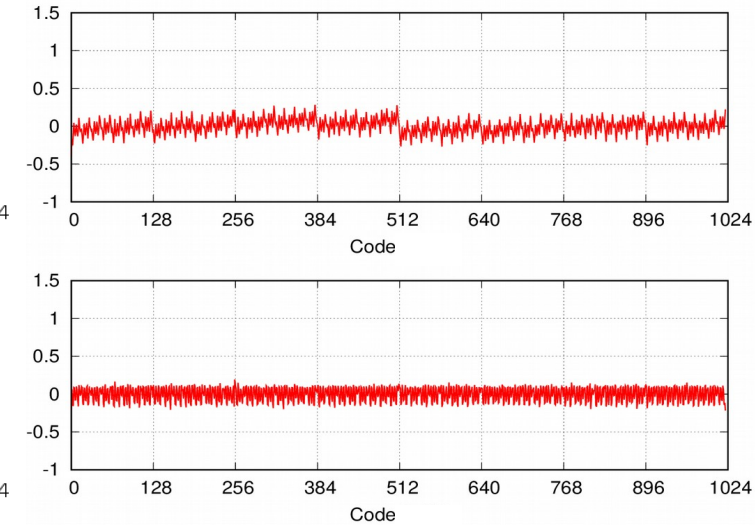
$$(-0.32) -0.96 < \mathbf{DNL} < 1.15 (0.20)$$

$$(-0.40) -0.70 < \mathbf{INL} < 1.15 (0.54)$$

$$\text{Static } \mathbf{ENOB} = 9.78 (9.88)$$

$$\text{Max sampling rate} \\ \leq \mathbf{40 \text{ MSps}} \\ (\leq 30 \text{ MSps with longer settling} \\ \text{delay})$$

2nd prototype



$$-0.22 < \mathbf{DNL} < 0.20$$

$$-0.30 < \mathbf{INL} < 0.40$$

$$\text{Static } \mathbf{ENOB} = 9.92$$

$$\text{Max sampling rate} \\ \leq \mathbf{55 \text{ MSps}}$$

J. Moron at al., A fast, ultra-low power 10-bit SAR ADCs in CMOS 130 nm technology, TWEPP 2016

J. Moron at al., Comparison of two fast, ultra-low power 10-bit SAR ADCs in CMOS 130 nm A and B technologies, TWEPP 2015

J. Moron at al., Development of variable sampling rate low power 10-bit SAR ADC in 130 nm IBM technology, TWEPP 2013

- **Process A**

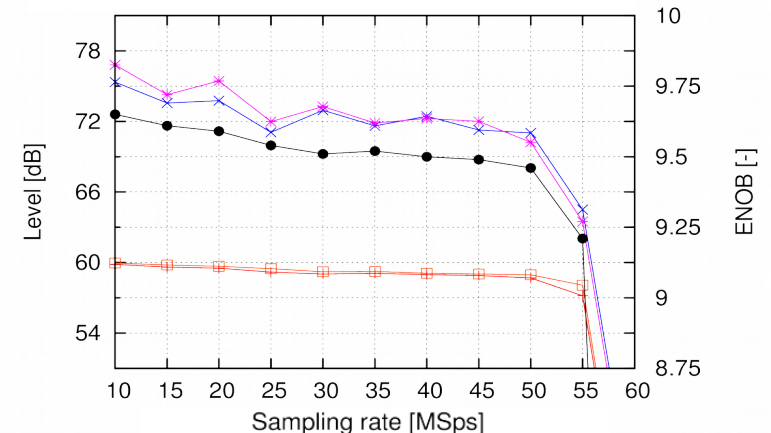
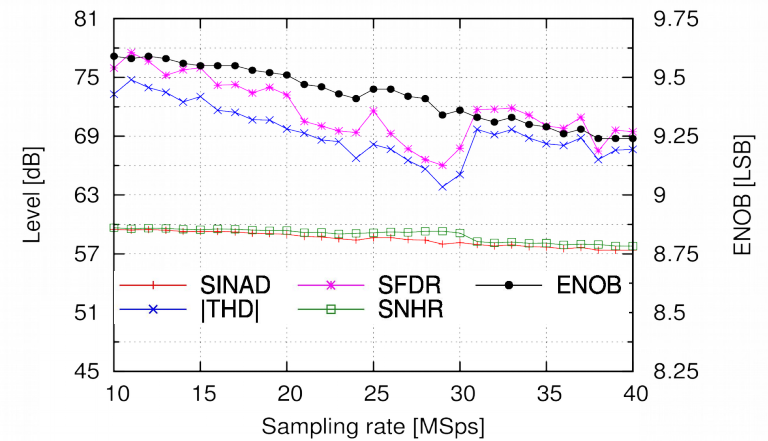
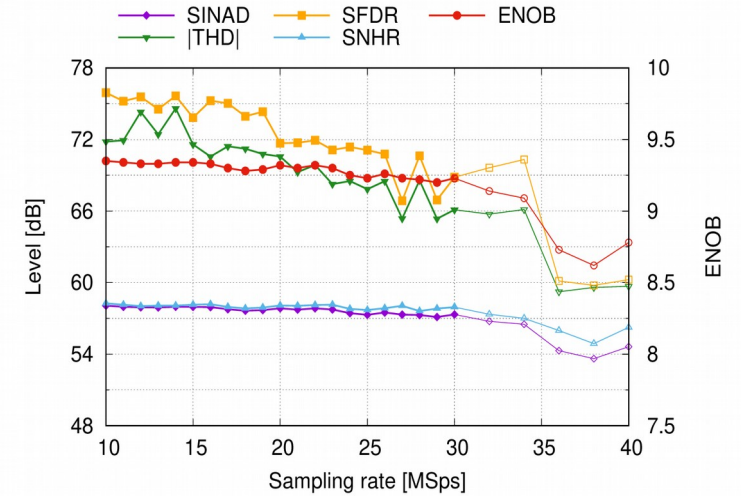
ENOB between **9.35 - 9.20** up to 30 MSps,
for 30-40 MSps between **9.20 - 8.60**
(mostly due to setup issues)

- **Process B, 1st prototype**

ENOB decreasing from **9.6**
to **9.25** at 40 MSps

- **Process B, 2nd prototype**

ENOB higher than **9.5** up to 40 MSps
decreases **9.4** at 50 MSps



- **Process A**

FOM \leq **35 - 37** fj/conv up to **30** Msps
 between **37 - 57** fj/conv from **30** to **40** MSps
 FOM_{lf} \sim **35** fj/conv up to **40** Msps

Power consumption - **880 μ W** at 40 MSps

- **Process B, 1st prototype**

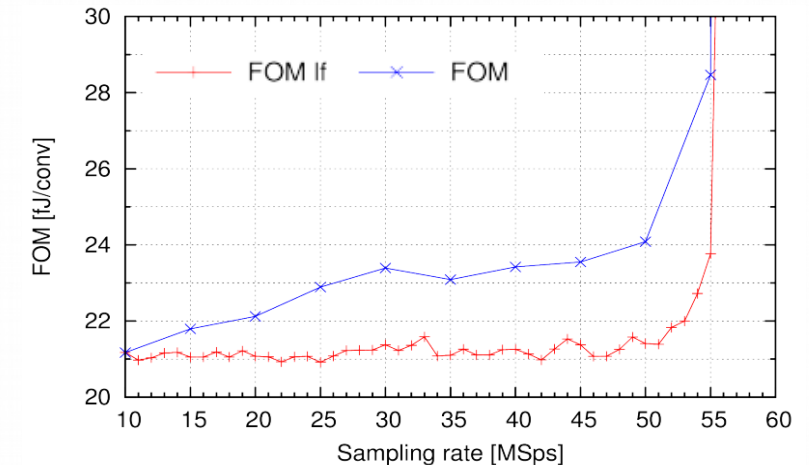
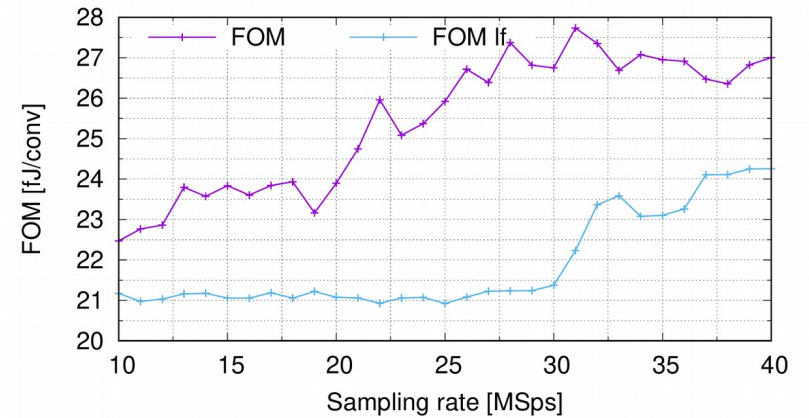
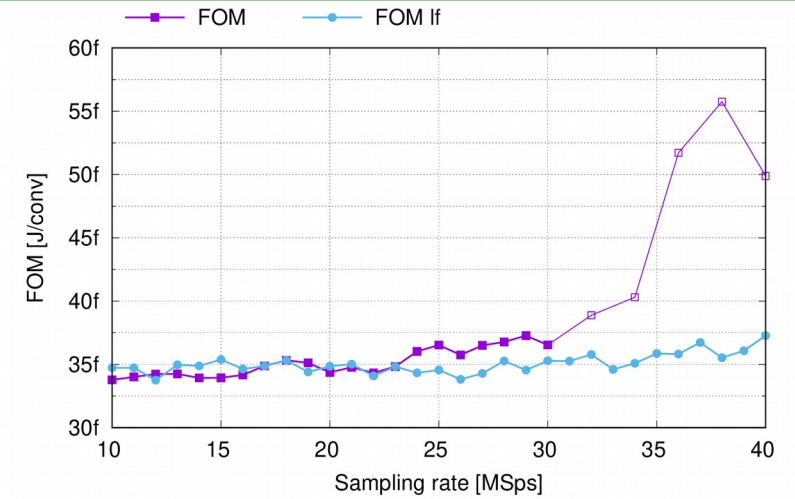
FOM \leq **22 - 28** fj/conv up to **40** MSps
 FOM_{lf} \sim **21** fj/conv up to **30** MSps,
 \leq **25** fj/conv from **30** to **40** Msps

Power consumption - **660 μ W** at 40 MSps

- **Process B, 2nd prototype**

FOM \leq **22 - 24** fj/conv up to **50** MSps
 FOM_{lf} \sim **21** fj/conv up to **50** MSps

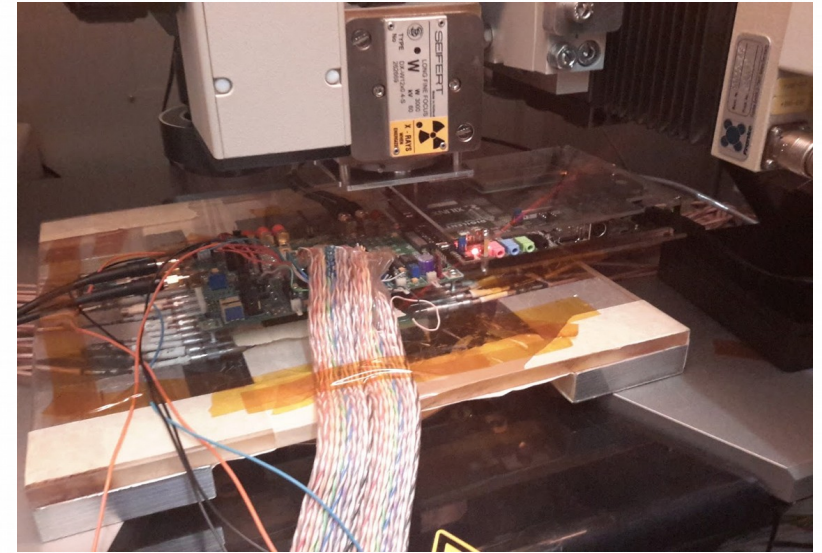
Power consumption - **660 μ W** at 40 MSps



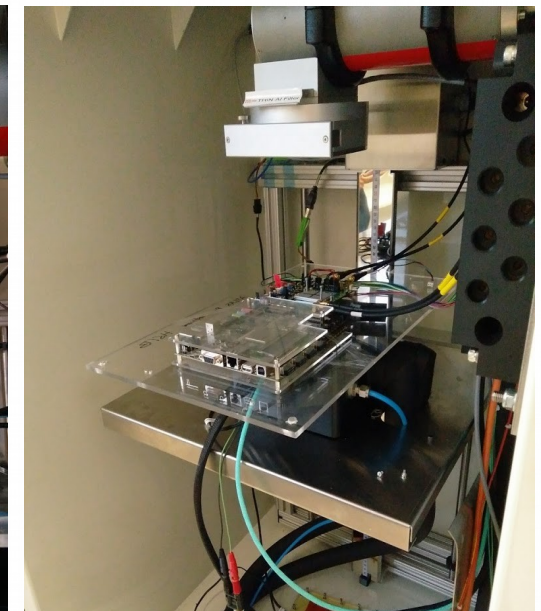
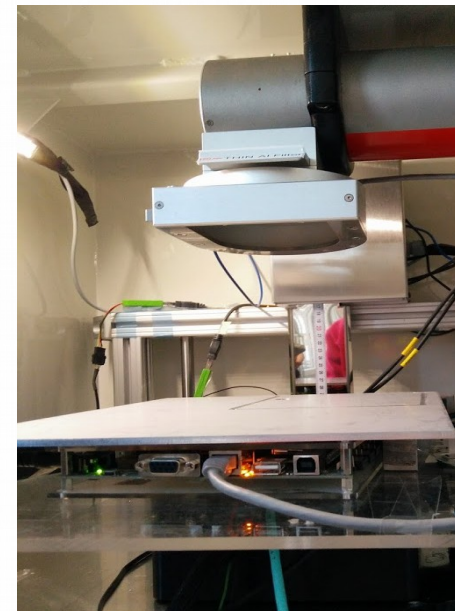
Four radiation campaigns

- Process A
 - Dose up to **120 Mrad**
 - Irradiated in 2015
- Process B, 1st prototype (FAB14)
 - Dose up to **500 Mrad**
 - Irradiated in 2015
- Process B, 2nd prototype (FAB6)
 - Dose up to **14 Mrad**
 - Irradiated in 2016
- Process B, 2nd prototype (FAB6)
 - Dose up to **300 Mrad**
 - Irradiated in 2017

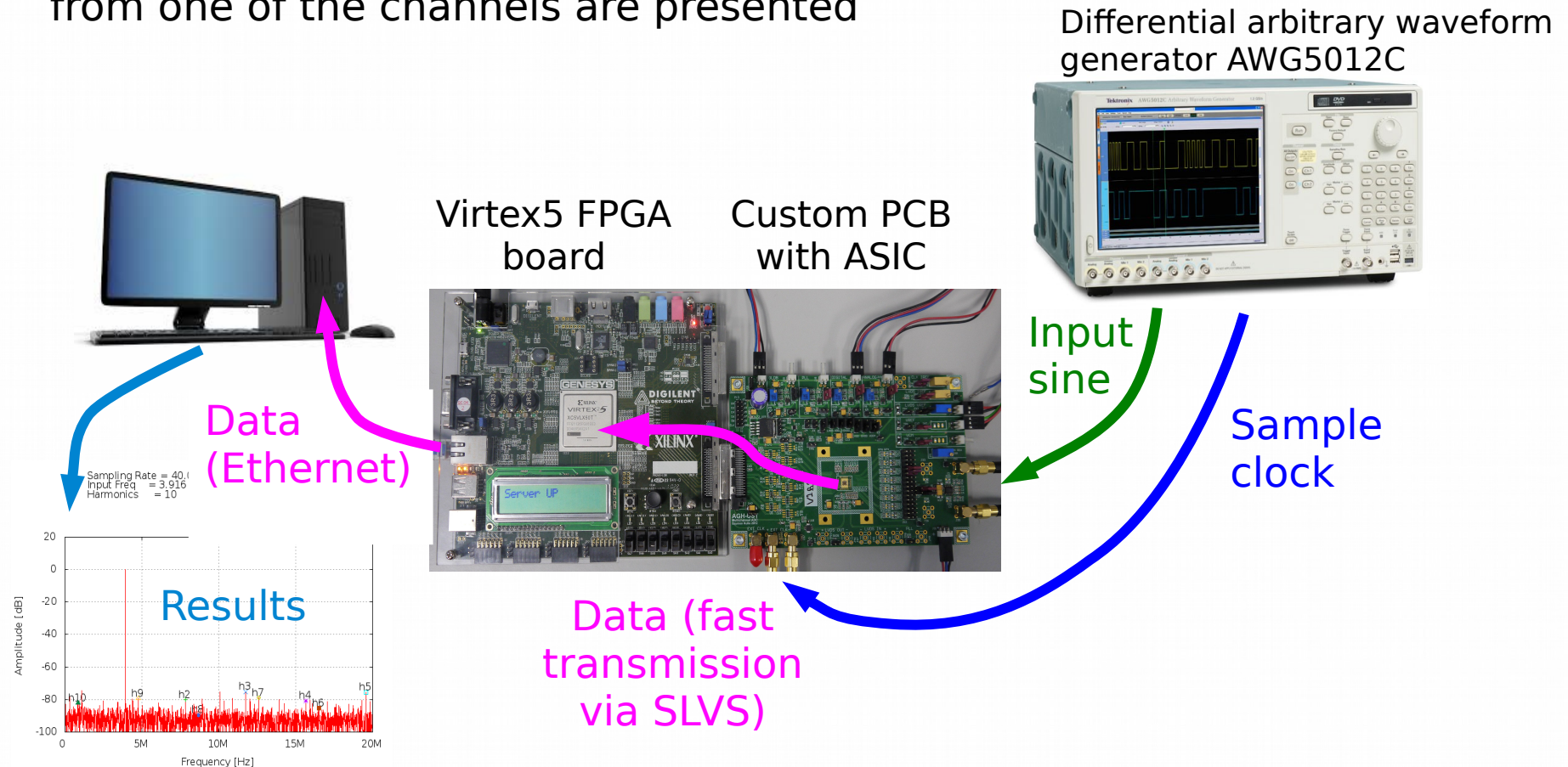
CERN-PH-ESE X-ray machine



ATLAS XRAY machine



- During irradiation tests all 8 ADC channels were active with parallel readout
- Dynamic metrics were measured for two channels
- For remaining six channels different combinations of constant input voltages (mid-scale, full-scale, etc.) were used
- No differences between channels were found, so only the dynamic metrics from one of the channels are presented



Irradiation results - Process A



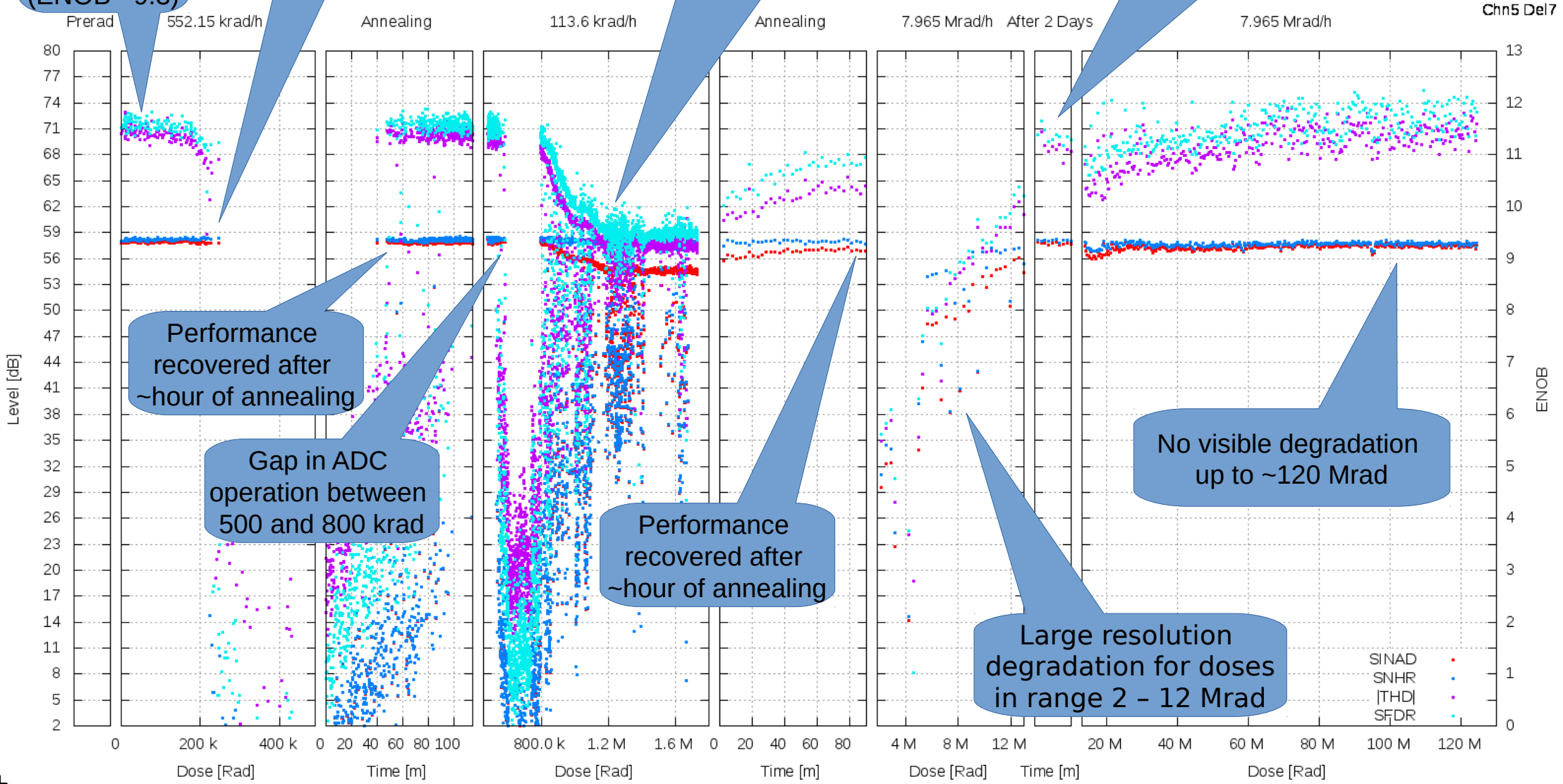
AGH

Good initial performance (ENOB ~9.3)

ADC stopped working after ~220 krad

Constant resolution loss (from ~9.3 to ~8.8) up to 1.6 Mrad

Two days of annealing Performance recovered



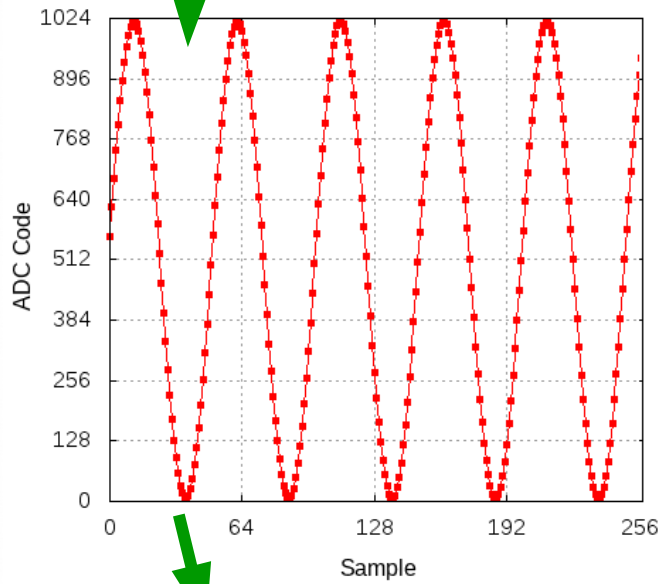
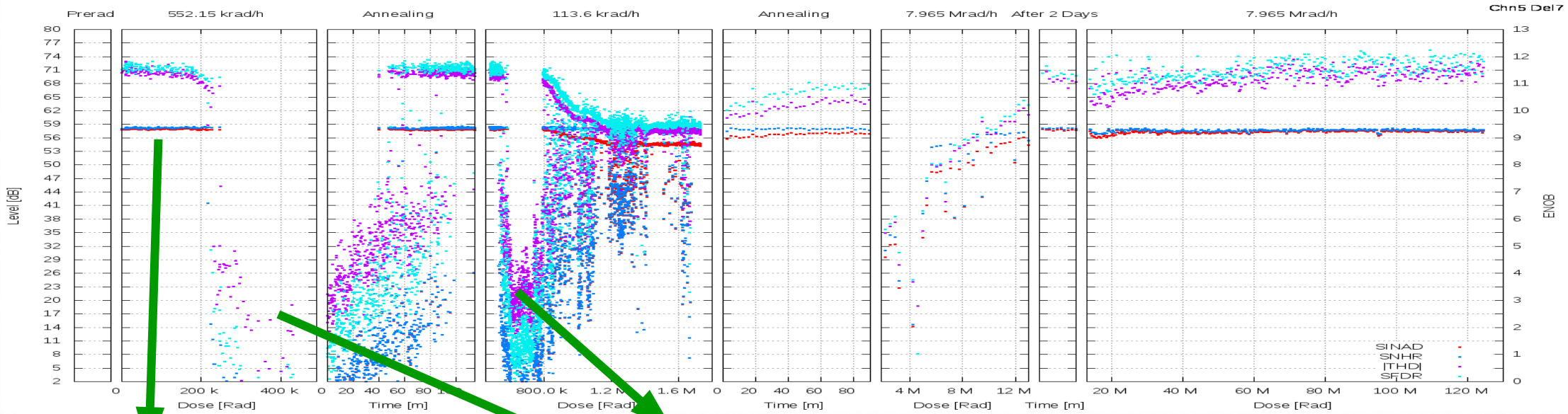
Performance recovered after ~hour of annealing

Gap in ADC operation between 500 and 800 krad

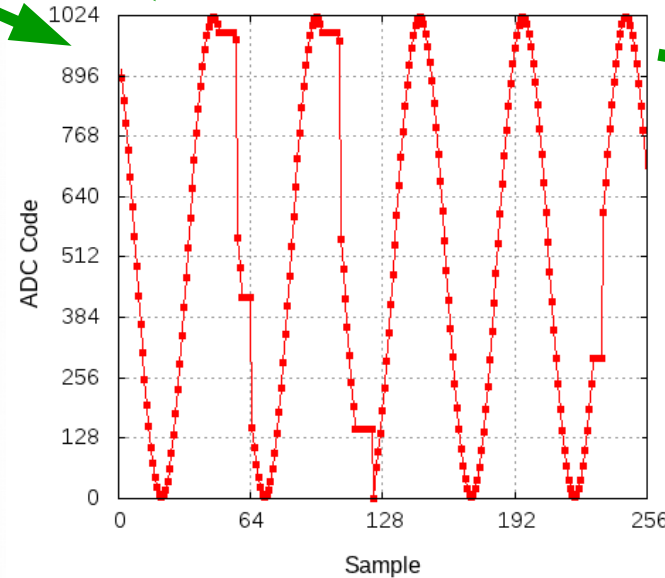
Performance recovered after ~hour of annealing

Large resolution degradation for doses in range 2 - 12 Mrad

No visible degradation up to ~120 Mrad



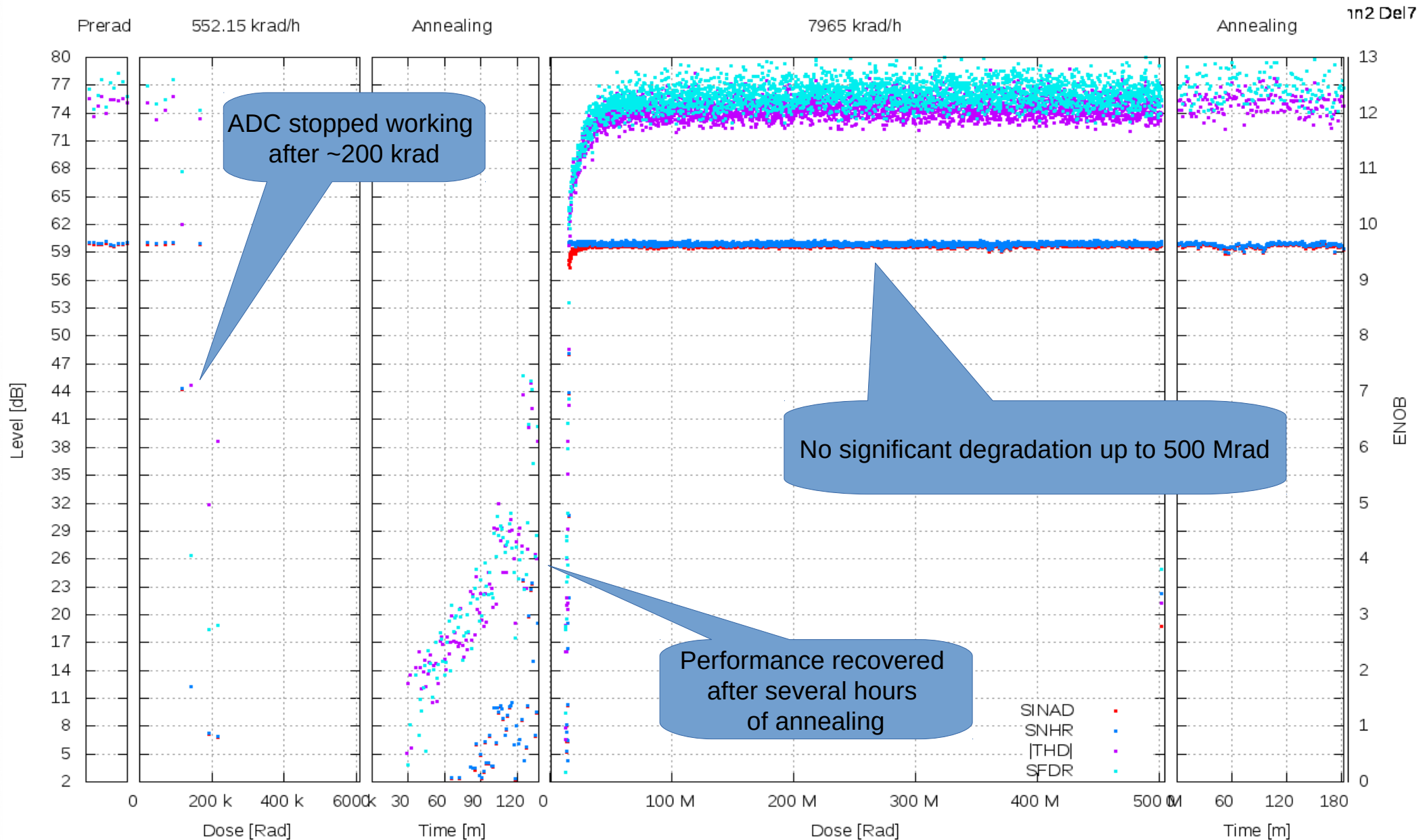
Good resolution → pure sine wave seen in data



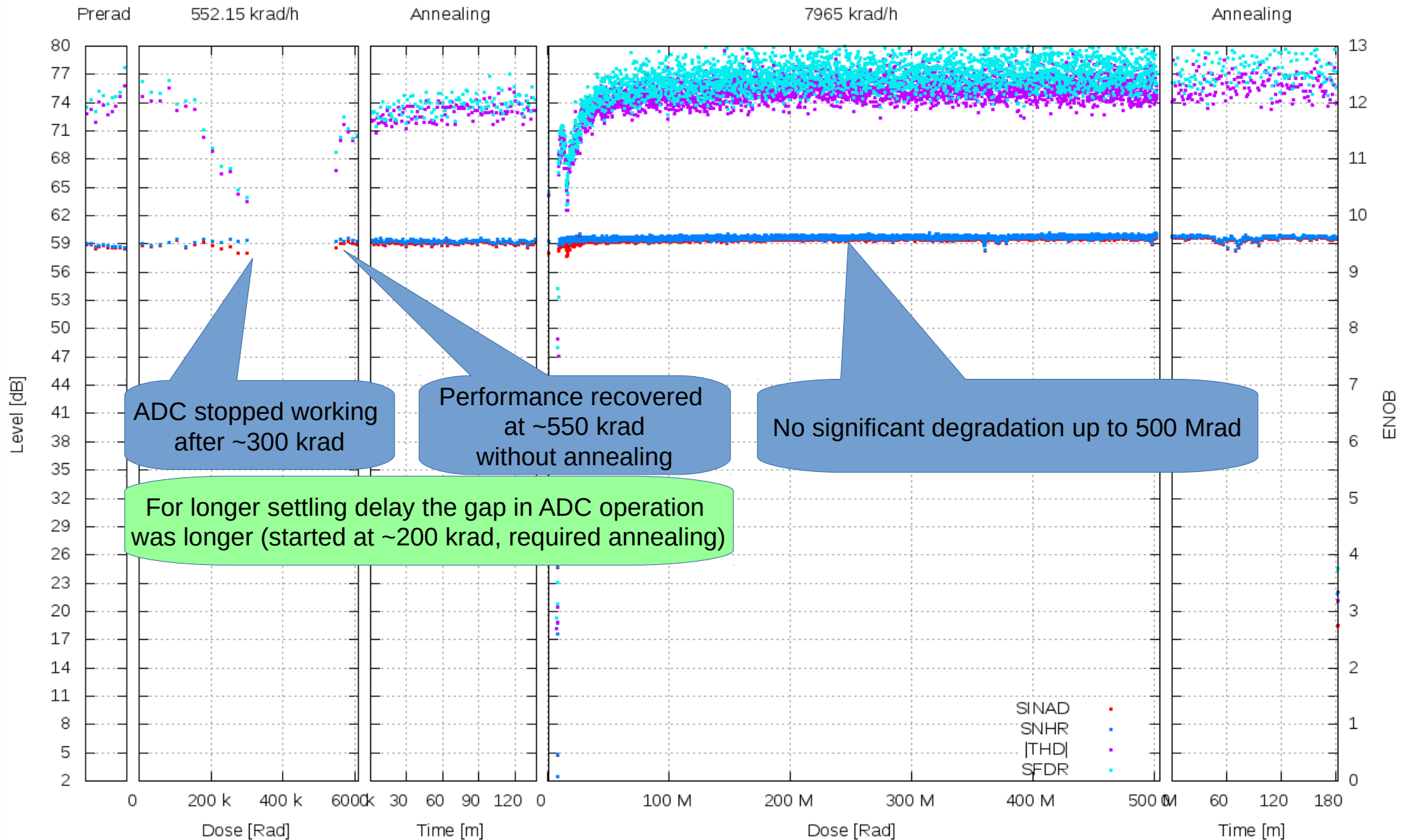
Sine distorted → degraded resolution:

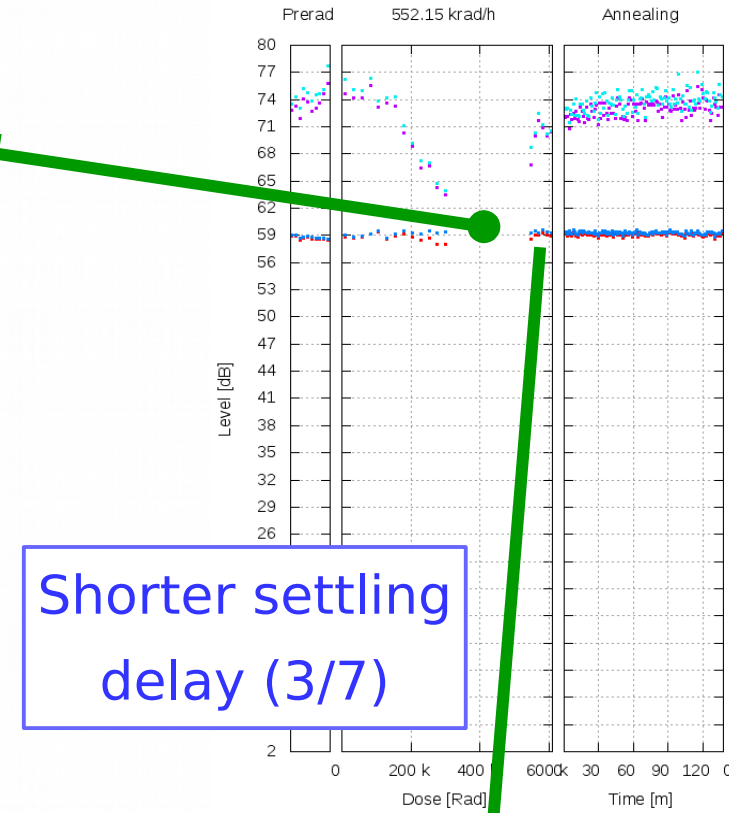
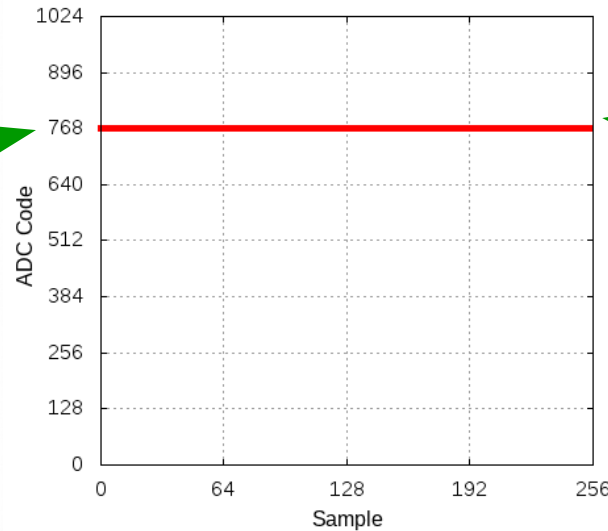
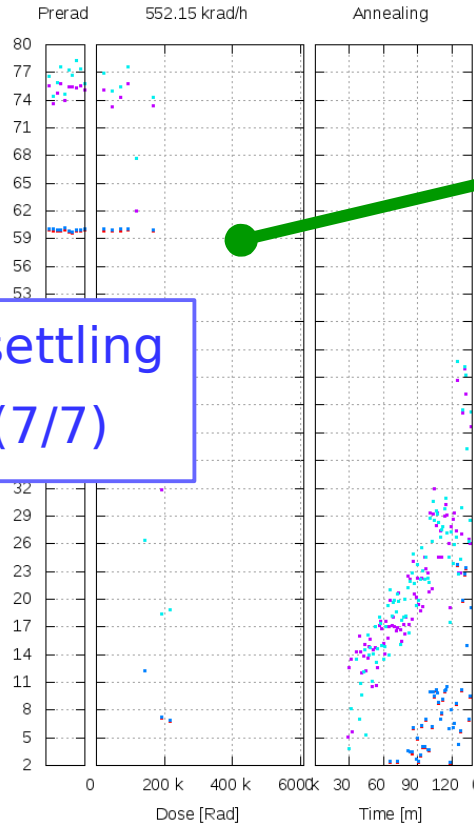
- Sometimes the same code is repeated few times
- Possibly due to metastable states in logic
- Still ~90% of samples are correct (but not enough to keep the dynamic metrics)

Longest settling delay (7/7)



Shorter settling delay (3/7)



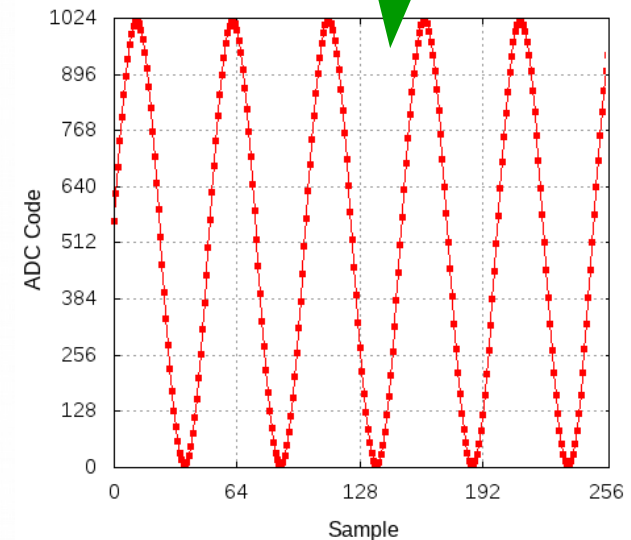


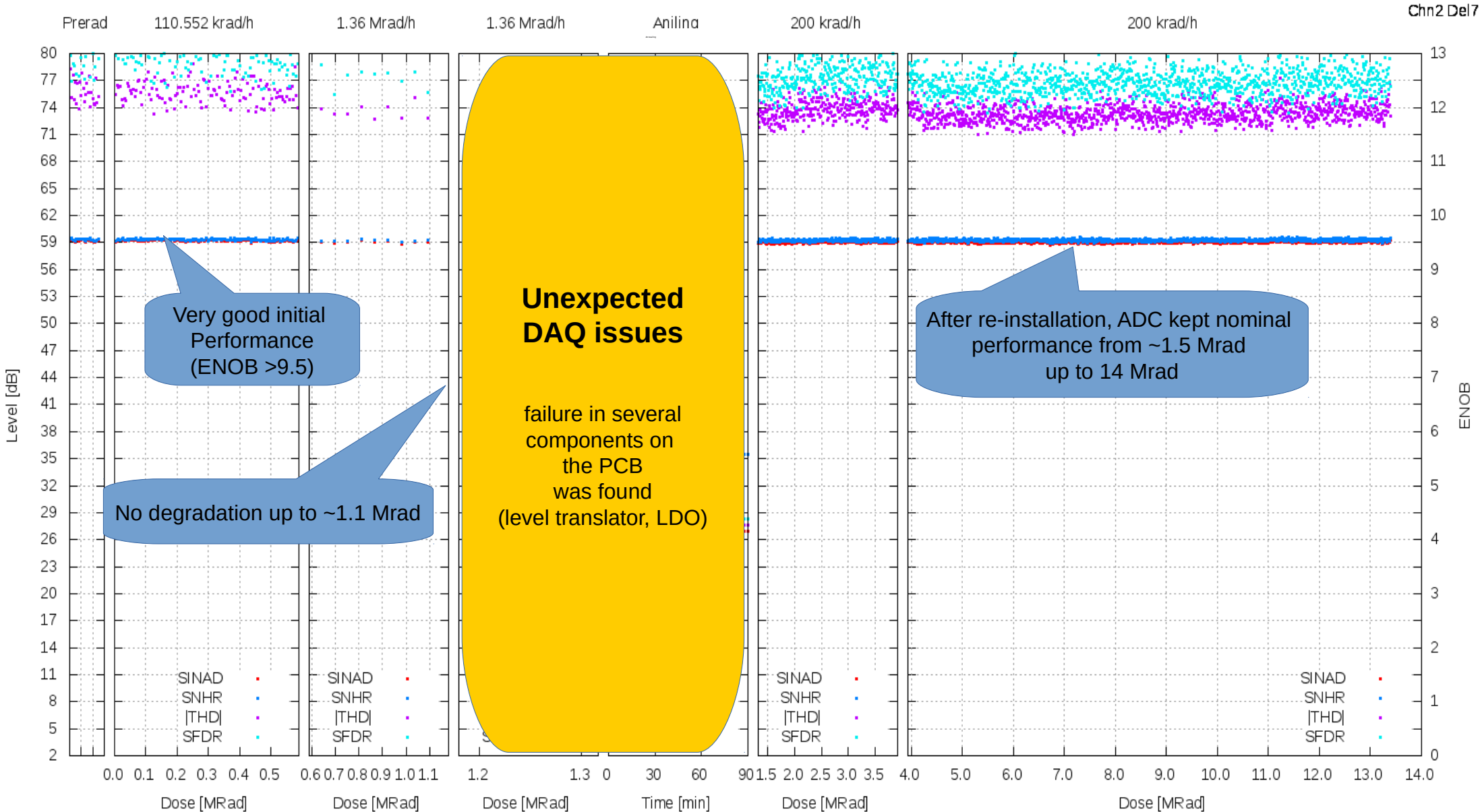
Longest settling delay (7/7)

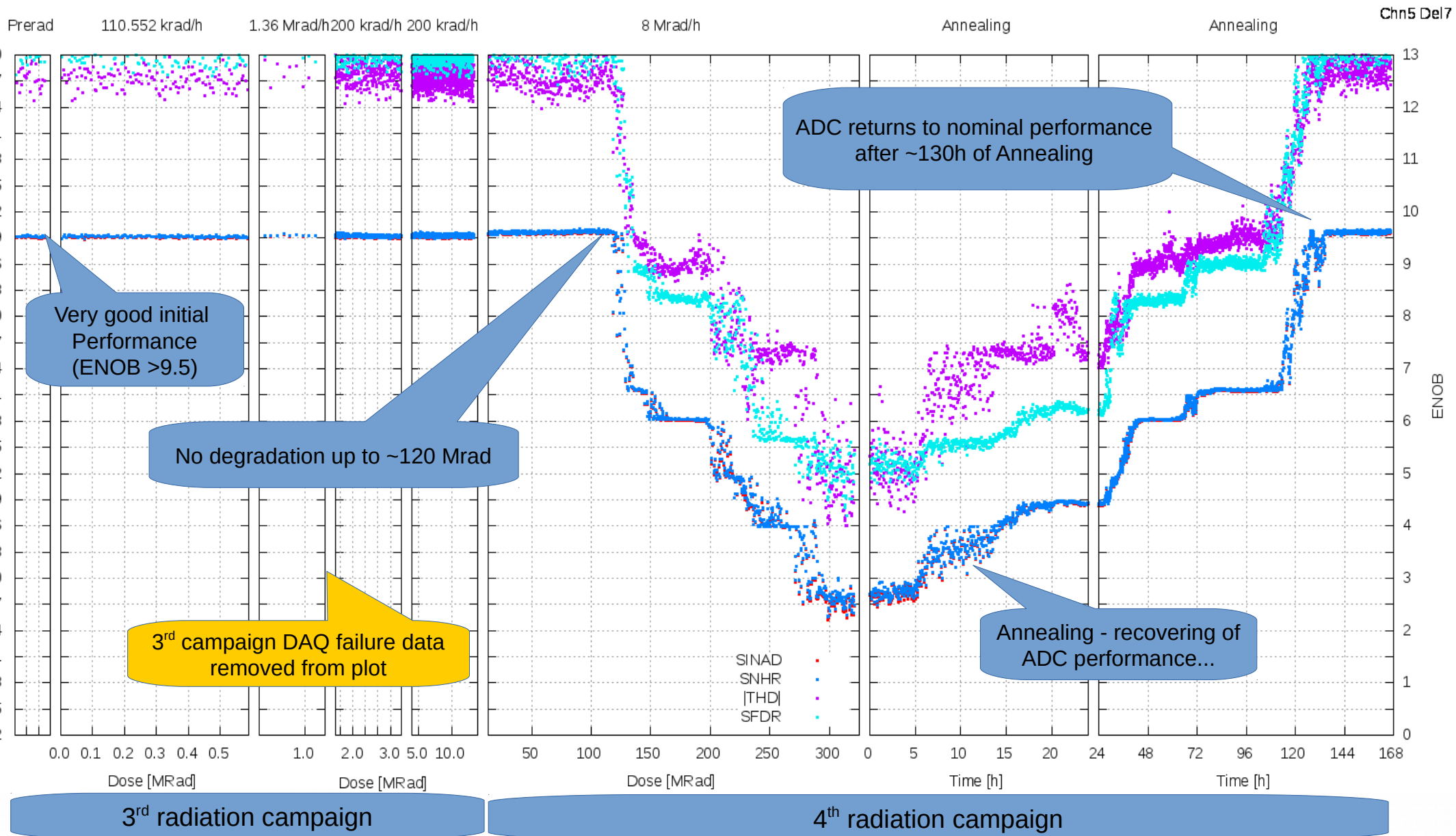
Shorter settling delay (3/7)

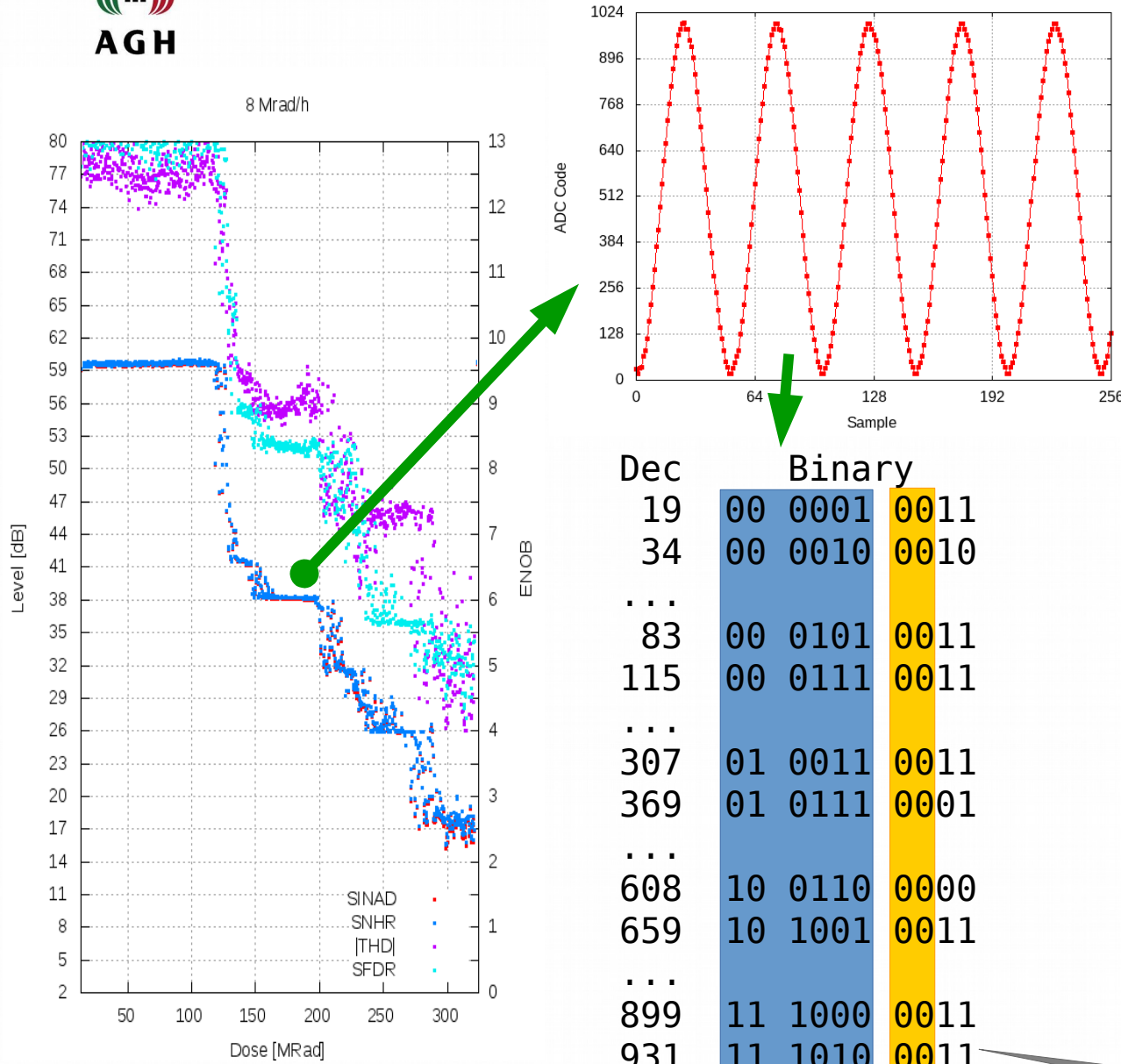
ADC stalled completely around 400 krad:

- Control logic slowed down so much that there was not enough time to finish the conversion before next sampling clock
- Shorter settling delay → shorted conversion → larger time margin → smaller range of doses for which ADC is stalled









Part of programmable resolution circuitry failed around 120 Mrad:

- Some bits of 10-bit result got masked, even if resolution was set to nominal (10 bits)
- For 120 - 150 Mrad one or two bits are masked for few consecutive samples
- For 150 - 200 Mrad 4th and 3rd bits are constantly masked
- Above 200 Mrad more and more bits are masked

Programmable resolution circuitry will be investigated and re-design or removed in next prototype

Only 6 significant bits working correctly

4th and 3rd bits are masked

Two remaining bits insignificant when higher bits are masked

- Three 8-channel ADC ASICs were fabricated and verified for high radiation doses, up to 500 Mrad
- ADC ASIC in process A worked correctly until highest received dose of 120 Mrad, although performance deterioration was observed in a short dose range below 1 Mrad
- ADC ASIC in process B, FAB14 worked correctly until highest received dose of 500 Mrad with performance deterioration in a short dose range around 400 krad
- ADC ASIC in process B, FAB6 worked correctly up to 120 Mrad without any deterioration
- In cases of deteriorated performance a short (from few hours to few days) room temperature annealing was always enough to recover the nominal performance

Thank you for attention