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Developement of ultra-low power, rad-hard SAR ADCs in 130 nm CMOS technologies

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The design and measurement results of two rad-hard, ultra-low power 10-bit SAR ADCs, fabricated in two CMOS 130 nm technologies, are presented. Both prototypes are fully functional achieving, in process A excellent linearity (INL, DNL < 0.3 LSB) and ENOB above 9.5 for sampling rate up to 50 MSps, and in process B a very good linearity (INL, DNL around 0.5 LSB) and ENOB around 9.2 with sampling rate up to 40 MSps. The power consumption at 40 MSps is, respectively, below 700 uW and 900 uW. The prototypes maintain their good performance for the doses up to 500 MRad.

Summary

In modern and future detectors of particle physics experiments an ultra-low power rad-hard area-efficient Analog-to-Digital Converter (ADC) is highly demanded. This work discusses the development of 10-bit Successive Approximation Register (SAR) ADCs meeting the above mentioned requirements and adapted to multichannel implementation in readout systems.

A fully differential ADC architecture was chosen, comprising a pair of bootstrapped switches, a differential Digital-to-Analog Converter (DAC), a dynamic comparator, and an asynchronous dynamic control logic. A fully dynamic architecture allows to remove the static power consumption while asynchronous logic eliminates a fast bit-cycling clock distribution. The selected Merge Capacitor Switching (MCS) scheme results in 93\% switching energy reduction in comparison to conventional scheme. The minimum allowable capacitor in given technology was used as the DAC unit capacitance, moreover a split DAC architecture was applied to reduce total capacitance. The prototypes were fabricated in two CMOS 130 nm technologies. In process A, an improved control logic implementation was used, resulting in increased meta-stability hardness and maximum sampling rate above 50 MSps. Also the layout of differential DAC was refined in comparison to process B, providing the linearity improvement. The ADC layout occupies 100 um x 800 um in process A and 146 um x 600 um in process B.

The prototype in process A achieves excellent performance with DNL and INL linearity errors below 0.3 LSB and effective resolution ENOB around 9.7 for 0.2 of Nyquist input frequency and above 9.5 for the Nyquist frequency at sampling rates up to the 50 MSps. A very good prototype performance is obtained in process B, with INL and DNL around 0.5 LSB and ENOB around 9.2 for 0.2 of Nyquist frequency at sampling rates up to 40 MSps, and around 9.0 at Nyquist frequency for rates up to 35 MSps. Power consumption is below 700 uW for process A and below 900 uW for process B at 40 MSps. For the first one, it gives an excellent FOM of around 23.5 fJ/conversion-step. For process A prototypes from two different foundries (12 inch and 8 inch wafer) were measured, giving similar results.

The prototypes were irradiated with high intensity X-ray tube up to the doses of around 500 MRad. For process B prototype degradation of resolution was observed for the dose of 400 kRad, which was restored after short annealing. A similar behavior, for the dose of 1 MRad, was observed for process A, 12 inch foundry prototype. After that both prototypes remained fully operational and maintained good resolution up to the maximal dose. For the 8 inch foundry prototype no deterioration for low doses was observed, however for this prototype the effective resolution rapidly dropped for the doses above 200 MRad. Nevertheless, also in this case the nominal performance was restored after 96 hours of annealing.

A fast ultra-low power 10-bit SAR ADCs were designed and fabricated. Measurements show a very good radiation hardness up to 500 MRad. Process A prototype shows one of the best FOMs obtained in 130 nm CMOS for similar specifications.

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