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Characterization of the first prototype of the Silicon Strip readout ASIC (SSA) for the CMS Outer Tracker Phase II upgrade

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The Silicon-Strip readout ASIC (SSA) for the pixel-strip module of the Phase II upgrades of the CMS Outer Tracker detector has been prototyped in a 65nm CMOS technology employing radiation tolerant design techniques. The SSA provides real-time primitives for the on-detector particle momentum discrimination and for the readout of the complete triggered events. This contribution will present the test results and the performance evaluation data from the first SSA prototype as well as radiation tolerance characterization results.

Summary

The High Luminosity CMS Outer Tracker upgrade requires to drastically reduce the transmission bandwidth and to keep the Level-1 (L1) trigger rate at an acceptable level (< 1MHz) in the high pileup conditions of the HL-LHC. For this reason, the Outer Tracker detector modules introduce the capability to perform on-detector fast recognition of interesting events by locally rejecting low transverse momentum particles and transmit encoded information of high momentum particles to the L1 trigger decision electronics. To facilitate the on-detector particle momentum discrimination, the Outer Tracker Pixel-Strip (PS) modules adopt a double layer sensor architecture which combines a pixel silicon sensor with a strip silicon sensor.

The SSA is the 120-channel, Silicon Strip readout ASIC of the Outer Tracker PS-Module. It generates, in real time, the hit cluster coordinates necessary for the correlation with hit clusters from the pixel layer. It also stores full events in an embedded radiation-tolerant memory for a latency period of 12.8 us. Full events are transmitted up to a maximum average trigger rate of 1MHz. The SSA has been prototyped for the first time on a 65nm CMOS technology incorporating all the required functionalities and performance characteristics for operation in the final readout system. Radiation Tolerant design techniques were employed to mitigate Single Event Effects as well as Total Ionizing Dose effects for operation in the radiation environment of the HL-LHC CMS Outer Tracker.

The fabricated prototype was tested successfully and characterized utilizing a custom made test bench consisting of an FC7 uTCA FPGA card followed by an interface board and the specially adapted firmware and software based on the D19C CMS DAQ framework. The digital functionality has been verified under different working temperatures and radiation levels up to 200Mrad. Measurements shows a configurable front-end gain between 35 and 54 mV/fC and an average noise of ˜300 e-, matching the demanding requirements of noise performance. The measured peaking time for an injected charge between 0.5 fC and 8 fC is 15ns allowing, in combination with the zero dead-cycle binary readout, to detect consecutive particle events. The embedded trimming circuit allows to obtain a measured threshold spread of less than 25aC between channels. The measured power consumption is ˜55mW, well within the strict power budget of the PS modules.

This contribution will present the custom made test bench system as well as the performance characterization results and radiation tolerance test results of the first SSA silicon prototypes.

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