Contribution ID: **126** Type: **Oral**

FLAME - A readout ASIC for a luminosity calorimeter at a future linear collider

Wednesday 19 September 2018 14:25 (25 minutes)

The design and measurement results of a prototype readout ASIC for the luminosity calorimeter at future linear collider are presented. The proof-of-concept ASIC, comprising 8 channels with a variable gain front-end, a differential shaper and a 10-bit SAR ADC in each channel, was fabricated in CMOS 130˜nm technology. The prototype is fully functional, achieving good linearity in a wide input charge range with a SNR for MIP signals of about 25 in the high gain mode. The ASIC consumes about 1.5˜mW/channel. The design of a full, 32-channel SoC type FLAME, currently under development, will also be covered in this contribution.

Summary

For a future linear collider, CLIC or ILC, a dedicated sandwich type calorimeter, LumiCal, is foreseen for the luminosity measurements. The LumiCal will comprise 30 or 40 layers of segmented silicon sensors, with above 90˜000 channels per detector. A 32-channels dedicated SoC type readout ASIC, FLAME, is being currently developed in CMOS 130˜nm technology. Each readout channel is composed of analogue front-end with multiple gain modes, a differential CR-RC shaper and a 10-bit SAR ADC. The ADC output data are encapsulated, coded with 8b/10b scheme, serialized with multi-phase PLL and sent out by two fast 5.2˜Gbps serial links with SST drivers to Xilinx FPGA gigabit receivers. The design, sent recently for fabrication, is based on the proof-of-concept 8-channel ASIC with simplified digital readout, FLAME_v0, whose measurement results are discusses in this work alongside the design of the complete FLAME.

For the LumiCal, the charge deposition per pad varies from few˜fC for MIPs up to few˜pC at the maximum of electromagnetic shower for 500˜GeV primary electrons. To cover the wide input charge range, the front-end with four gain modes, followed by a pole-zero cancellation circuit, a CR-RC shaper with 50˜ns peaking time and a fast 10-bit SAR ADC was designed. Since a fully differential architecture was chosen for the ADC, also the shaper circuitry was designed fully differential in order to avoid additional conversion of a single-ended signal. The shaper output is continuously sampled by the ADC with the nominal rate of 20˜MSps, however the rates up to 50˜MSps can be also obtained. The channel layout occupies 100˜um˜x˜1200˜um. In the FLAME_v0 the output data are partially serialized into eight links, one per each channel, allowing the multichannel operation.

The FLAME_v0 prototype is fully functional and achieves good linearity for input charge range up to 40˜fC in the highest gain, 100˜fC and 150˜fC in moderate gains and up to 2˜pC in the lowest gain. The ENC calculated from ADC samples in the highest gain mode varies from 900˜electrons at 5˜pF detector capacitance to below 2000˜electrons at 50˜pF, allowing to obtain the SNR for MIP in range 10–30 for different detector capacitance. The pedestal spread, without trimming, remains below 16˜LSB in the highest gain mode and around 5˜LSB in the remaining modes. No measurable crosstalk was observed in multichannel operation. The power consumption of analogue part is below 1.2˜mW per channel, while the ADC consumes only 350˜uW at 20˜MSps and 700˜uW at 40˜MSps. The performance of the FLAME_v0 prototype proved the concept of the front-end comprising a fast 10-bit ADC in each channel.

Based on the measurement results of the FLAME_v0 prototype a complete SoC type FLAME ASIC was designed.
In the final FLAME the preamplifier and shaper output voltage ranges were significantly improved, allowing to obtain enhanced input charge range in only two gain modes. To cover the pedestal spread trimming DACs

were added in each channel. Also the internal biasing circuitry was added to the ASIC. The improved channel layout occupies 80˜um˜x˜2300˜um.

Authors: MORON, Jakub (AGH University of Science and Technology (PL)); MURDZEK, Jan Karol (AGH University of Science and Technology (PL)); SWIENTEK, Krzysztof Piotr (AGH University of Science and Technology (PL)); IDZIK, Marek (AGH University of Science and Technology (PL)); FIRLEJ, Miroslaw (AGH University of Science and Technology (PL)); Dr FIUTOWSKI, Tomasz Andrzej (AGH University of Science and Technology (PL))

Presenter: IDZIK, Marek (AGH University of Science and Technology (PL))

Session Classification: ASIC

Track Classification: ASIC