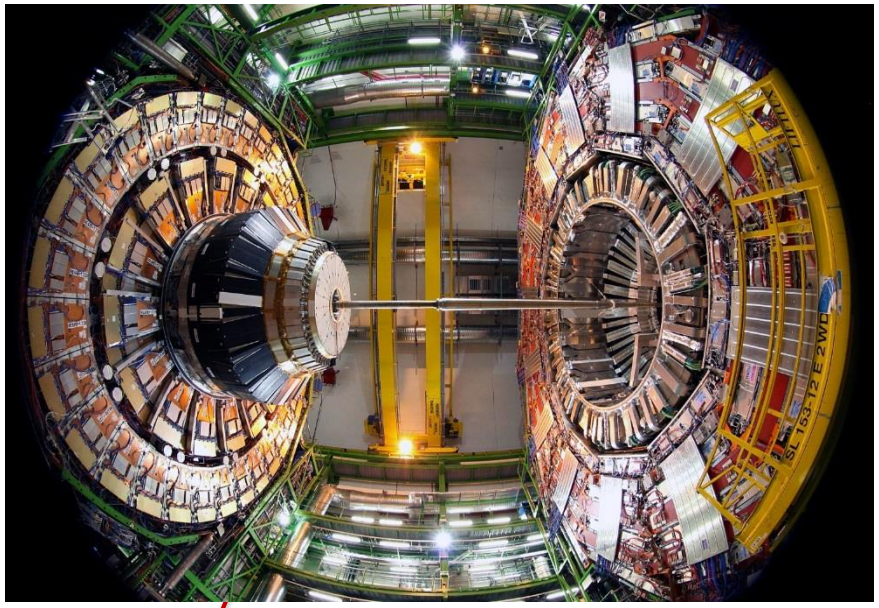
HGCROC-V1 test results

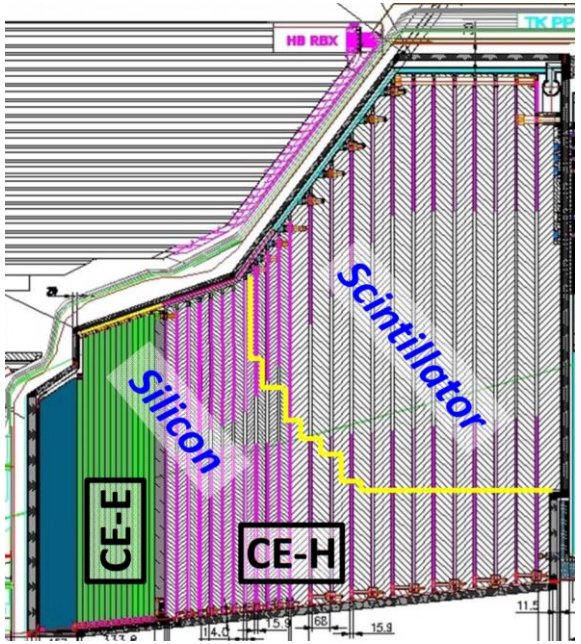
C. De La Taille on behalf of CMS HGCAL

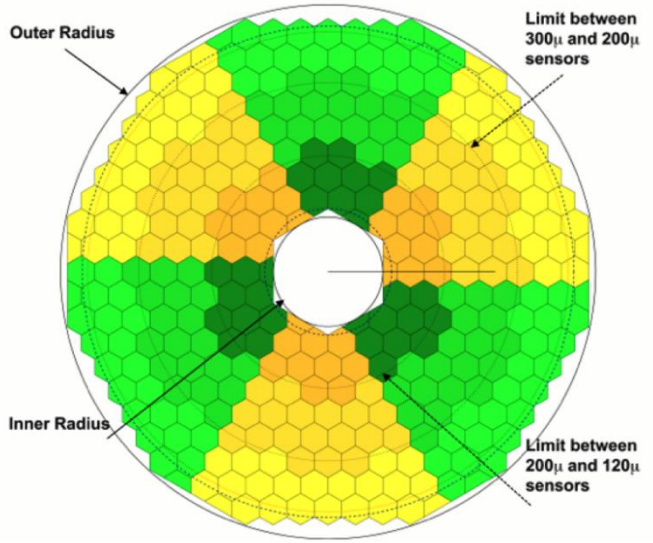
TWEPP 2018

Organization for Micro-Electronics desiGn and Applications

HGCAL: CMS EndCap Calorimeters for the LHC Phase-II upgrade



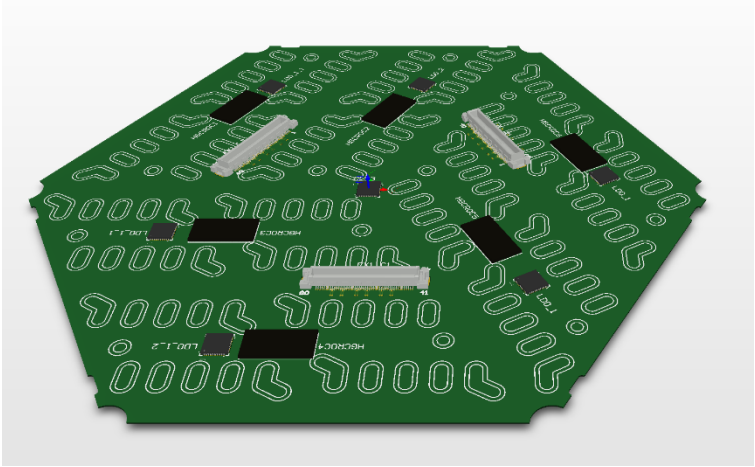


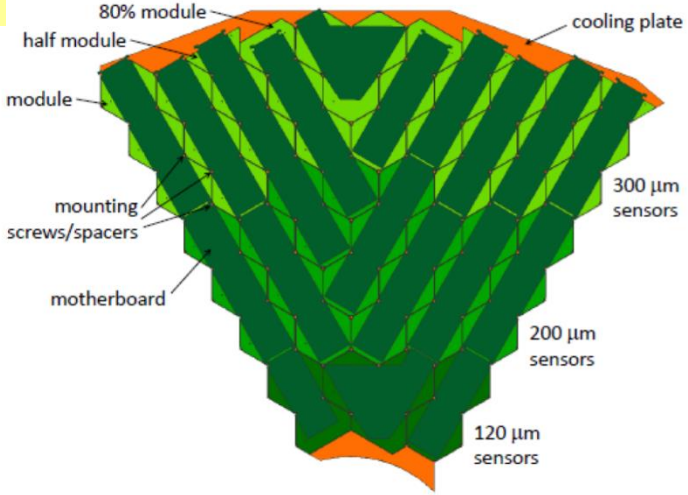


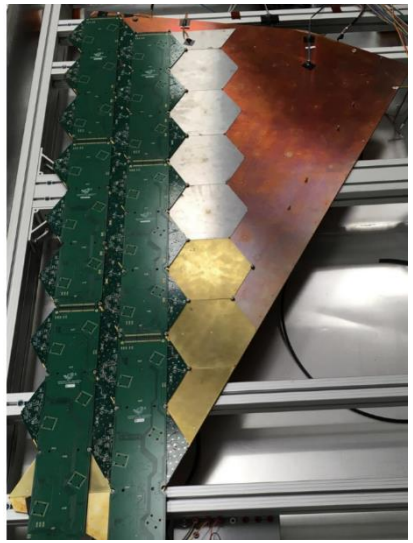
New Endcap Calorimeters

- Rad. tolerant
- High Granularity: increased transverse and longitudinal segmentation, needed to mitigate pileup effects to select events with a hard scatter process at L1-Trigger and to identify the associated vertex and particles
- precise timing capability: further mitigation of pileup effects

See talk from Dave Barney TWEPP18 tuesday

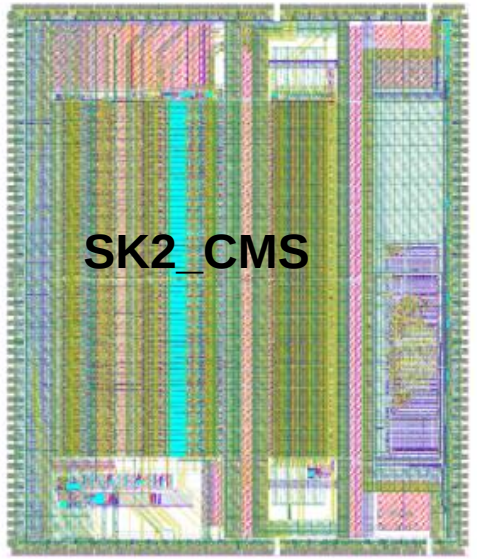


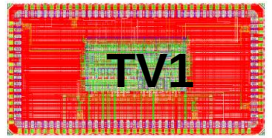


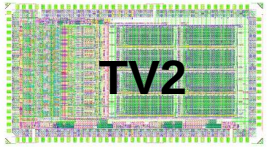


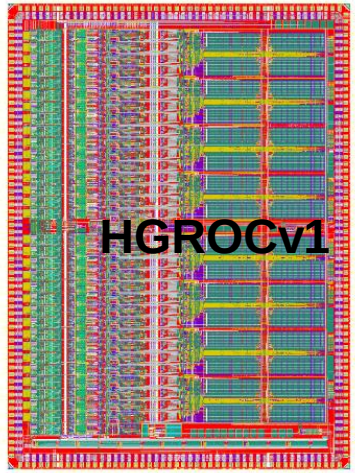
Development history

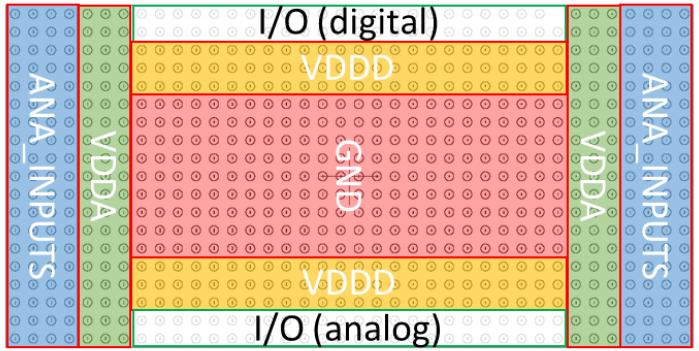
- Jan 16 : **SKIROC2_CMS** [TWEPP 2016]
  - SiGe 350 nm 7x9 mm²
  - Dedicated to test beam and analog architecture (TOT)
- May 16 : 1st test vehicle: **TV1**
  - CMOS 130 nm 2x1 mm²
  - Dedicated to preamplifier studies
- Dec 16 : 2nd test vehicle: **TV2** [TWEPP 2017]
  - CMOS 130 nm 4x2 mm²
  - Dedicated to technical proposal analog channel study
- **July 17 : HGCROCv1** [TWEPP 2018]
  - CMOS 130 nm 5x7 mm²
  - all analog and mixed blocks; large part of digital blocks
- Dec 18 : HGCROCDV1
  - CMOS 130 nm 15x6 mm²
  - Final size, packaging and I/Os







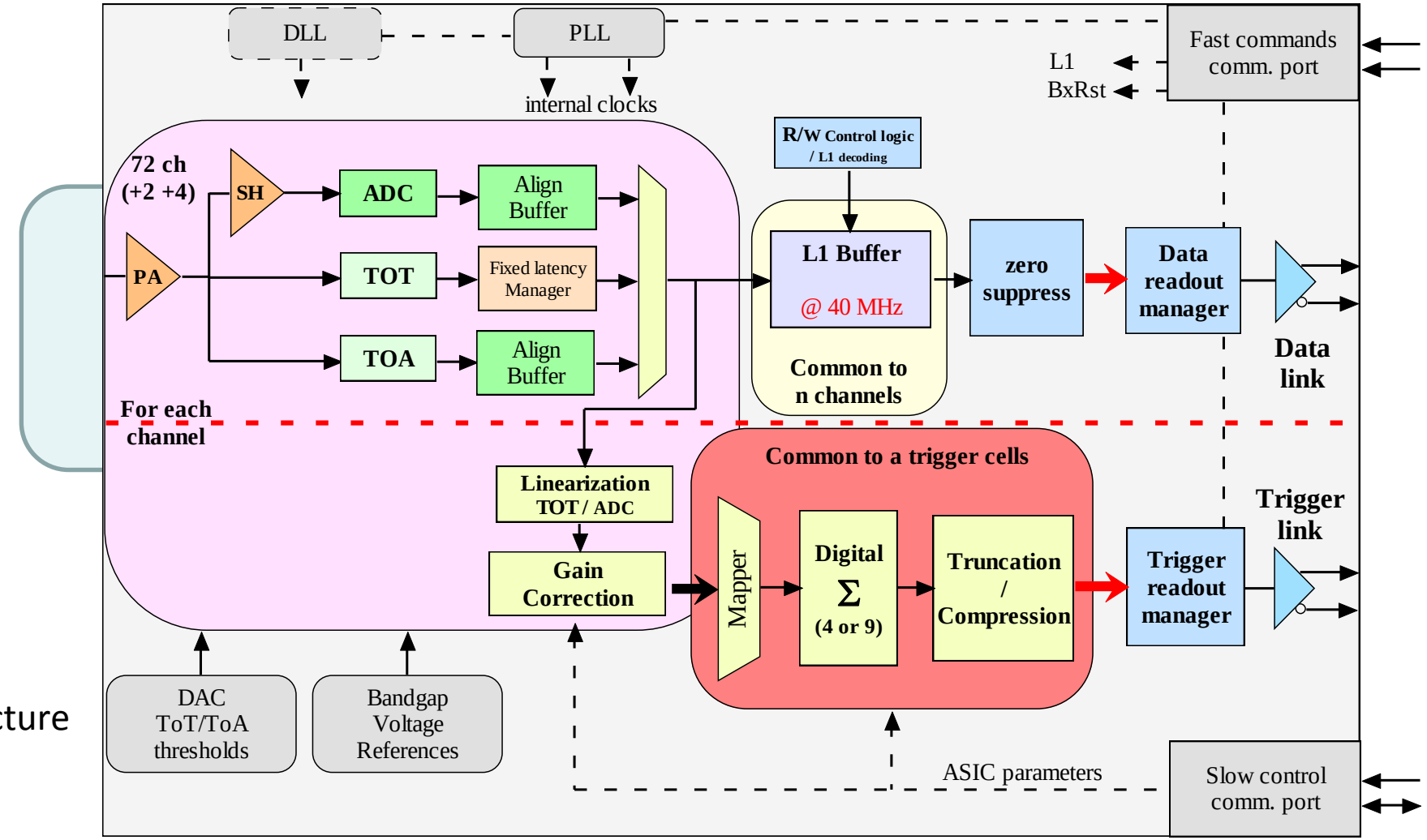




HGROCv1 overview

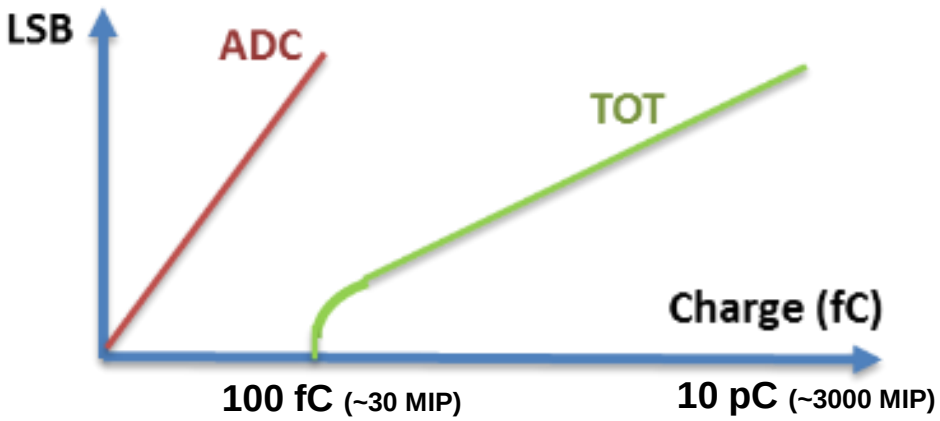
HGROCv1 features:

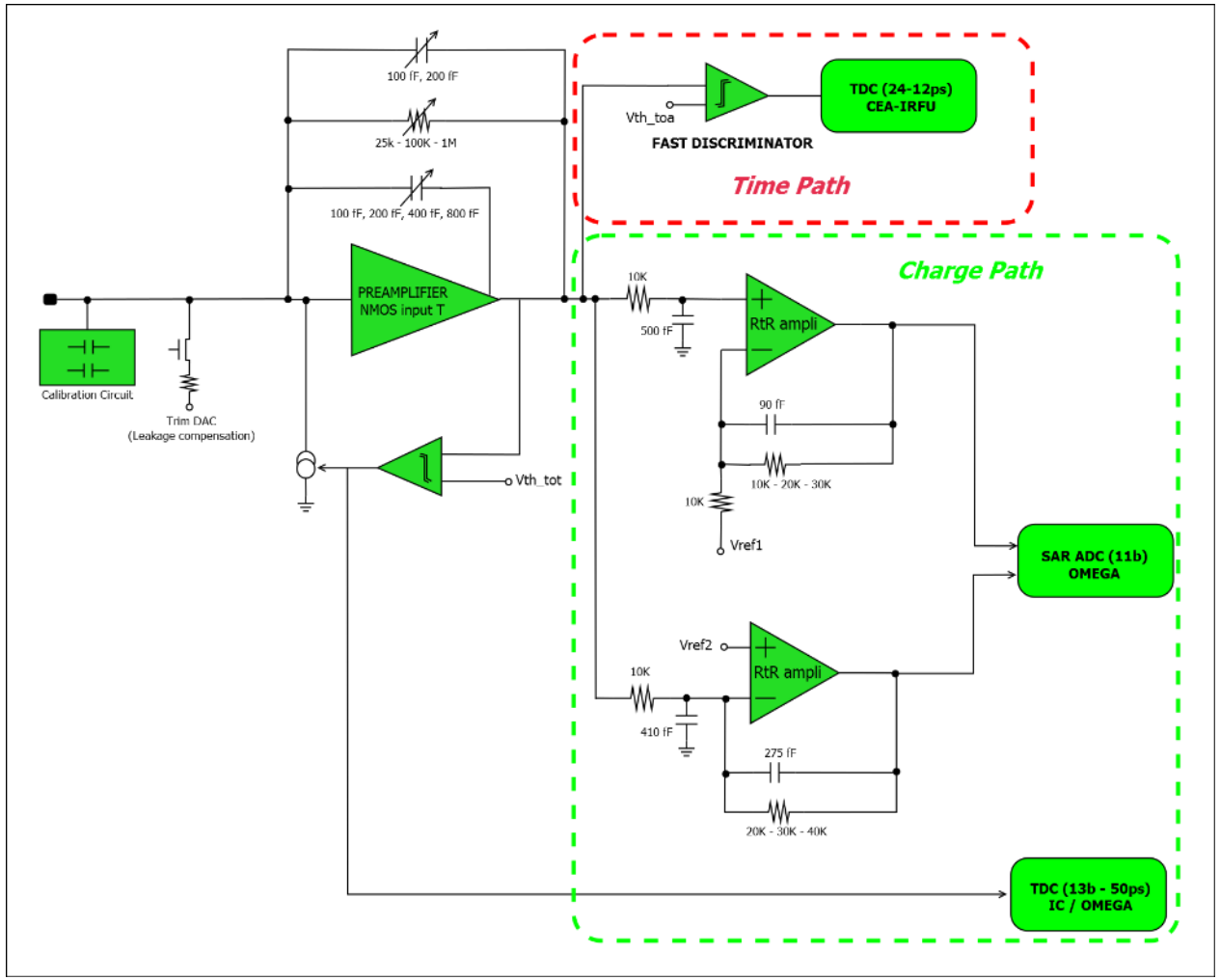
- 32 channels
- Dual polarity
- TOT with 2 variants:
  - Low power @ Imperial
  - DLL @ OMEGA (CERN based)
- TOA (CEA)
- 11-bit SAR ADC (OMEGA)
- Simplified Trigger path
  - Only sum by 4
  - No 0-suppress (4+4 log)
- SC with triple
- digital block with simplified architecture
- Bandgap from CERN [S. Michelis]
- PLL from CEA-IRFU
- 10b DAC from TV2



Analog channel

- Preamplifier gain adjustable on 4bit
- Simple CRRC shaper (assumed digital filtering)
- Decay time given by R_{f_pa} (25K or 100 k)
- New TOT architecture
  - Both polarities, Gain adjustable by slow control
- New TOA fast discriminator
- Local 5bit DAC to adjust the Vrefs and the thresholds
- Local input current DAC to compensate the leakage
- Internal calibration circuit
  - Low range up to 600 fC
  - High range up to 10 pC

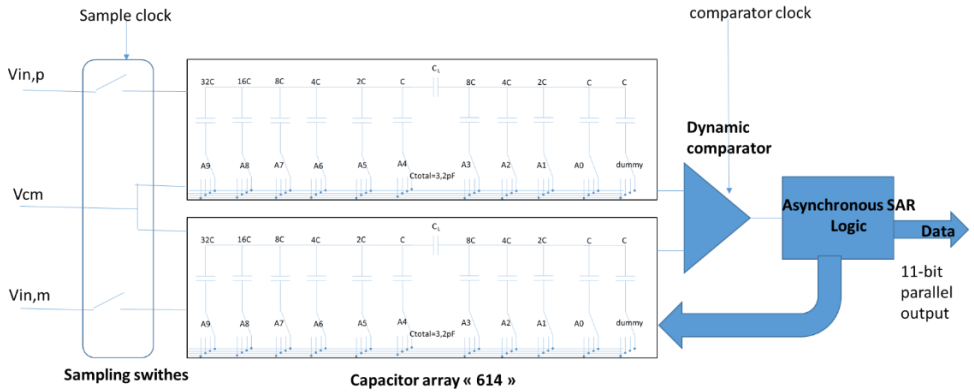


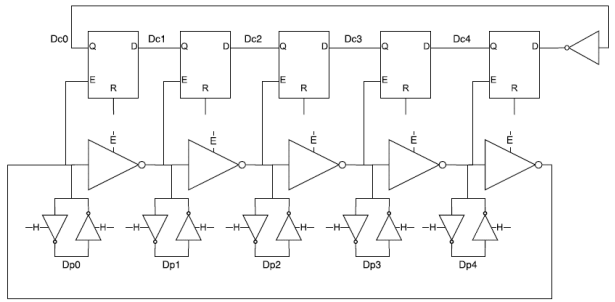


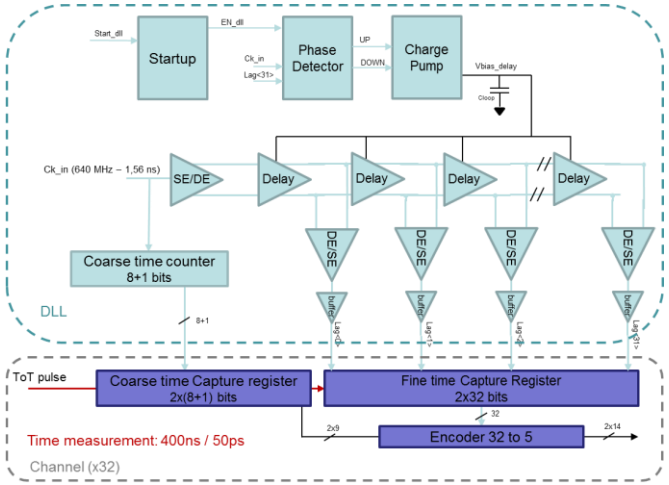
Power dissipation @ 1,5V supply
- Vdda (preamp): 1,6mA
- Vdd (tot): 160µA
- Vdd(shaper, toa): 1,1mA

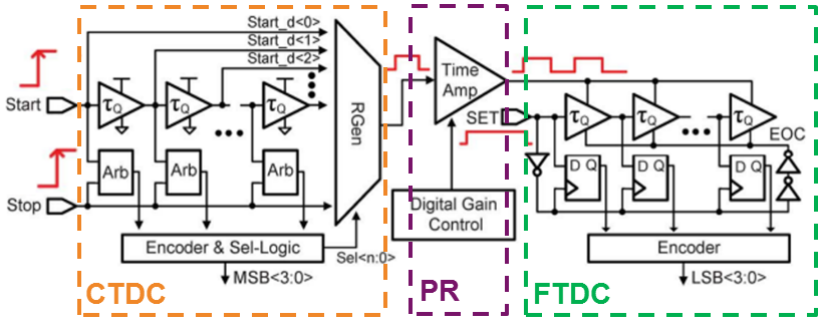
Mixed-signal circuits

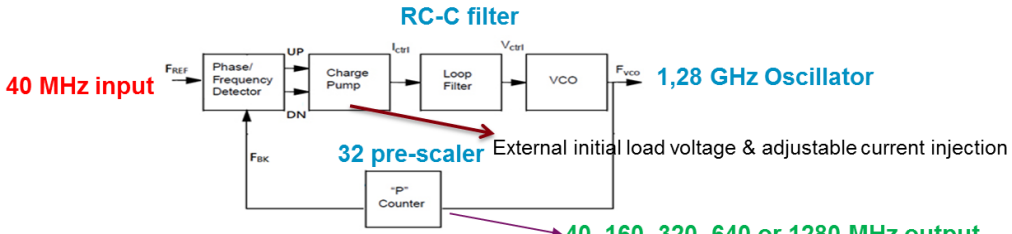
- ADC SAR 11bit 40 MHz
  - Inspired from Krakow design, 11 bit
- 2 TDCs for TOT
  - IC design, 50ps/200ns, based on a ring oscillator
  - OMEGA design, 50ps/400ns, based on a global DLL running at 640MHz
- TDC for TOA
  - CEA-IRFU design
  - 10/11 bit
- PLL
  - CEA-IRFU design
  - 40MHz input clock
  - 1,28GHz running frequency





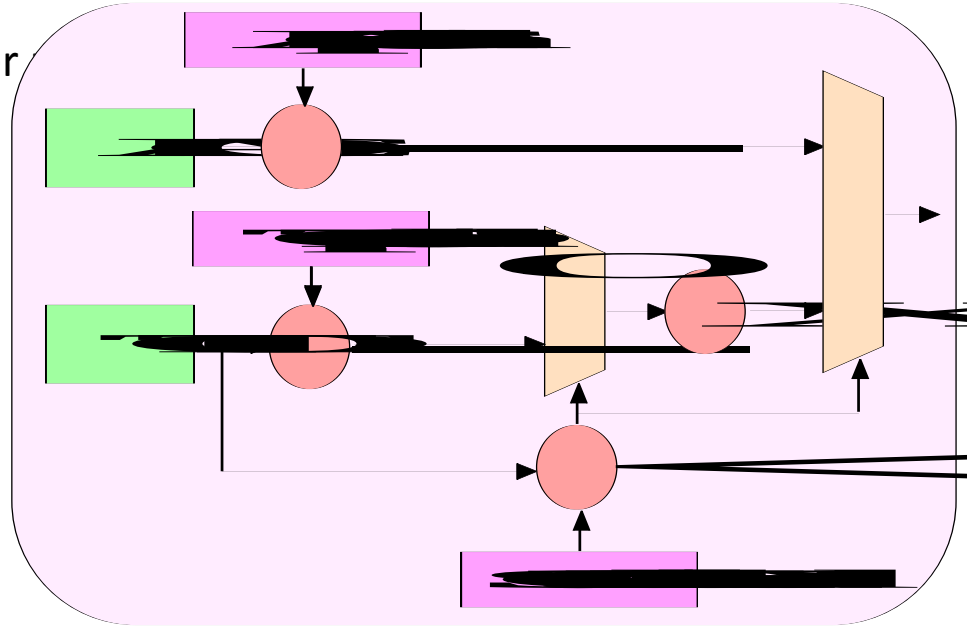


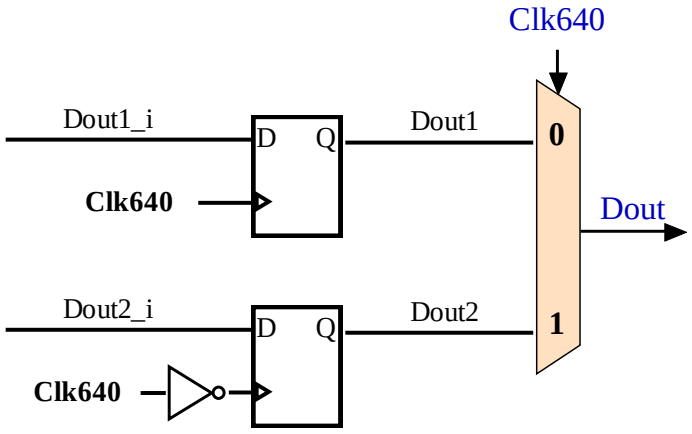




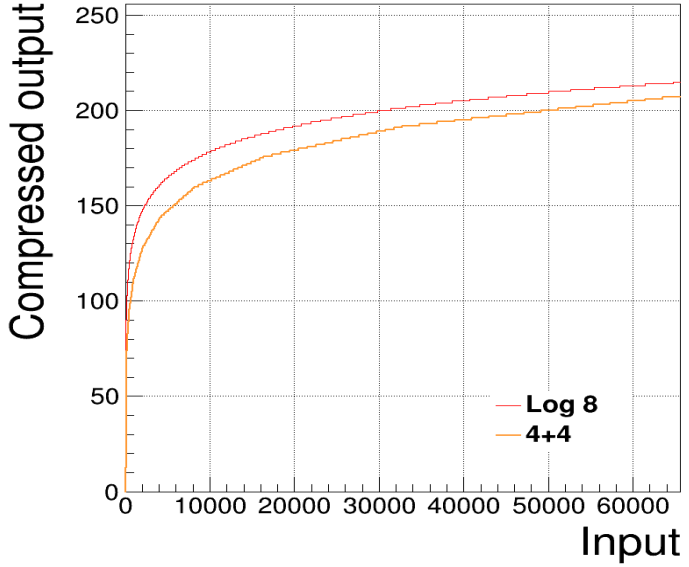
Serializer and Elink for trigger path

- The chip integrates 2 elink transmitters to handle the 64 bits from the trigger
  - 4 channels are encoded into 8 bits (with 4+4 encoding)
  - 2 variants (fully digital or mixed ➔ way the last mux is done)
  - Possibility to readout a known frame (set by SC)
  - Default is 1,28 Gb/s (640 Mb/s possible)
- Main specifications:
  - Data rate 1,28 Gb/s (internally 640M DDR)
  - Compatible with LpGBT protocol
  - Programmable Pre-emphasis (based on Paulo Moreira scheme)
  - Synchronization pattern on request (in place of trigger data)



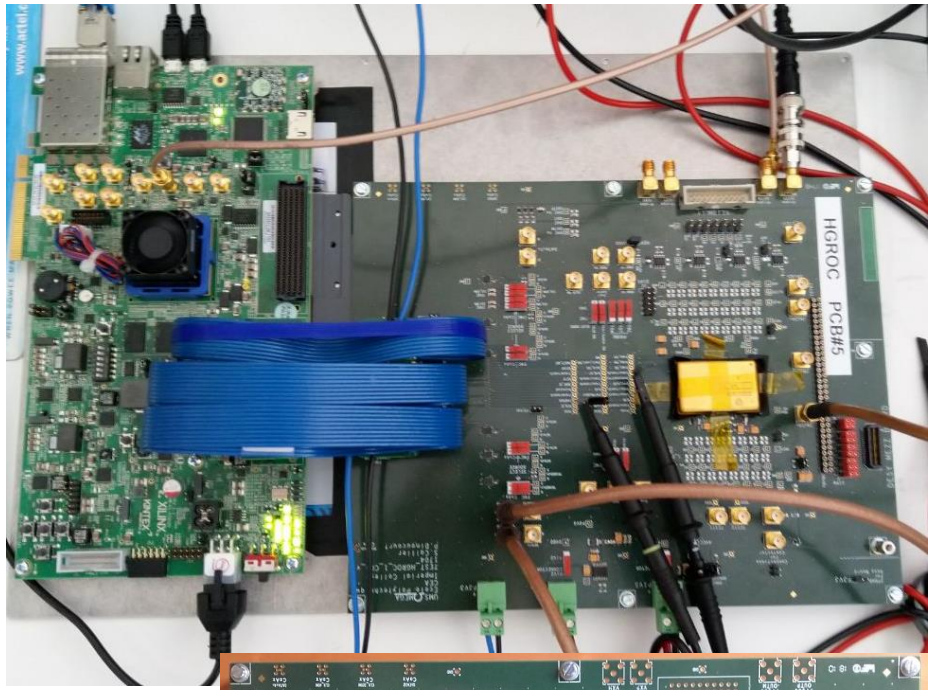


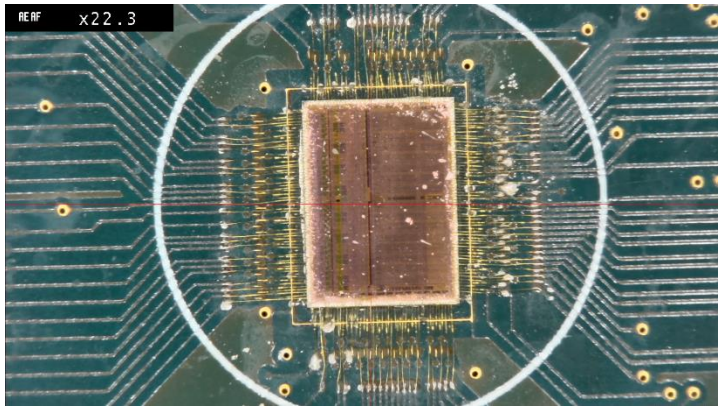
Specification description	Value
Vcm (common voltage)	0,6 V
Vdiff (differential voltage)	100 to 200 mV
Pre-emphasis current	0,5 to 4 mA
Termination load	100 Ω

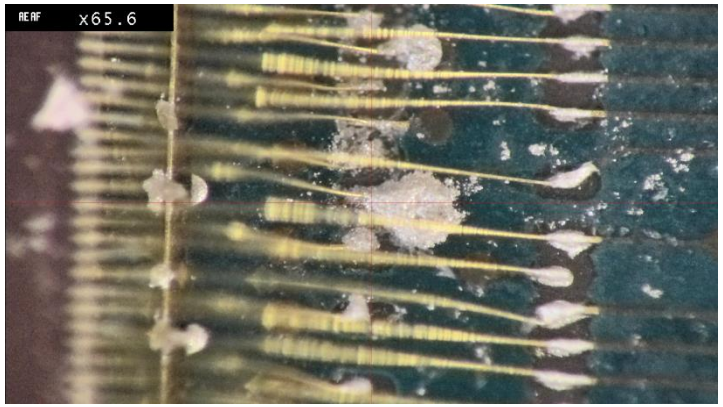


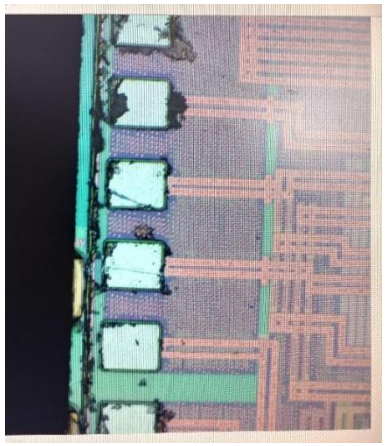
Test setup : PCB issues

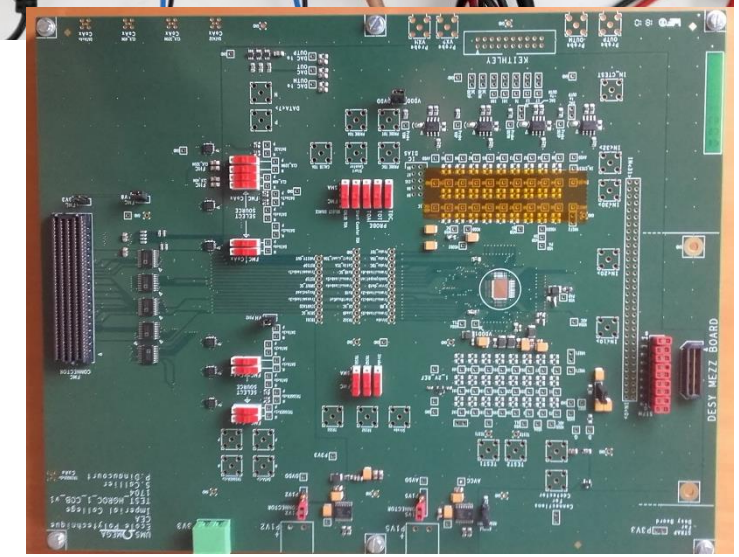
- Many issues during the dicing, cabling and bonding
- 3 boards over 5 are partially usable
- More boards redone and bonded at CERN & FNAL
- Tests done at LLR, CEA-IRFU, Imperial & Omega







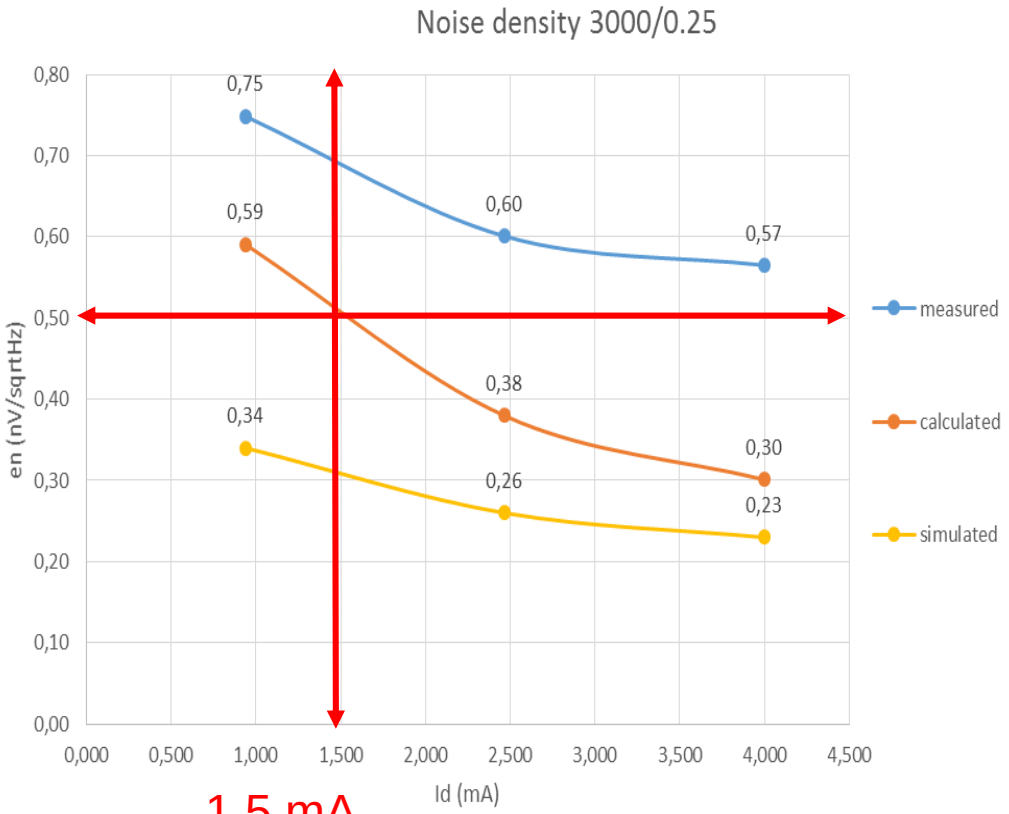




Preamp noise measurements (T=300K)

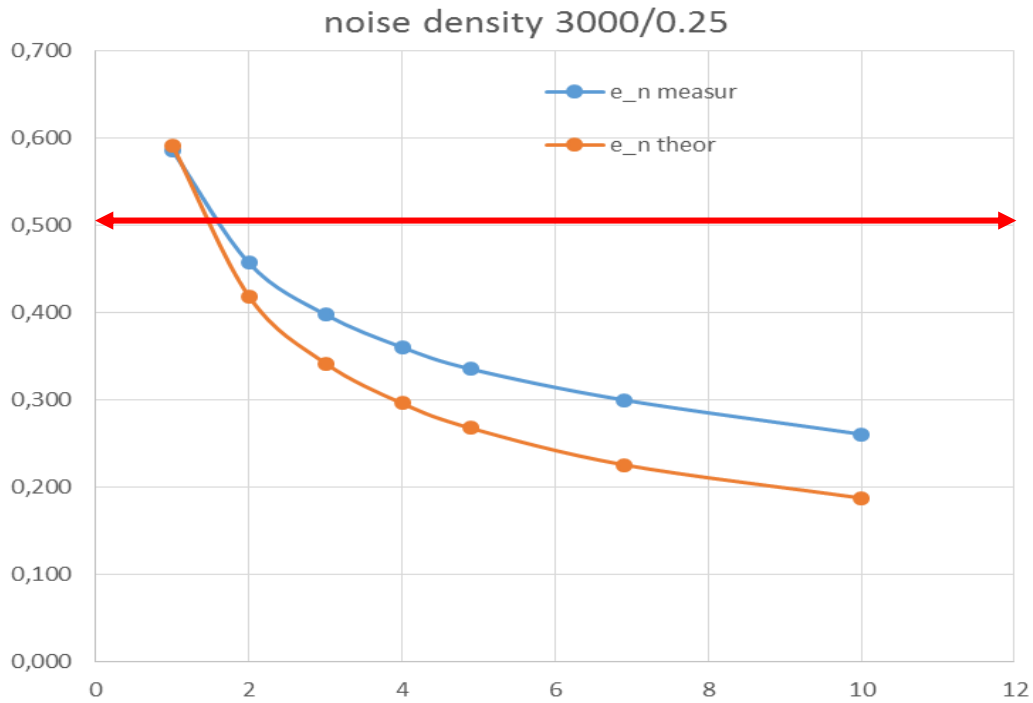
- Early noise measurements too high : simulation below theory and excessive noise
  - Simulations by Jan Kaplon [CERN] 3000/0.26 @ Id=1 mA
  - Theory predicts in weak inversion : gm = 24 mA/V en = 0.59 nV/√Hz
  - Simulations now use old Spice 2 model in strong inversion en = 0.68 nV/√Hz
- Excessive noise measured at large current : bulk noise
- New transistor layout comes close to theory (~ 2 Ω difference)

TSMC 130n	IBM 130n	TSMC 65n
0.35 nV/√Hz	0.67 nV/√Hz	0.75 nV/√Hz



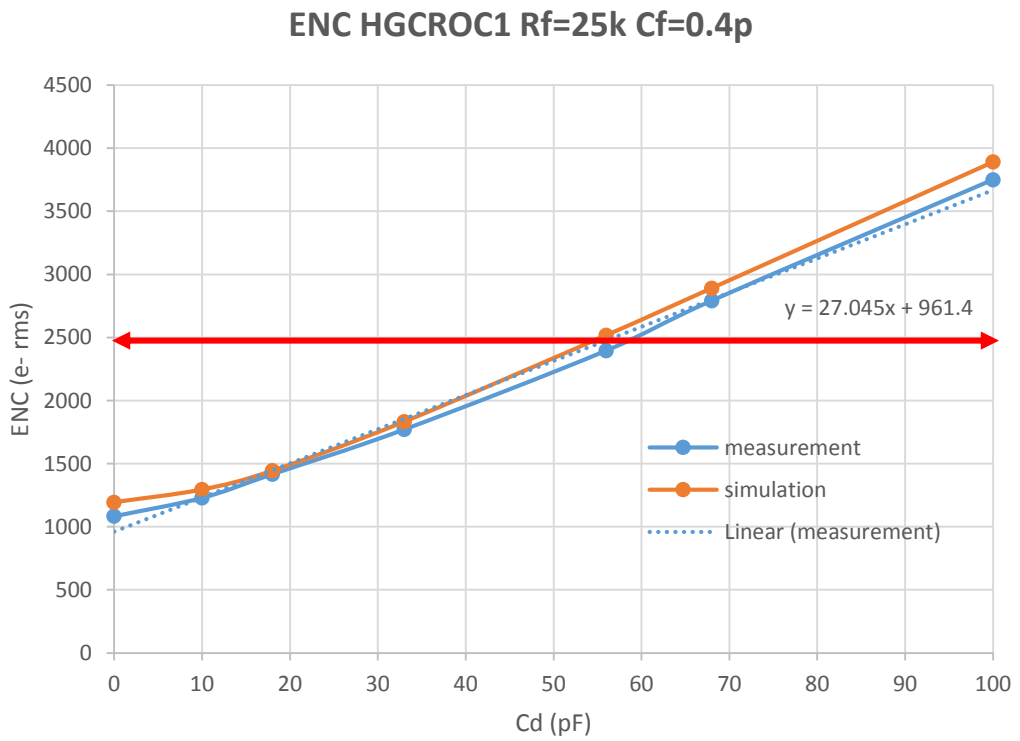
1.5 mA

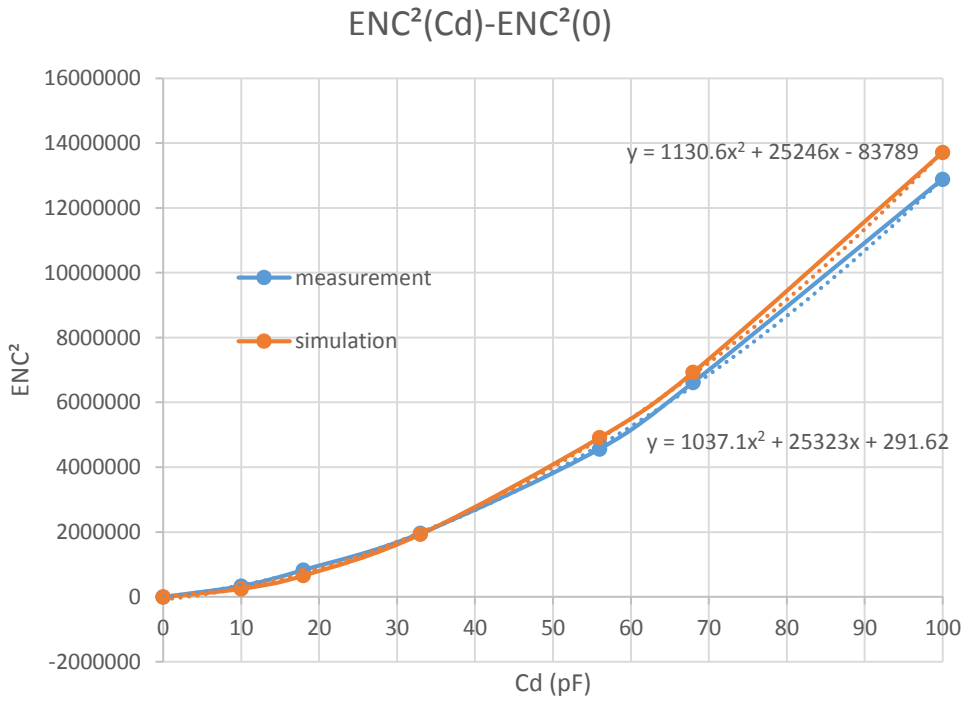
0.5 nV/√Hz



Preamp ENC measurements (T=300K)

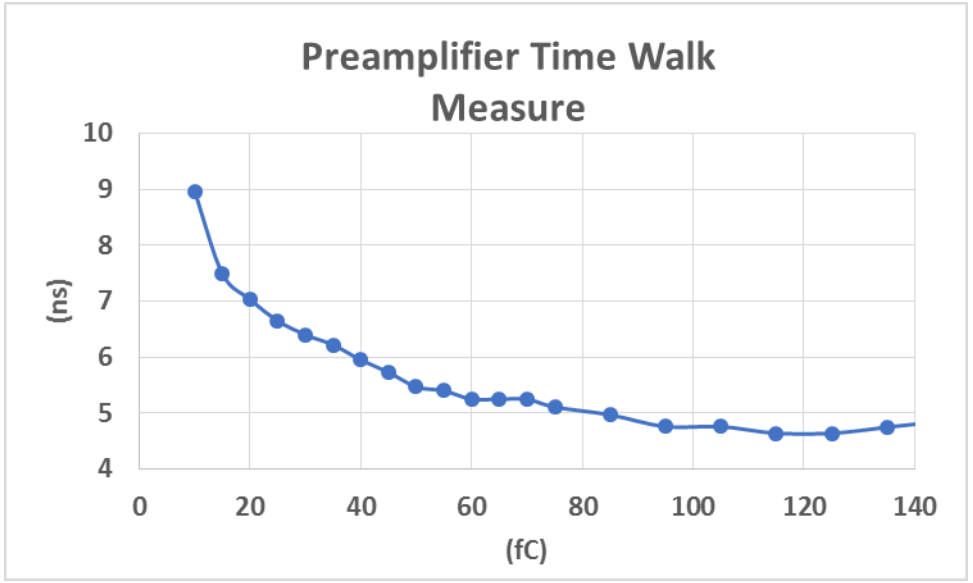
- ENC vs detector capacitance. Spec : ENC < 2500 e- @ Cd=50 pF
- Quadratic fit of ENC² gives e_n and C_PA
  - $ENC^2(Cd) - ENC^2(0) = 3^E4\ e_n{}^2/\ tp\ (\ Cd^2 + 2\ Cd*Cpa) \quad = \alpha Cd^2+\beta Cd \Rightarrow \quad e\_n= sqrt\ \alpha\ tp/3^E4\ ;\ Cpa= \beta/2^\alpha$
  - Here e_n = 0.79 nV/ C_pa = 12.5 pF in measurement and 0.75 nV 11 pF in simulation
  - Preamp contributes ~75% to total noise

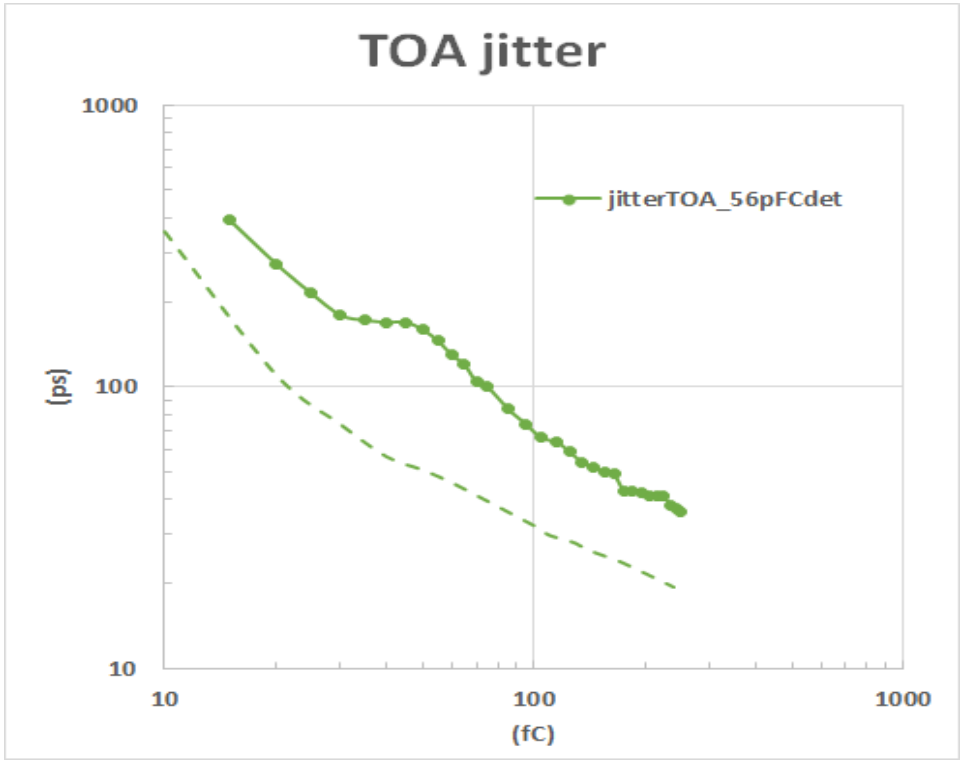




Preamp timing measurements

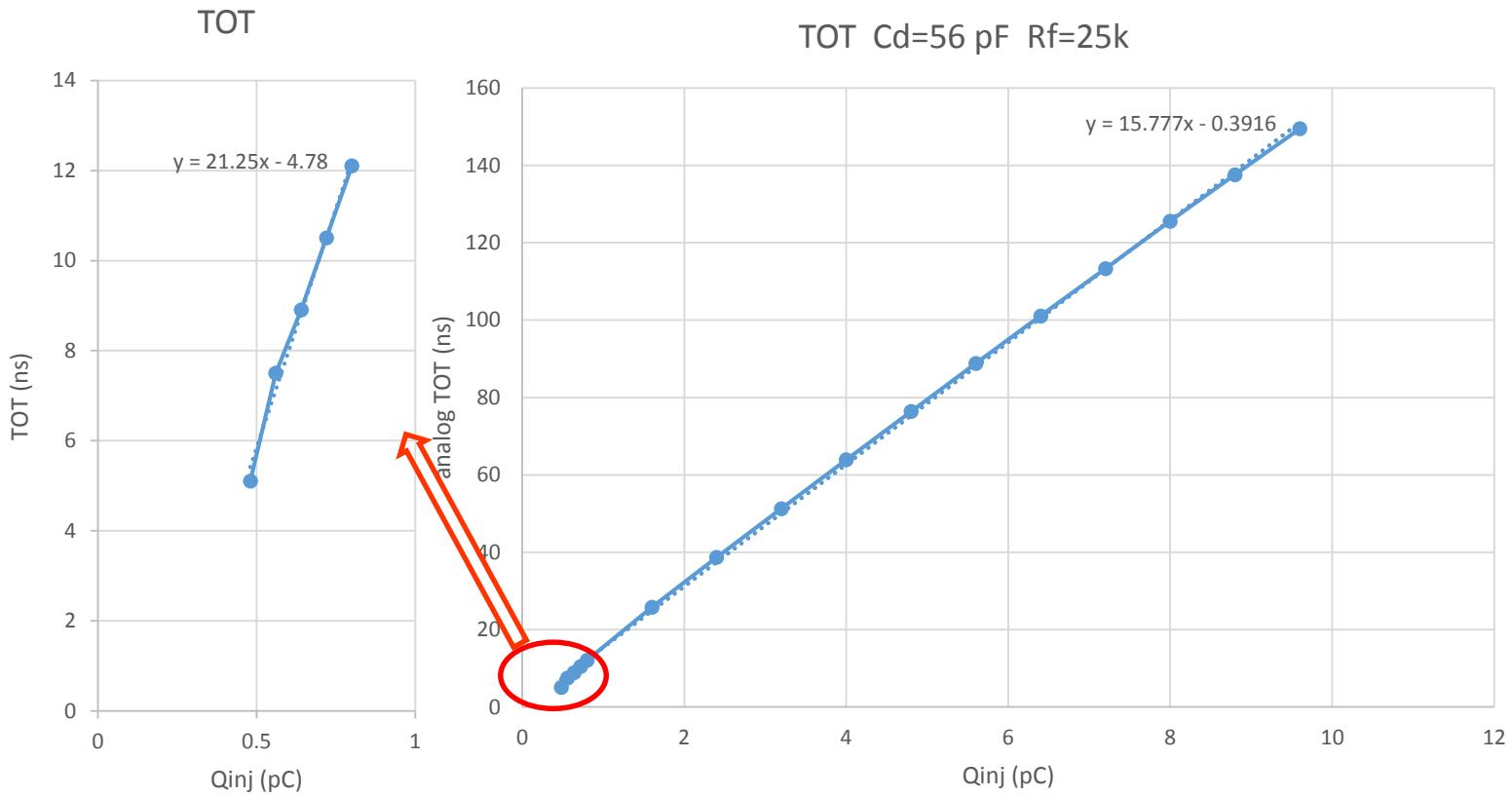
- TOA discriminator output (scope measurement, no TDC)
- TOA Time walk and jitter
  - TW in good agreement with simulations (~8 ns risetime @Cd=50 pF)
  - Jitter larger than simulation ~ 5-7 ns/Q(fC) compared to 3 ns/Q(fC)

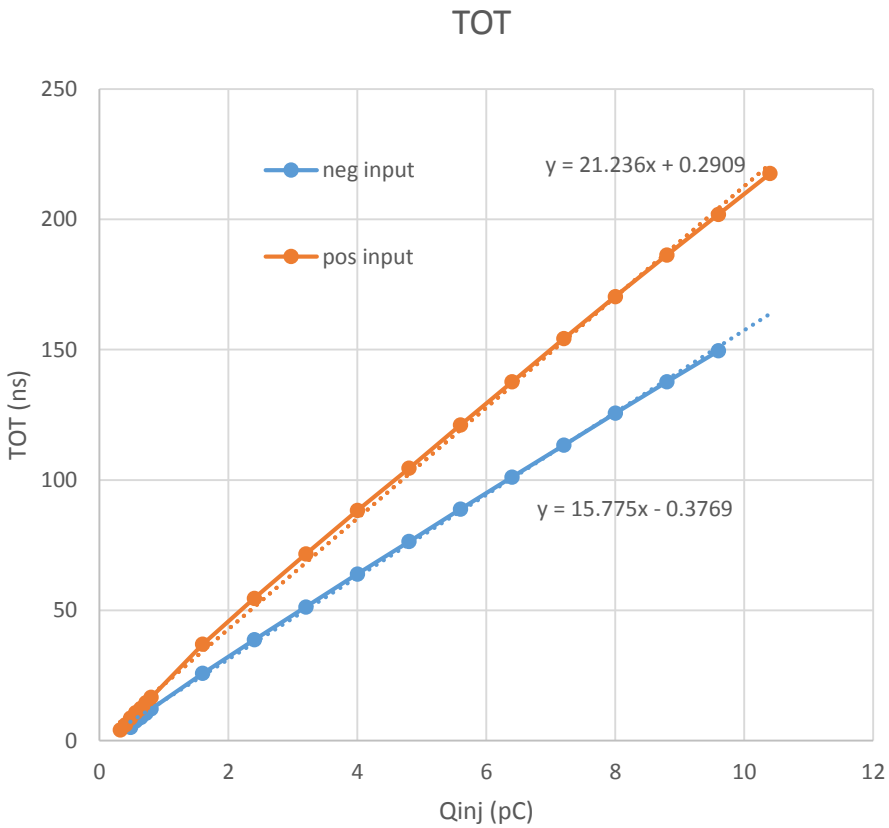




TOT (analog) measurement

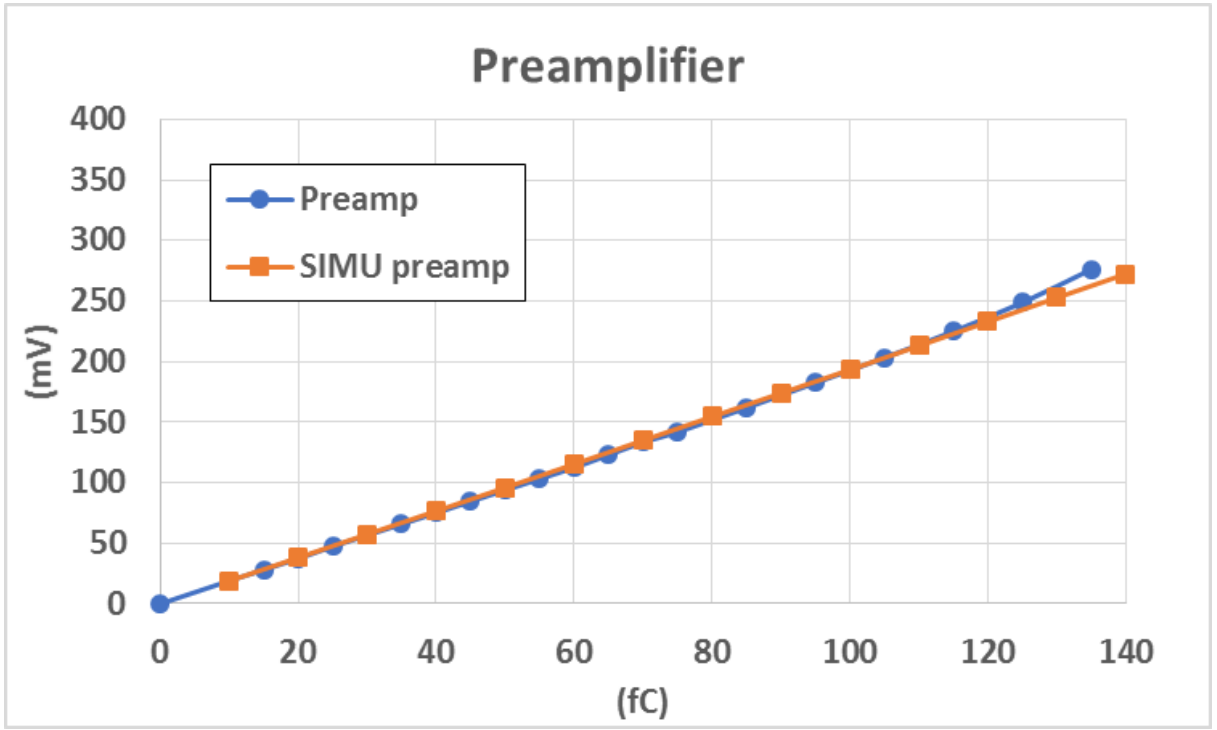
- TOT discriminator output (scope measurement, no TDC)
  - Slope tunable ~16 ns/pC. Full range < 200 ns = 8 BC
  - Noise ~50 ps corresponds to ~3 fC
  - Stub on PCB impedes shortest TOT measurements

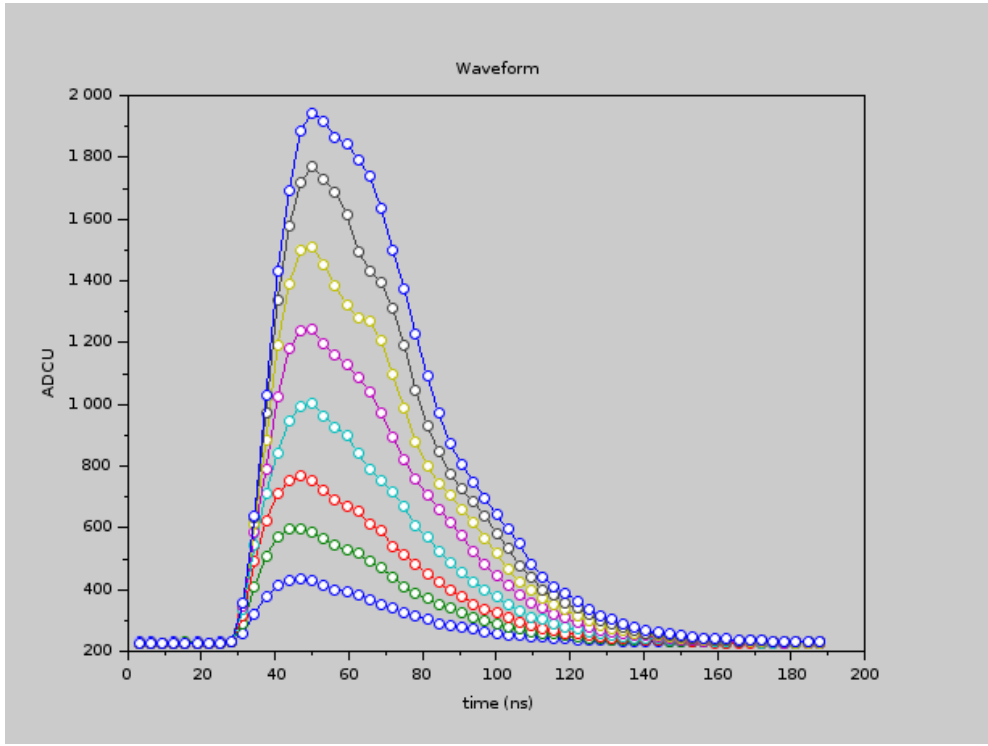




Preamp linearity measurements

- The preamplifier works as expected: linearity and amplitude similar to the simulations
- Amplitude measured with TOT discriminator

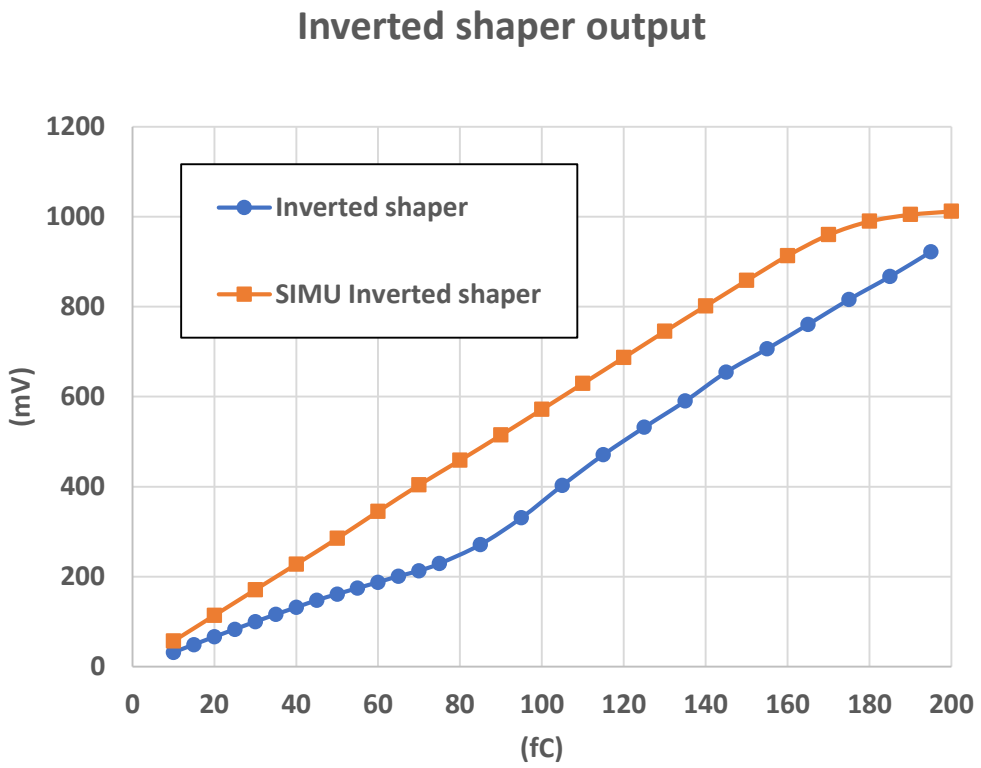


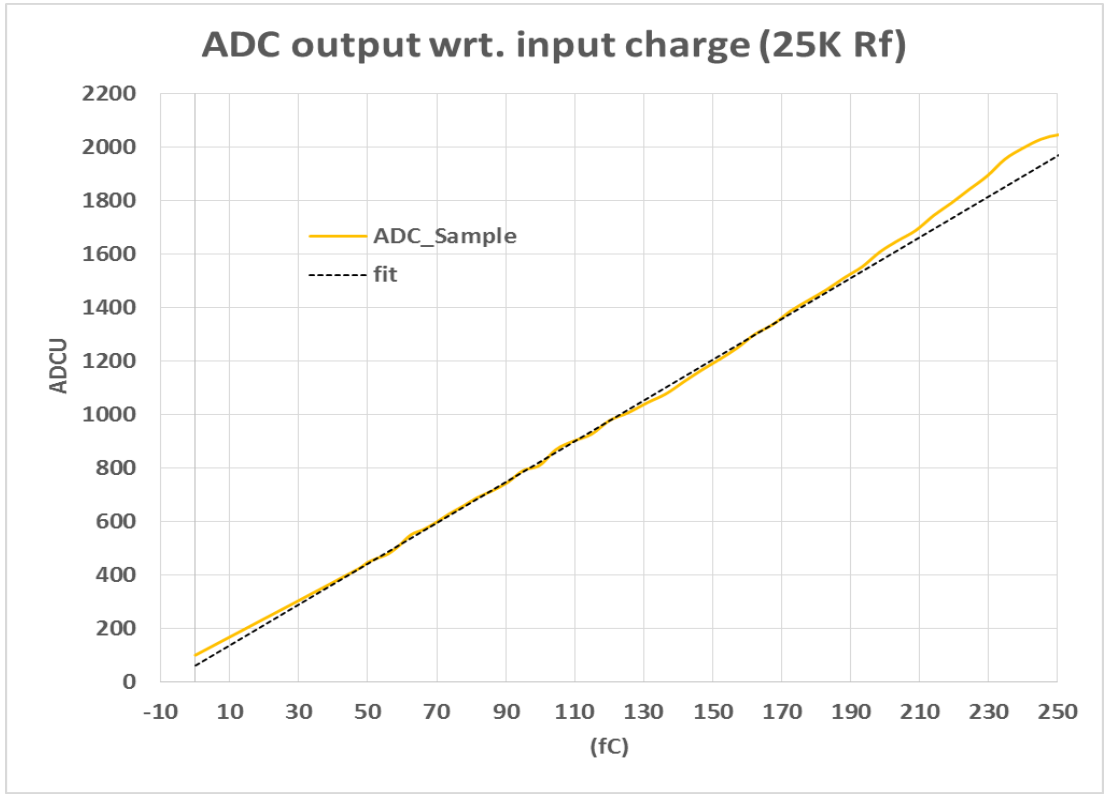


Waveform scan with the ADC

Charge measurement

- Strong non-linearity on probe measurement !
- But ADC measurement ~OK



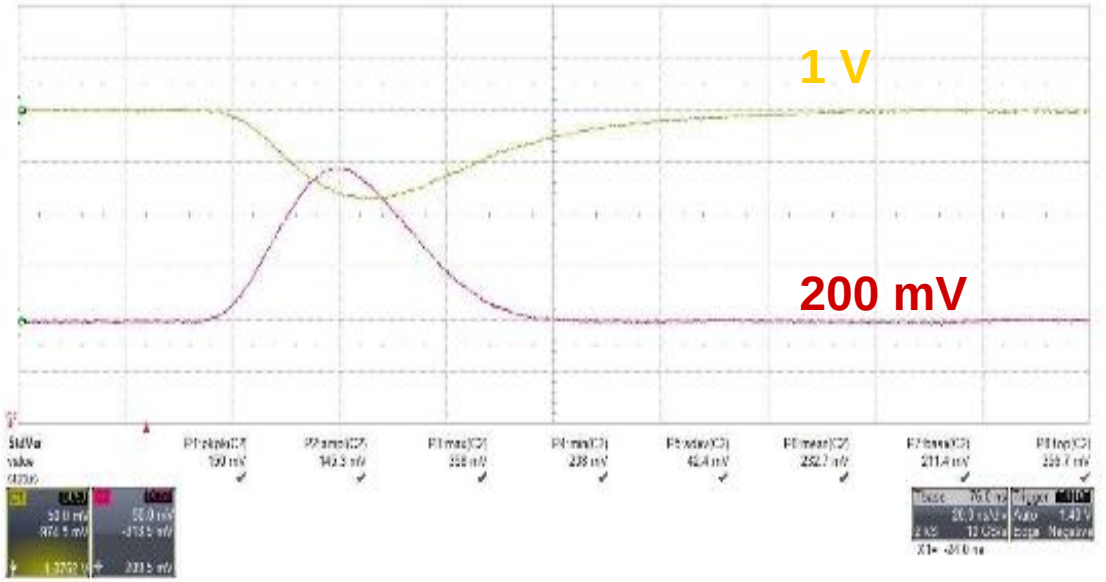


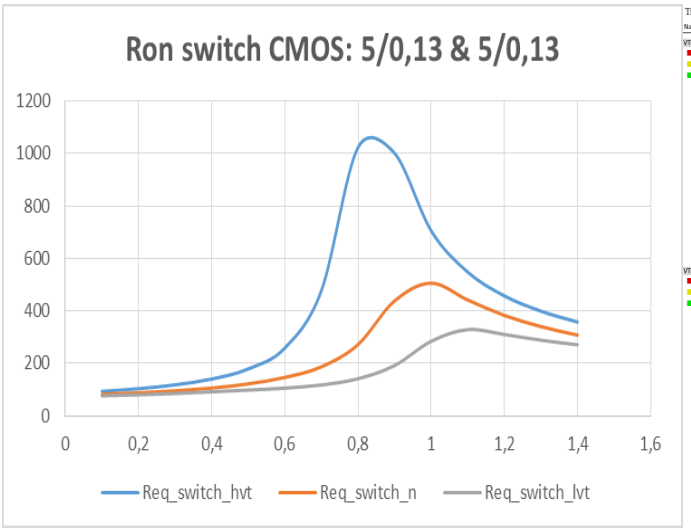
Shaper linearity issues (on the SCOPE)

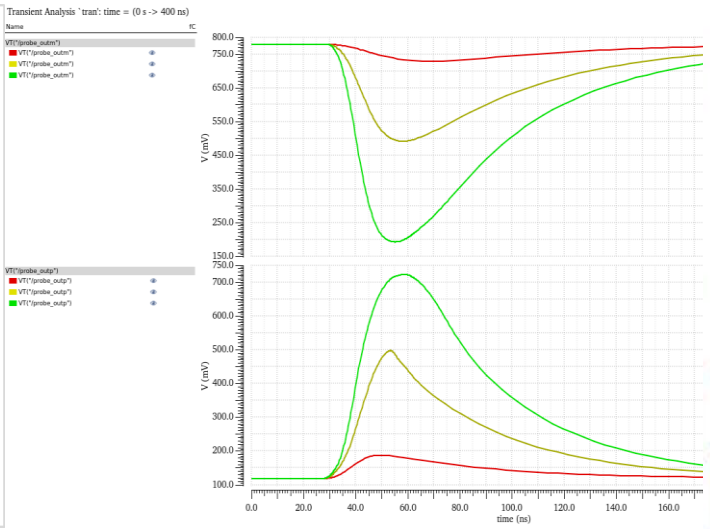
- Two issues appear when the signal sits in the upper voltage range
  - The signal is too slow
  - The amplitude is lower than expected

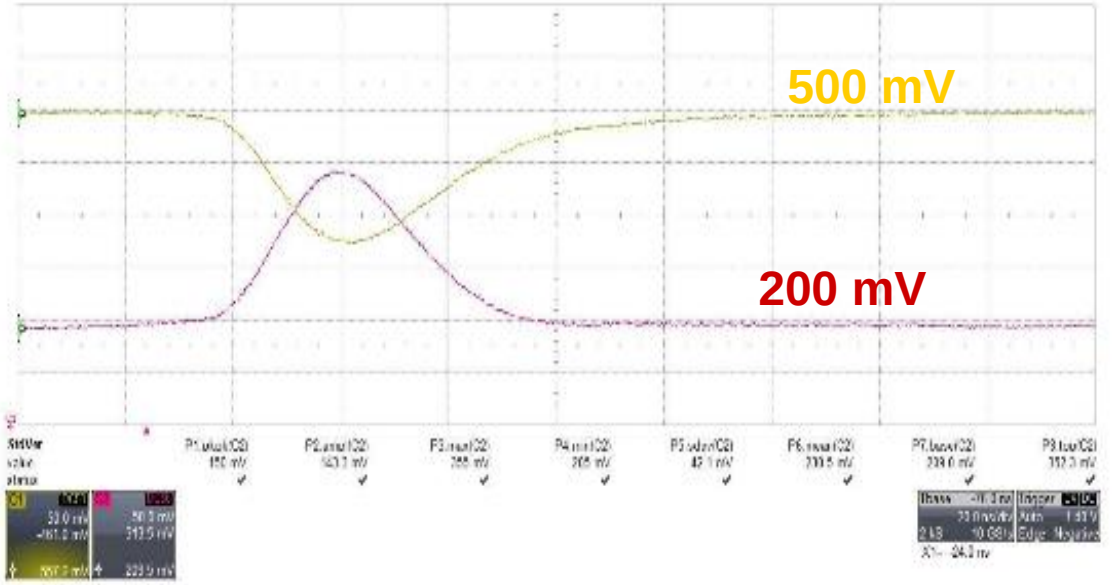
➔ The behavior looks like a RC filter applied to the shaper output but with a pole depending on the voltage level

➔ Probe switches made of HVT MOS (blue) (In TV2, switches made of normal Vt in orange)





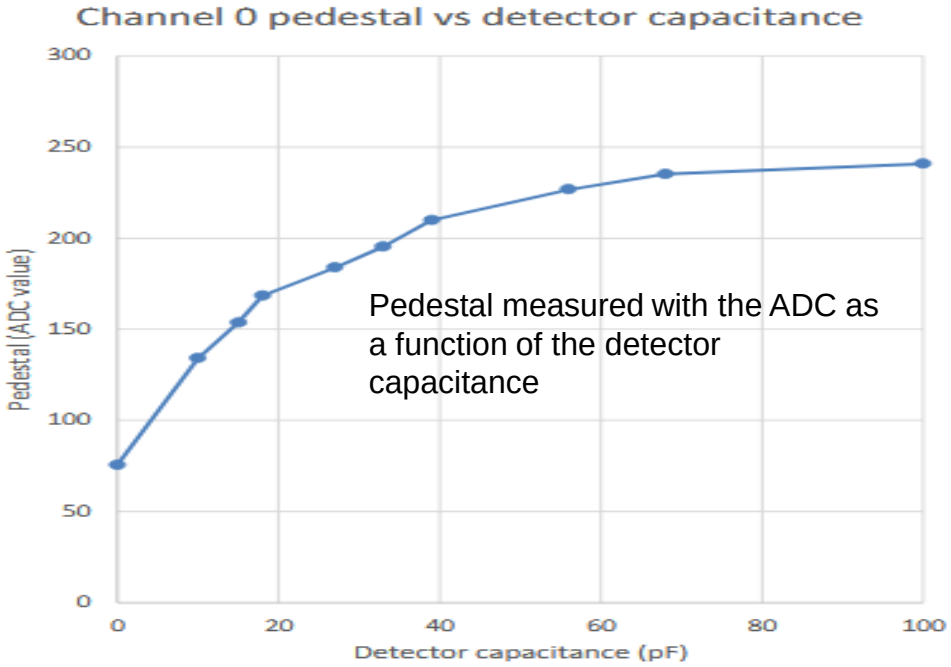




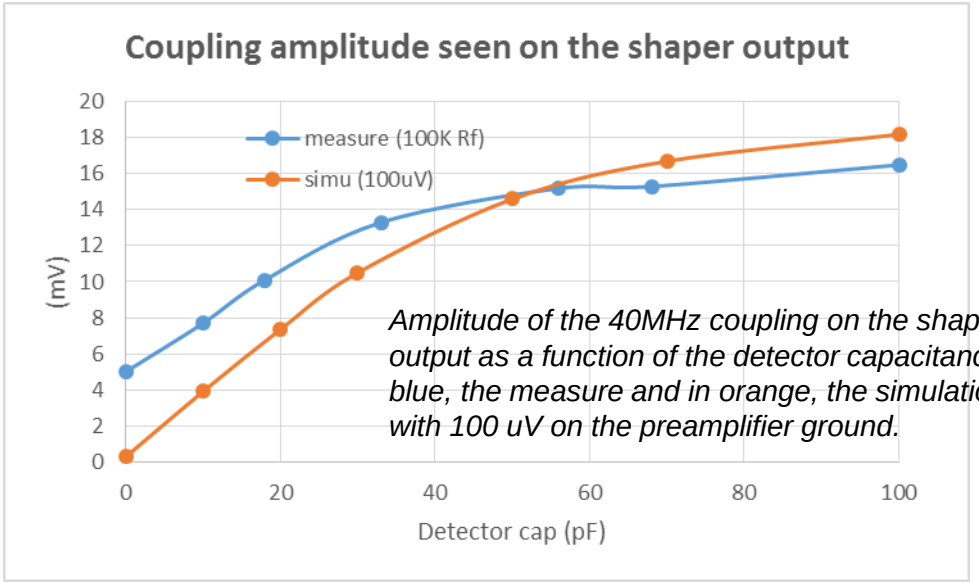
ADC characterization

- ADC linearity still under investigation but INL/DNL appear too large
  - Poor extraction of parasitics in 614 C-2C DAC

  => Use Krakow's ADC in next chip : silicon proven
- Pedestal variation with sensor capacitance
  - A good indicator of digital noise sampled synchronously
  - Noise gain goes as Cd/Cf ~100



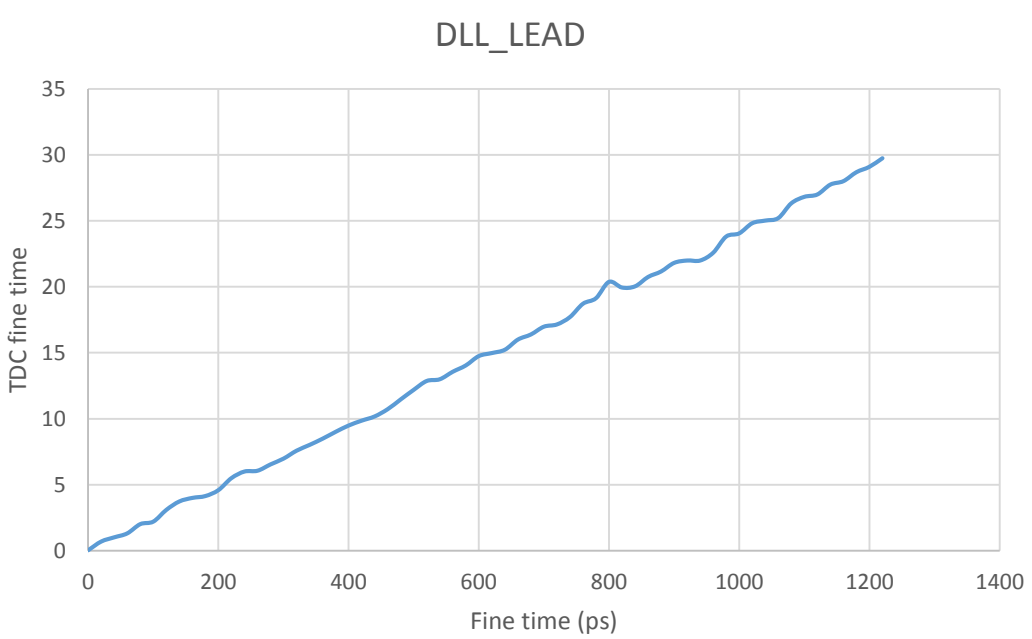
Pedestal measured with the ADC as a function of the detector capacitance

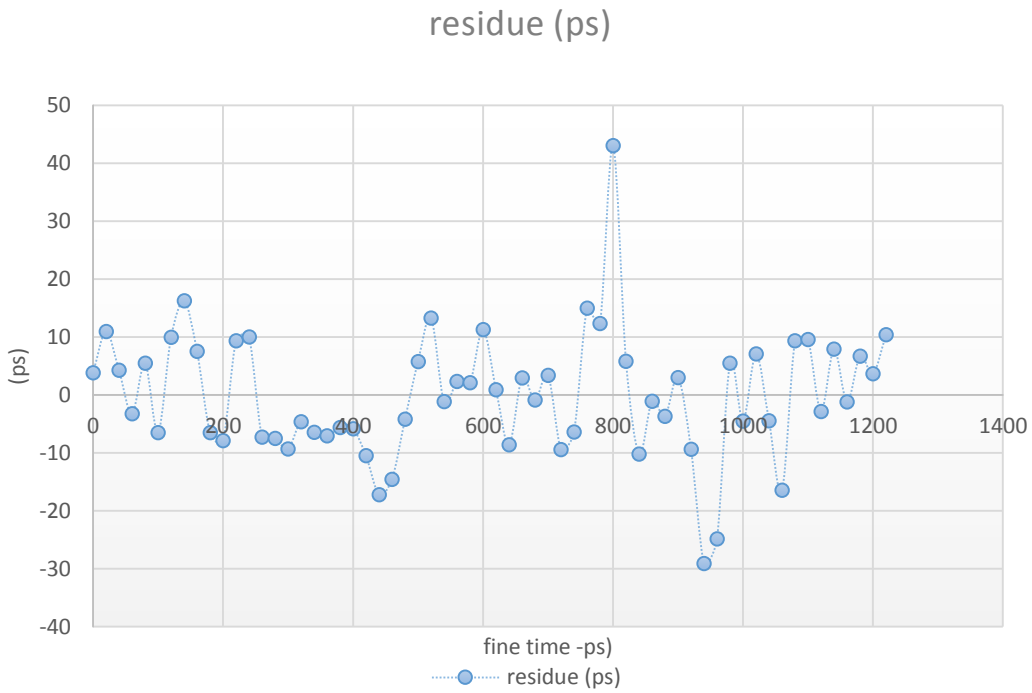


Amplitude of the 40MHz coupling on the shaper output as a function of the detector capacitance. In blue, the measure and in orange, the simulation with 100 uV on the preamplifier ground.

TDC measurements

- TOT TDC based on CERN pico-TDC design [Paulo]
- 640 MHz counter for coarse time and 32-taps DLL for fine time : LSB = 40 ps
- Good noise (~ 30 ps), INL, DNL OK
- But large power dissipation (3 mW/ch)

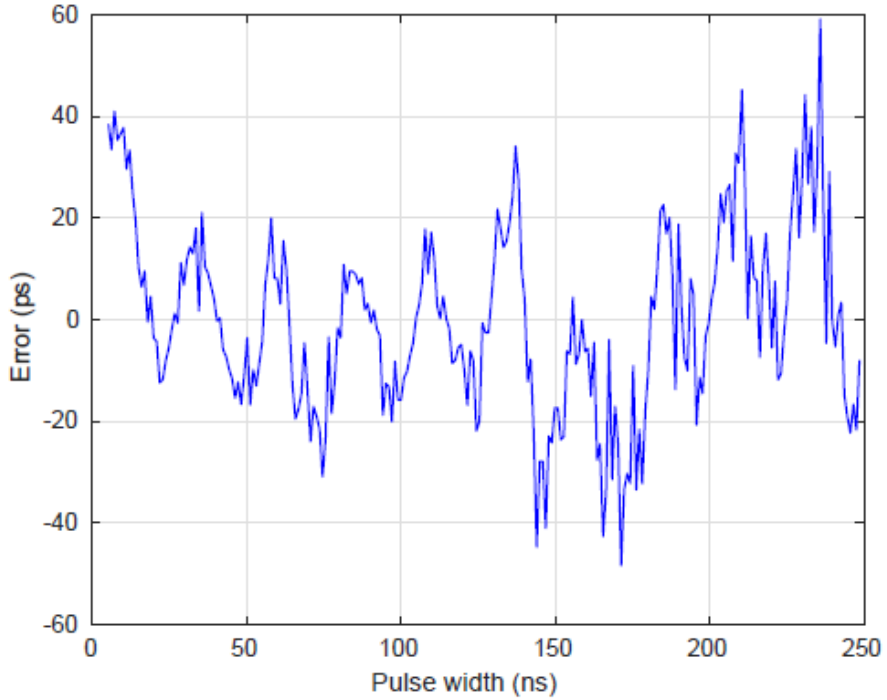




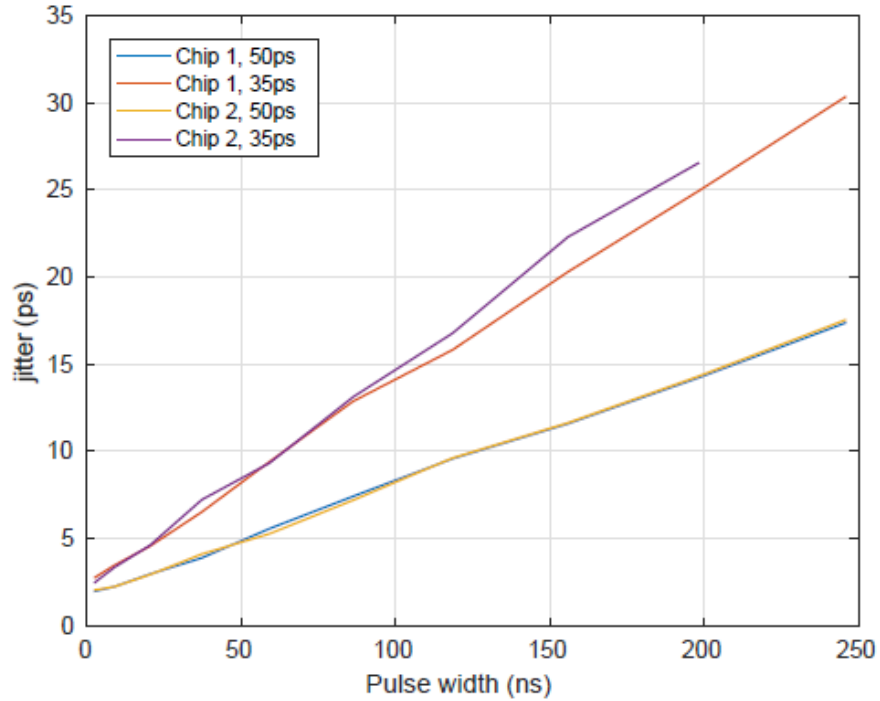
TOT TDC from IC

- Minimum bin size < 35 ps
- All channels within +/- 2.5%
- Power < 500 µW
- Good results, but open loop configuration : needs regular calibration

INL

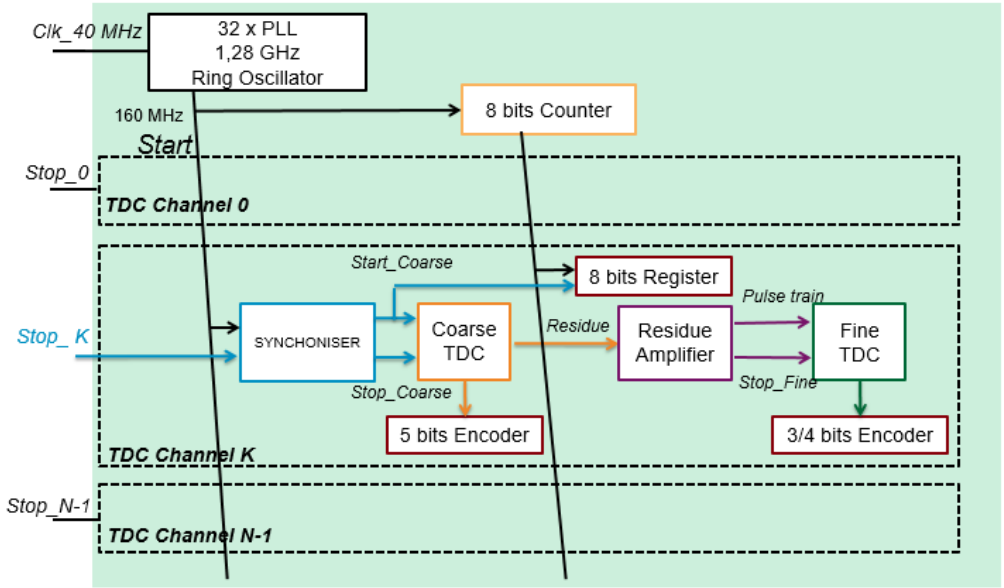


Jitter



MULTI-CHANNEL TDC ARCHITECTURE FOR TOA MEASUREMENT

10/11 bits over 25 ns multichannel TDC architecture :



3 stages TDC (LSB 25 or 12 ps)

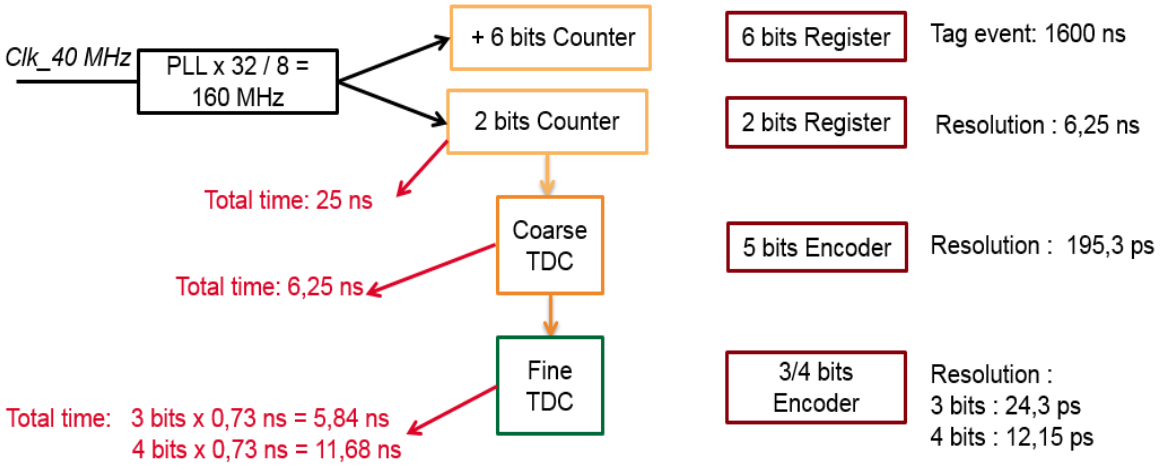
TDC resolution is increased by a counter

The 2 most significant bits of the TDC are now obtained by a **counter** operating at the CTDC frequency who is also a multiple of the 40 MHz bunch clock.

The common 8-bit counter ➔ 2 bits for LSB and 6 other bits for bunch marking.

A common PLL in phase with the external bunch clock (40 MHz)

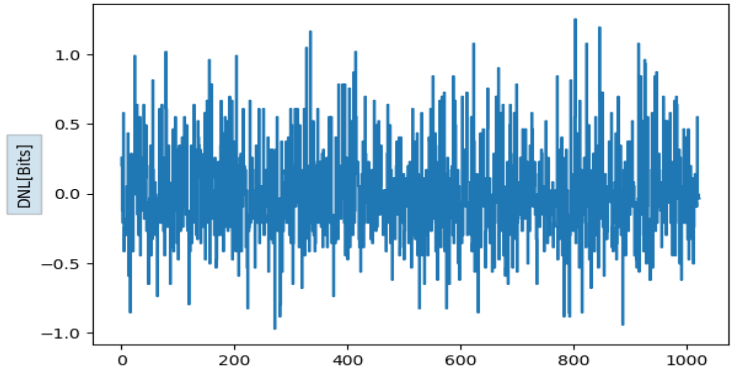
Timing and resolution :

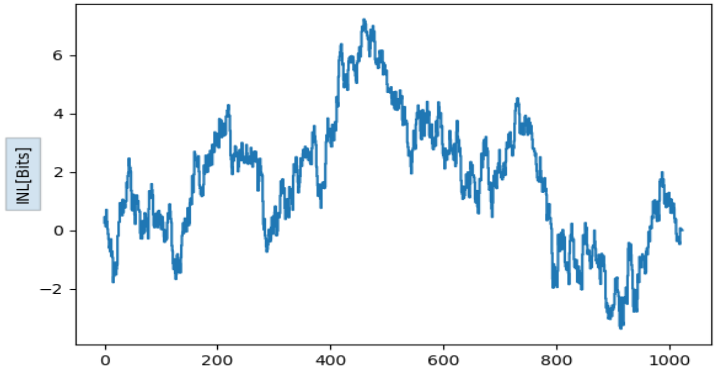


$$RMS_{quantisation} = \frac{LSB}{\sqrt{12}} = 3{,}5 \text{ ps}$$

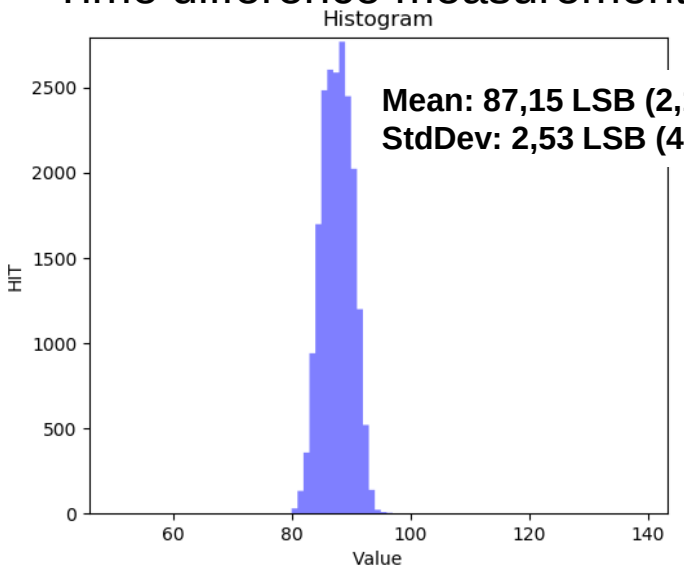
TOA TDC PERFORMANCES

Configuration 10 bits TDC over 25 ns (24,4 ps LSB)





Time difference measurement



Mean: 87,15 LSB (2,12ns)
StdDev: 2,53 LSB (43,6ps)*

*** Dominated by the INL**

TDC channels and PLL are fully working as expected

About the TDC : (10-11 bits)

➔ 25 ns total range is covered
➔ Conversion time < 25 ns
➔ **Internal servo-controlled DLL : commun master DLL for a continuous self-calibration** is working (no calibration phase needed)
➔ Power consumption : 1.5 mW for the master DLL , **2.1 mW/channel hit (0 if no hit)**
Area : 250 µm x 160 µm
⇒ **Performance under study but results in asynchronous mode =>**
⇒ **DNL <+/- 1LSB, INL ~10LSB peak-to-peak (TBC with more statistics)**
⇒ **TDR => ~40 ps RMS for each channel**

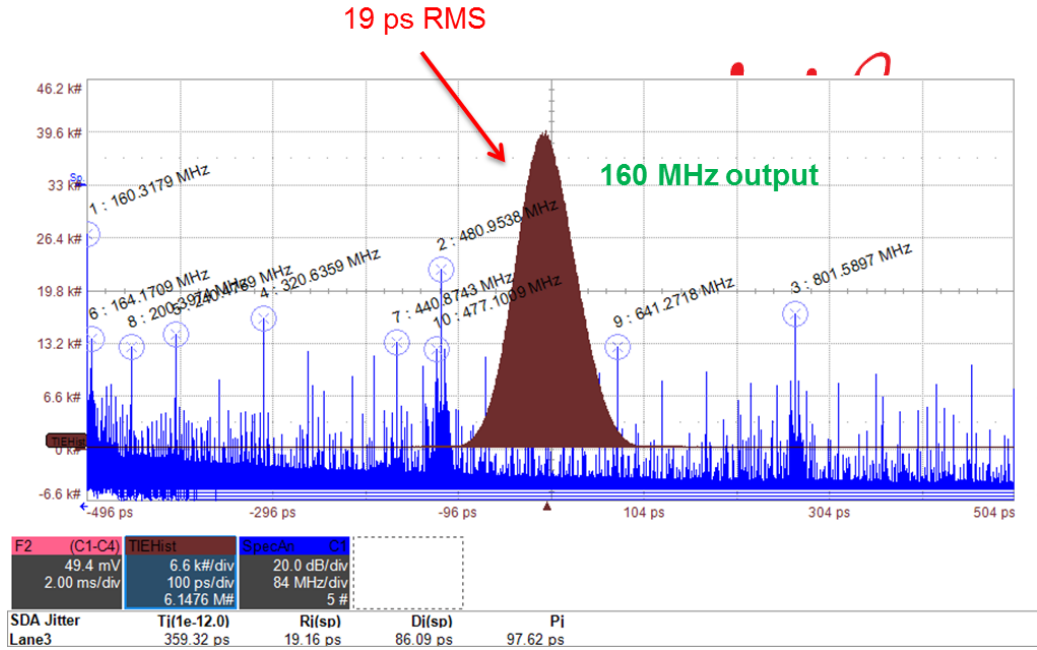
Next steps :

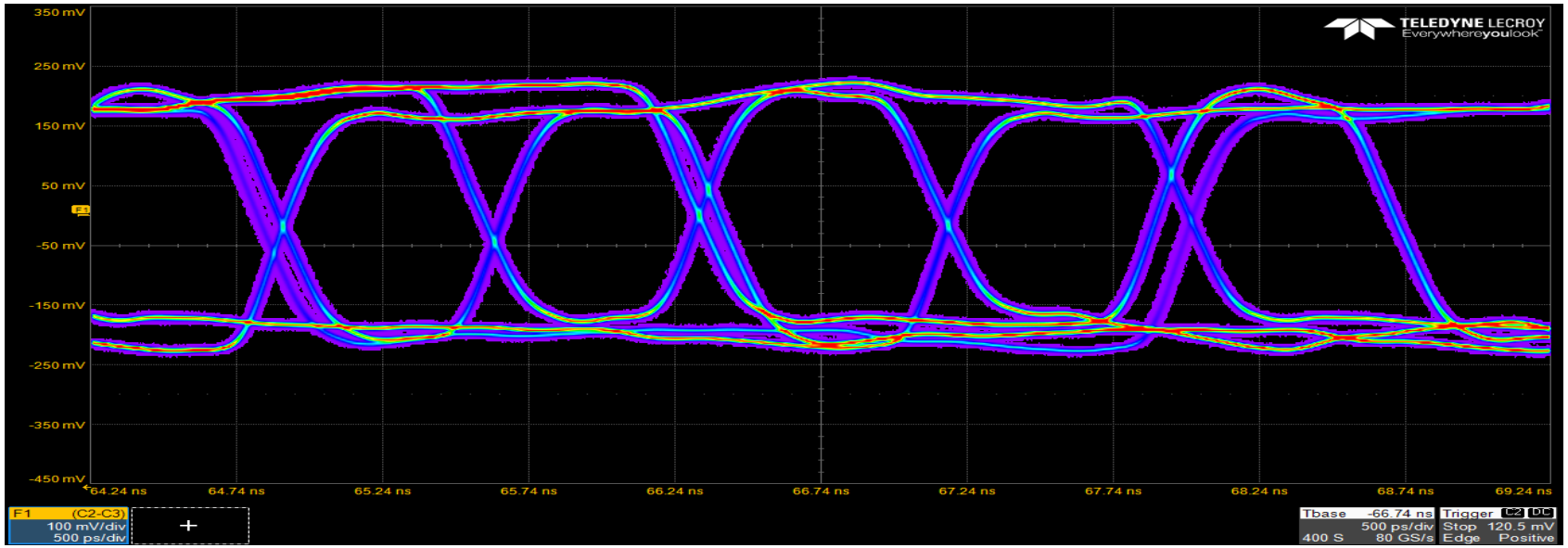
➔ Need to increase the statistics => test bench improvement
➔ Systematic test of all channels
➔ Test if offline correction of INL is efficient. Q: Is it possible in the CMS context ?
➔ Tests with synchronous **pulses => test bench modification**
➔ **Upgrade the design**

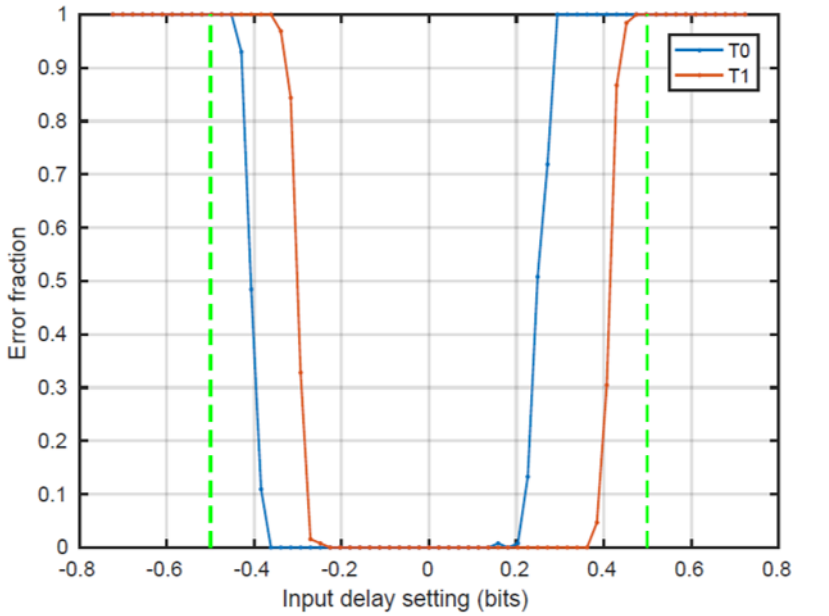
PLL and E-links

- PLL works well with jitter < 20 ps

- Trigger path running at 1,28 Gb/s
  - Work going on at LLR/Split to reconstruct trigger data
  - Good eye opening
  - But asymetry in final multiplexer to be fixed

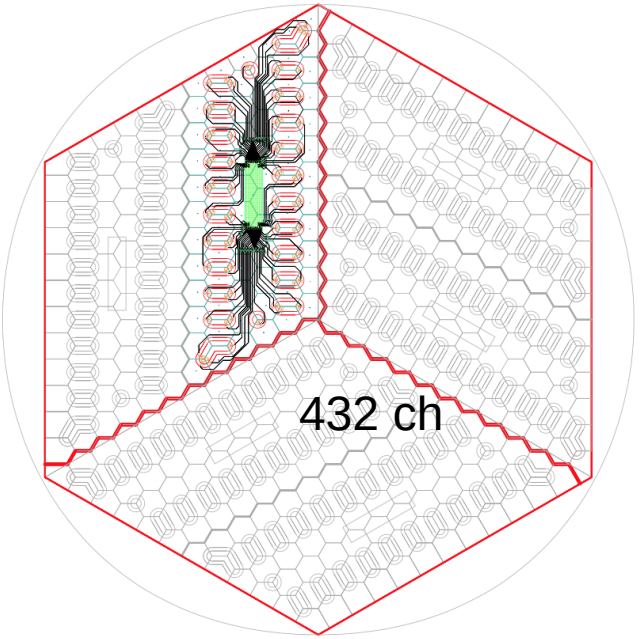


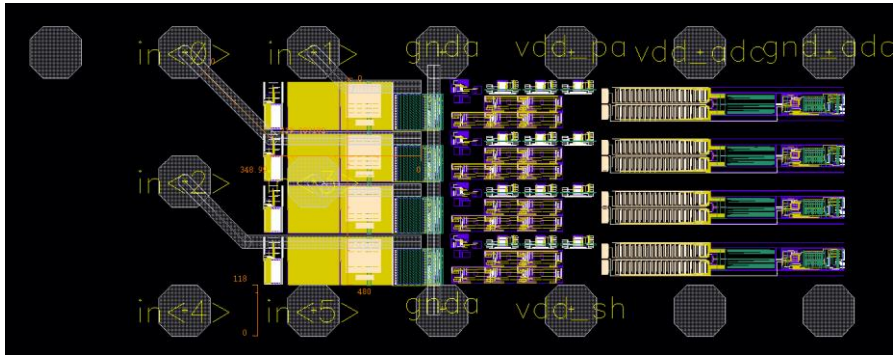




Next steps : HGCROC2

- Full size 72 channels final pinout
- Final interfaces : I²C and Fast commands
- Final analog/mixed blocks
  - Faster preamp for better timing
  - Fourth order Sallen-Key shaper for fast return to baseline
  - Krakow's ADC
  - CEA TDC for both TOA and TOT
- New DRAM from CERN
- New C4 packaging
  - Strong constraints on the layout
  - Better power supply distribution
- Submission in MLM dec 2018





PA+Sh+ADC = 1500*120 µm

Conclusion

- HGCROC is making good progress but a lot remains to be done !
  - Testbench measurements, irradiation measurements, testbeam measurements…
  - Next version HGCROCDV1 (dec 18) will provide full scale prototype for sytem studies

- Thanks for your attention

- HGCROC designers : AGH, CEA-IRFU, CERN, Imperial, OMEGA
  - G. Bombardi, J. Borg, F. Bouyjou, E. Delagnes, F. Dulucq, M. El Berni, O. Gevin, F. Guilloux, M. Idzik, C. de La Taille, A. Marchioro, J. Moron, L. Raux, D. Thienpont, T. Vergine
- HGCROC measurements : *id*. + LLR & FESB Split
  - *id.* + PA Bausson, L. Bernardi, S. Callier, D. Coko, P. Dinaucourt, Y. Geerebaert, ,A. Lobanov, I. Mandjavidze, I. Puljak, O. Sahin, F. Thiant, A. Zabi

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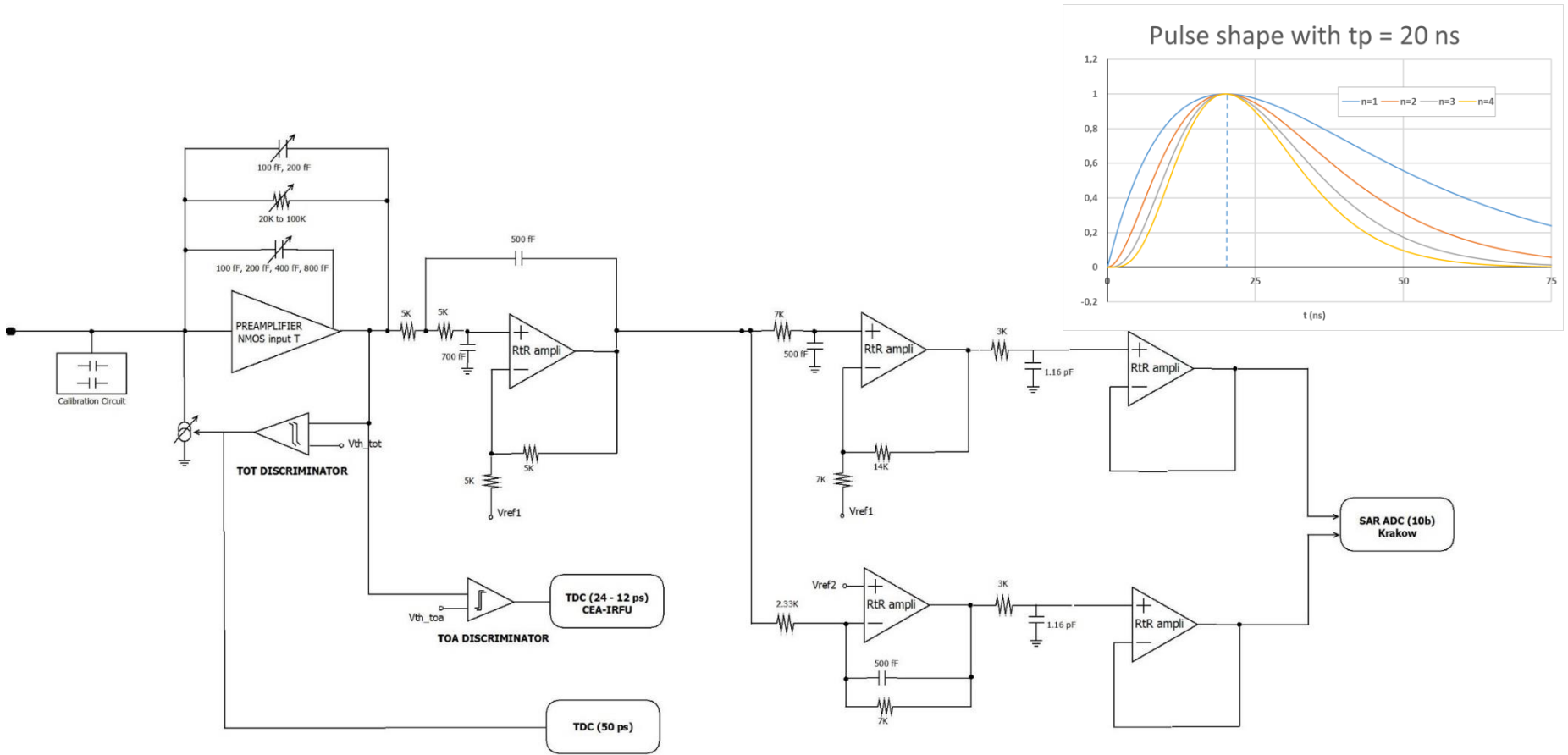
Backup

Preamp gain / polarity

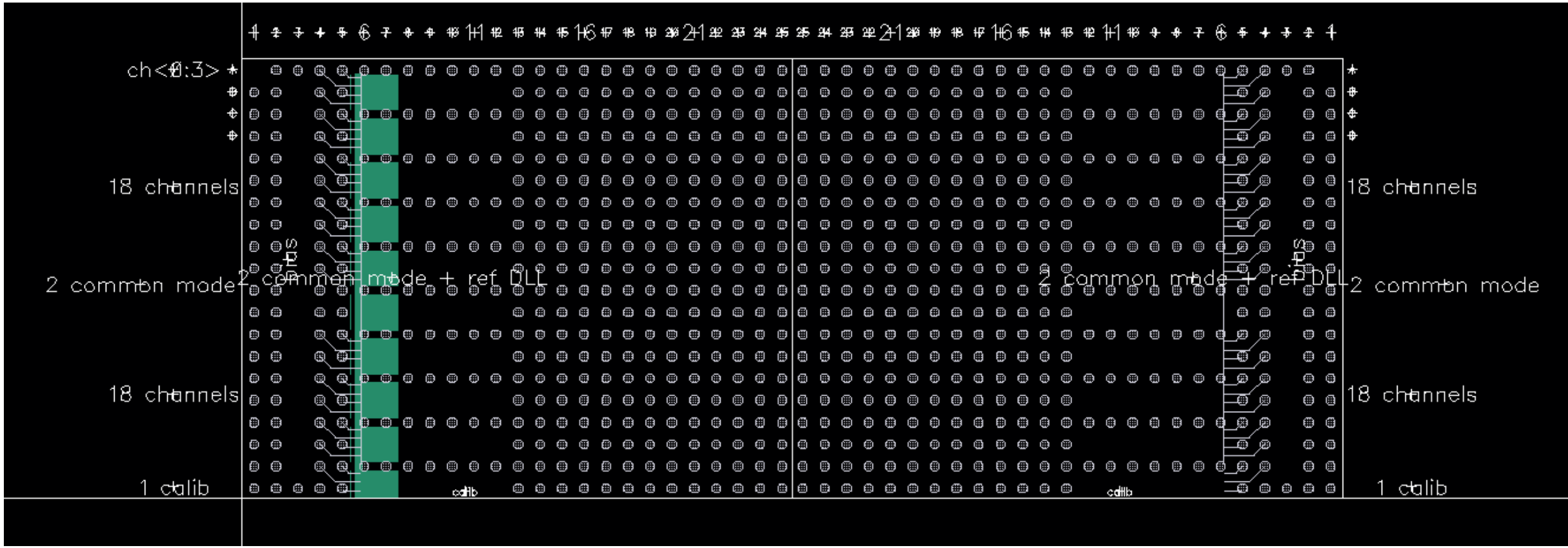
- Go for 3 gains with saturation at 80-160-320 fC (~100 MIP)
  - 2 bits to select Rf and Cf, keeping RfCf = 10 ns
- Keep dual polarity (for 300 um)

thickness	MIP		Noise		LSB	ADC range	ADC range	MIP	Noise
	e-	fC	e-	fC	fC	fC	MIP	ch above ped	LSB
120um	9000	1.4	2000	0.3	0.4	320	222	3.6	0.8
120um	**9000**	**1.4**	**2000**	**0.3**	**0.2**	**160**	**111**	**7.2**	**1.6**
120 irrad (worse 3000 fb-1)	**6000**	**1.0**	**2600**	**0.4**	**0.1**	**80**	**83**	**9.6**	**4.2**
200 um	15000	2.4	2500	0.4	0.4	320	133	6.0	1.0
200 um	**15000**	**2.4**	**2500**	**0.4**	**0.2**	**160**	**67**	**12.0**	**2.0**
200 irrad (worse)	**6000**	**1.0**	**3000**	**0.5**	**0.1**	**80**	**83**	**9.6**	**4.8**
300 um	**20000**	**3.2**	**2000**	**0.3**	**0.4**	**320**	**100**	**8.0**	**0.8**
300 irrad (worse 3000fb-1)	**10000**	**1.6**	**2200**	**0.4**	**0.2**	**160**	**100**	**8.0**	**1.8**
300 irrad (worse 3000 fb-1)	10000	1.6	2200	0.4	0.1	80	50	16.0	3.5

- Selection of 4th order Sallen-Key
  - Similar performance with pole/zero
  - Pole zero more complicated with variable preamp gain
  - 3 stages needed to drive ADC properly



Next steps : HGCROC2



Simulated timing performance in HGCROV1

- Fast discriminator at preamp output
- Expected performance : j = 3,5 ns/Q(fC) at Cd=50 pF
- Time walk : 8 ns

Two approaches to improve jitter for HGCROC-DV1 :

- Increase current in preamp to improve speed and noise
  - 1 mW extra power => lower noise
  - 4 ns rise time
  - S(1 fC)/N ~ 1.8
  - Simulated jitter j = 2.3 ns/Q

- New innovative fast branch in preamp (time output)
  - 1 ns rise time output
  - 1 mW+ 300 uW extra power
  - S(1 fC)/N ~ 0.5 with 50pF detector capacitance
  - Simulated jitter : j = 1.6 ns/Q

Jitter: new fast output vs. new charge output

- New charge preamp: + 1mW
- New fast preamp: +1,3 mW

- Minimum Q for ToA
  - Charge output: <5fC
  - Time output: >10fC but 30ps jitter better