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## HGCROC-V1: a prototype ASIC for CMS HGCAL

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For the high granularity end-cap calorimeter upgrade (HGCAL) of CMS, HGCROC-V1 was submitted in July 2017. It has 32 channels with the low noise preamplifier followed by 25 ns shapers, ADC and TDCs for the charge and time measurements. A 512 deep memory stores the digitized data until the readout is performed at 320 Mb/s. A trigger path, done by summing clusters of 4 adjacent channels, gives a compressed charge information at 40 MHz. Its data are serialized through a dedicated link at 1.28 Gb/s. The chip embeds all necessary ancillary services as bandgap circuit, PLL and reference voltage DACs.

### Summary

The high granularity silicon tungsten calorimeter (HGCAL) chosen by the CMS collaboration to replace its endcaps for the phase 2 upgrade will provide unprecedented 5D images of electromagnetic showers. The sensors are made of  $\sim 1\text{cm}^2$  PIN diodes of 100-300  $\mu\text{m}$  thickness providing a MIP signal around 1-4 fC. With 6 million channels of low noise, high speed and large dynamic range readout electronics embedded on detector, the front-end ASICs are very challenging and innovative. The total power dissipation is below 15 mW/ch and the radiation hardness up to 200 Mrad.

HGCROC-V1 has 32 channels of the full analog chain: low noise, high gain and dual polarity preamplifier followed by single-to-differential 25 ns shapers, 11-bit 40 MHz SAR-ADC, which provides the charge measurement up to 100 fC. Above 100 fC, a discriminator and TDC provide charge information from TOT (Time Over Threshold) over 200ns dynamic range and 50 ps binning. Two different TDCs were submitted to perform the TOT measurement: one based on a global DLL running away at 640 MHz, the other one based on a ring oscillator but running only when a TOT signal occurs. A fast discriminator and TDC provide timing information to 25 ps accuracy; another TDC architecture was submitted based on a low power local DLL.

The HGCAL detector will participate to the L1 trigger generation, consequently the chip keeps in memory the data during the L1 latency and send out compressed view of the charge information at 40 MHz. The digital processing are divided in two parts: the data path where data are stored in a 512-deep SRAM and the trigger path where they are summed, compressed, serialized and sent out at 1.28 GHz.

The ASIC embeds several critical subparts which have to be characterized separately. Thus, analog performances as noise, linearity and crosstalk will be studied and presented apart. The ADC and the TDCs will be measured also as separated blocks and will be presented. Another critical aspect is the clock performances in terms of stability, jitter, power supply rejection and temperature dependency. These performances will be measured and presented in the talk. High frequency readout will be showed as well, for instance the bit error rate and the eye diagram. At last, digital to analog coupling will be explained and way of improvement will be given.

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