Test results of irradiated CMOS pixel circuits in LFoundry 150 nm technology for the ATLAS Inner Tracker Upgrade

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Outline

• ATLAS Inner Tracker (ITk) upgrade

• CMOS sensor option for pixels

• LFoundry technology demonstrators
  - LF-CPIX characterization and beam measurement
  - LF-Monopix characterization and beam measurement

• Conclusion
The High Luminosity Large Hadron Collider (HL-LHC) is foreseen to switch on by 2026 with a center of mass energy of 14 TeV and a luminosity of $5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, five times higher than at present.

The increased luminosity will result in $\sim$ ten times higher radiation levels and ten times higher data rates.
ATLAS ITk upgrade for HL-LHC

- To match the requirements in terms of radiation hardness, readout speed and granularity at the HL-LHC, the replacement of the present Inner Tracker is needed.
- The new tracker (ITk) will consist of silicon only technologies.

**Outer pixel layers (two official possibilities*)**:
- Classical hybrid pixel as the baseline. (Planar sensor + RD53 readout IC).
- Full monolithic CMOS chip with integrated readout.

<table>
<thead>
<tr>
<th>ATLAS-Pixel</th>
<th>Outer</th>
<th>Inner</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fluence [$n_{eq}/\text{cm}^2$]</td>
<td>$10^{15}$</td>
<td>$10^{16}$</td>
</tr>
<tr>
<td>Ion. Dose [Mrad]</td>
<td>80</td>
<td>1000</td>
</tr>
<tr>
<td>Total area [m$^2$]</td>
<td>10</td>
<td>1</td>
</tr>
</tbody>
</table>

*Technical Design Report for the ATLAS Inner Tracker Pixel Detector
Monolithic CMOS Sensor

- Commercial process (mass production technology).
- No hybridization (reduced material budget and costs, easier procurement).
- Considerable depleted regions in high resistive substrates, fast charge collection by drift.

Two design approaches

**“Large Collection Diode”**

- **PROS:** Short drift distances → radiation tolerant
- **CONS:** Large sensor capacitance → noise & speed (power) penalties

**“Small Collection Diode”**

- **PROS:** Small sensor capacitance → Low analog front-end power
- **CONS:** Long drift distances → Less radiation hard

\[
\text{ENC}_{\text{thermal}}^2 \propto \frac{4kT}{3g_m} C_d^2
\]

\[
\tau_{\text{CSA}} \propto \frac{1}{g_m C_f}
\]
LF technology development line

- The process:
  - DeepNW/DeepPW 150nm LF process
  - 7 metal layers
  - High resistivity (> 2kΩ.cm)

2014~2015
Small size demonstrator

CCPD_LF:
33×125µm² pix; 6pix → 2 FEI4 pix
5×5 mm² IC, bondable to FE-I4
Bonn / CPPM / KIT

2016~2017
Large size demonstrator

LF-CPIX:
50×250µm² pix; diff. pix flavors
10×10 mm²; 2 versions -Guard-Ring-
Bonn / CPPM / IRFU

2017~Present
Large Monolithic demonstrator

LF-Monopix:
50×250µm² pix
10×10 mm² IC
1st full monolithic demonstrator!
Bonn / CPPM / IRFU

Characterization and irradiation results (today !)

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Characterization and irradiation results (today !)
**LF-CPIX**

- **LF-CPIX:**
  - Testing of sensor diode collection part.
  - Testing of analog part of pixels.

**LF-CPIX:**
50×250µm² pix; diff. pix flavors
10×10 mm²; 2 versions -Guard-Ring- Bonn / CPPM / IRFU
**LF-CPIX pixel and matrix architecture**

- **Process**: LFoundry 150 nm CMOS process.
- **Wafer resistivity**: >2kΩ cm.
- **Pixel size**: 250 μm x 50 μm (= FE-I4 readout chip size).
- **Digital Matrix**: 23 x 106.
- **Flavor**: Active pixel (3 types of CSA).

![Diagram of LF-CPIX pixel and matrix architecture]

- **Preamplifier**
  - NMOS input
  - PMOS input
  - CMOS input

- **Readout circuitry LF-CPIX**

- **Comparator**
- **HIT register**

![Diagram of comparator and HIT register]

**Pixel flavors in the matrix**

- NMOS input
- PMOS input
- CMOS input
The breakdown voltage ~ -220V.

All 3 flavors are working well and the threshold can be tuned, the threshold dispersion can be tuned down to 60e-.

Typical noise mean value less than 120e-.

S-curve fit to extract effective threshold and noise.
Setup under proton beam @ CERN PS

- Aug → Sep 2017:
- 24 GeV protons irradiated.
- ~150 MRad reached (roughly 2 times the dose expected for the ITk 4th layer).
- Fluence: $1.71 \times 10^{15} \text{n}_{eq}/\text{cm}^2$. 

Distance of 20m
PS irradiation → 150 MRad

- The threshold mean value for the 3 flavors are 2000e- after proton beam irradiation up to 150 Mrad.

- The threshold dispersion for the 3 flavors can be tuned to less than 50e- after proton beam irradiation up to 150 Mrad.
PS irradiation → 150 MRad

- The noise mean values for all flavors are less than 200e- at low temperature after proton beam irradiation up to 150 Mrad.

![Graph showing noise distribution for NMOS flavors at different temperatures](image)
**LF-Monopix**

- **LF-Monopix:**
  - 1st full monolithic concept.
  - 1st test of the digital architecture.

**LF-Monopix01** (Monolithic)
LF-Monopix: Pixel design

- 150nm CMOS process, LFoundry (Resistivity >2kΩ.cm).
- Similar diode and analog front end circuitry design as in LF-CPIX.
- 129 x 36 pixel array (9 sub matrices with different pre-amplifiers, discriminators, R/O concepts ...).
- Column-drain R/O logic (FE-I3 like).
- 40 MHz (up to 160MHz by design) LVDS serial output.
LF-Monopix: Laboratory results

- Breakdown $\sim -280$ V $\Rightarrow$ up to $\sim 300$ μm depletion.
- The threshold and dispersion can be tuned down to $2000e^-$ and $100e^-$ respectively.
- The typical noise $\sim 200e^-$. 

### Analog outputs

- **I-V curve**
- **Threshold mapping**
- **Noise mapping**

### Laboratory results

- **I-V curve**
- **Threshold mapping**
- **Noise mapping**

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**LF-Monopix**

- **Laboratory results**

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**Topical Workshop on Electronics for Particle Physics (TWEPP)**
LF-Monopix: Efficiency under ELSA test beam

- ELSA beam:
  - 2.5GeV electron
  - Nov 8-10, 2017

**Un-irradiated chip**

- Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix
- DAC setting: default
- HV: -200V
- Temp: -25°C
- Beam: 2.5GeV electron

**Neutron irradiated (NIEL=10^{15} neq/cm^2)**

- Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix
- DAC setting: default
- HV: -130V
- Temp: -25°C
- Beam: 2.5GeV electron
Leakage Current (LF-Monopix)

Proton beam @ CERN PS
- The set-up was similar to the one of LF-CPIX
- June → Sep 2018:
- 24 GeV protons irrad
- ~160 MRad reached (roughly 2 times the dose expected for the 4th layer)

The leakage current increase after irradiations seems acceptable
Threshold scan after 160 Mrad proton irradiation

- Low Temp: -12°C
- 80 days annealing @ 23°C

Threshold histograms for 6 flavors

Flavor 3:
CMOS AMP
V1 Discriminator
Entries = 516
Mean = 4038.0e-
Sigma = 965.6e-

Flavor 6:
CMOS AMP
V2 Discriminator
Entries = 516
Mean = 5914.8e-
Sigma = 1325.0e-

Flavor 4:
CMOS AMP
V2 Discriminator
Entries = 516
Mean = 5274.6e-
Sigma = 1617.0e-

Flavor 7:
CMOS AMP
V1 Discriminator
Entries = 516
Mean = 5319.7e-
Sigma = 1252.8e-

Flavor 8:
NMOS AMP
V2 Discriminator
Entries = 516
Mean = 5448.8e-
Sigma = 1166.7e-

Flavor 9:
NMOS AMP
V1 Discriminator
Entries = 516
Mean = 4535.3e-
Sigma = 864.0e-
Threshold tuning after 160Mrad proton irradiation

- Flavor8: NMOS AMP+ V2 Discriminator

- TH=0.80V, Temp:-12°C, HV=-40V, 80 days room temperature annealing.

- After tuning, the flavor8 could be tuned to target thresholds (~2800 e-) with a dispersion 156e-.
Conclusion & outlook

- Promising results of **LF-CPIX** were shown in terms of:
  - Good breakdown voltage characteristics (BV below -200V).
  - Radiation hardness of the technology:
    - Tuning of all the 3 flavors possible (threshold dispersion<50e).
    - Limited noise increase after 150 Mrad (noise<200e).
- **LF-Monopix**: fully functional demonstrator chip with column drain readout.
  - Good breakdown voltage characteristics (BV below -270V).
  - Limited threshold dispersion (can be tuned within 110e~148e depending on flavor).
  - ENC for different flavors is between 190e to 280 e-.
  - Good irradiation performances:
    - High efficiency ~99% after 1 x 10^{15}neq/cm^2.
    - Limited leakage current increase after 160MRad.
    - After 160 Mrad proton irradiation, tuning down to 2860e with a dispersion 156e-.
- **Next step and Outlook**.
  - Need to understand the radiation effect on different parts of the chip.
  - Need to reduce the pixel size and leakage current (layout optimization).
  - Based on the results of the LF-MONOPIX, find best strategy for the next demonstrator.

The collaboration works on an improved full size LF CMOS prototype that could be used in ATLAS ITk layer 4 → target: submission in 2019
Thanks for your attention!
General description of the LF-MONOPIX

- 150nm CMOS (Resistivity $>2$ kOhm-cm)
- $129 \times 36$ pixel array
- 40 MHz (160MHz by design) LVDS serial output

- 7 flavors with “in-pixel” R/O logic: NMOS or CMOS amplifier, “V1” or “V2” discriminators, current steering or CMOS token transmission.

- 2 flavours with off-matrix (“external”) R/O logic: CMOS amplifier, “V2” discriminator, NMOS or PMOS source followers.
Calibration of the capacitance (LF-Monopix)

\[ \text{Cinj} = \frac{Q}{V} = N \times \frac{\text{e}}{V} \]

- Cinj: Injection Capacitance
- N: Number of 55Fe electrons (1619e-)
- e: elementary charge
- V: external injection

Calibration of the Capacitance Setup

External Injection  55Fe Source  Signal
Determination of Injection Capacitance

- Injecting charge directly to the pre-amplifier.
- Low feedback voltage (VPFB): Longer ToT (sampling with higher resolution)

\[ \gamma(\text{ToT}) = \alpha \times (1 - \exp(-t/\tau)) \]

\[ \tau = 0.717 \]

Max ToT = 120.568

Sources, LF-MONOPIX01: Pix[26,10], TH = 0.855 V, VPFB=4

\( \mu = 153.036 \)
\( \lambda = 0.445 \)

\( C_{\text{inj}} = Q / V \sim 2.75 \text{ fF} \)

(assuming 3.6 eV/e-)

\( ^{241}\text{Am} \):

16539 e-

\( K_\alpha \quad 12353 \quad e- \)

\( K_\beta \quad 13997 \quad e- \)

Resolution:

(1175 e-) 4.2 keV FWHM
(For \(^{241}\text{Am} x\)-rays)
LF-Monopix01: Pixel design

- Pre-amplifiers => aimed at peaking time $\leq 25$ ns with 400 fF $C_d$
  - NMOS input: modified from LF-CPIX in order to deal with the increased $C_d$
    - Bias current $\sim 17$ $\mu$A
    - Peaking time $\sim 20$ ns (4 ke$^-$ signal)
    - ENC $\sim 170$ e$^-$

- CMOS input: same as LF-CPIX
  - Bias current $\sim 15$ $\mu$A
  - Peaking time $\sim 25$ ns (4 ke$^-$ signal)
  - ENC $\sim 135$ e$^-$
LF-Monopix01: Pixel design

- **Discriminator => influence on the time walk**
  - Discriminator V1: same as LF-CPIX
    - 2-stage amplifier as comparator
    - Bias current: 4.5 µA
    - Slow at threshold edge
  - Discriminator V2:
    - Two amplifiers load each other
    - Self biased: < 4µA
    - CMOS inverter as 2nd stage
LF-Monopix01: Pixel design

- Low noise is critical for some digital blocks
  - Token propagates while pixels are sensitive
    - Current Steering (CS) logic
      => constant current => less noise
LF-Monopix01: Pixel design

- Low noise is critical for some digital blocks

- Data R/O with source follower
  => avoids high current injection into the PW during high to low transition
- SF bias at column end ~20 µA
  • 24 pairs per column => LE, TE, Addr.