

Test results of irradiated CMOS pixel circuits in LFoundry 150 nm technology for the ATLAS Inner Tracker Upgrade

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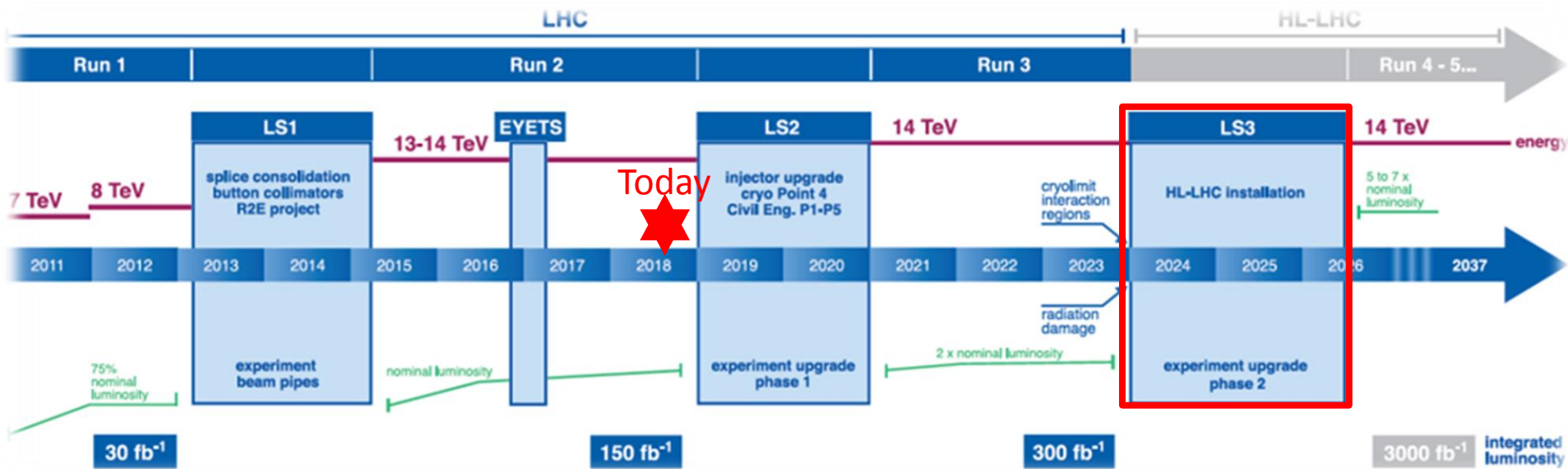
Topical Workshop on Electronics for Particle Physics(TWEPP)

Antwerp, Belgium. 20th Sep 2018

Outline

- ATLAS Inner Tracker (ITk) upgrade
- CMOS sensor option for pixels
- LFoundry technology demonstrators
 - LF-CPIX characterization and beam measurement
 - LF-Monopix characterization and beam measurement
- Conclusion

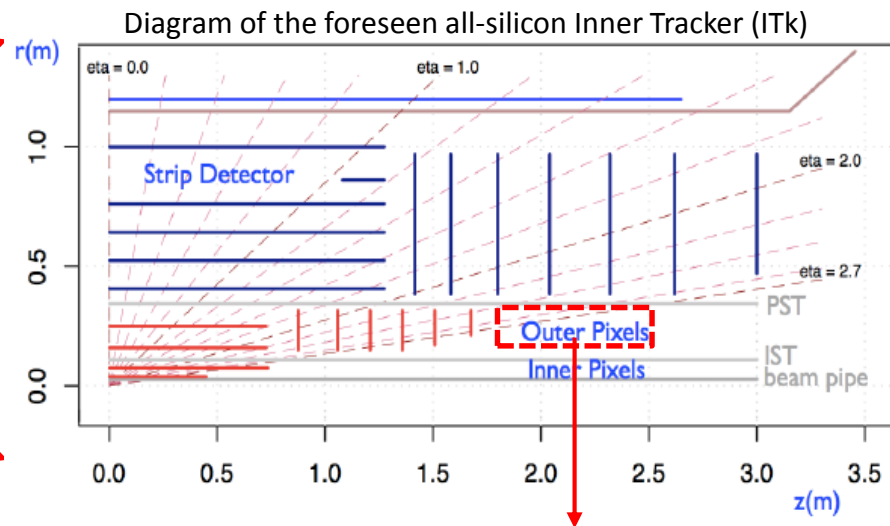
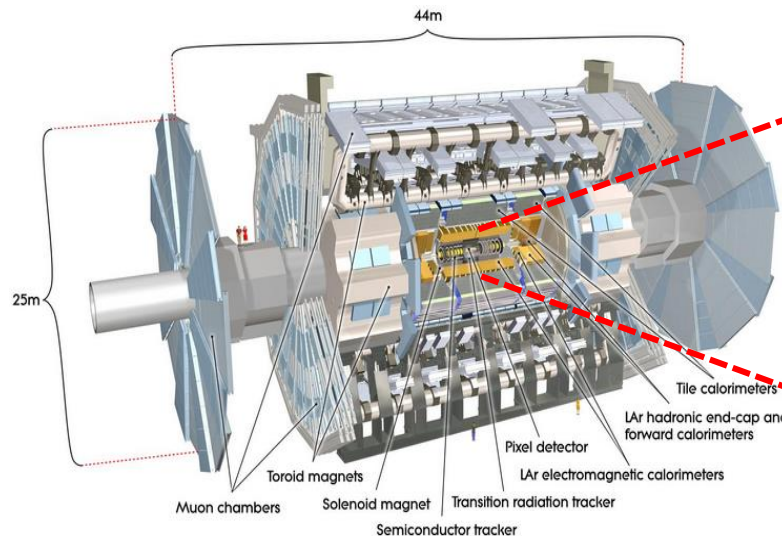
LHC / HL-LHC Plan



- The High Luminosity Large Hadron Collider (HL-LHC) is foreseen to switch on by **2026** with a center of mass **energy of 14 TeV and a luminosity of $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$** , five times higher than at present.
- The increased luminosity will result in **\sim ten times higher radiation levels and ten times higher data rates.**

ATLAS ITk upgrade for HL-LHC

- To match the requirements in terms of radiation hardness, readout speed and granularity at the HL-LHC, the replacement of the present Inner Tracker is needed.
- The new tracker (ITk) will consist of **silicon only technologies**.



- Outer pixel layers (two official possibilities*):**
 - **Classical hybrid pixel** as the baseline. (Planar sensor + RD53 readout IC).
 - **Full monolithic CMOS chip** with integrated readout.

* Technical Design Report for the ATLAS Inner Tracker Pixel Detector

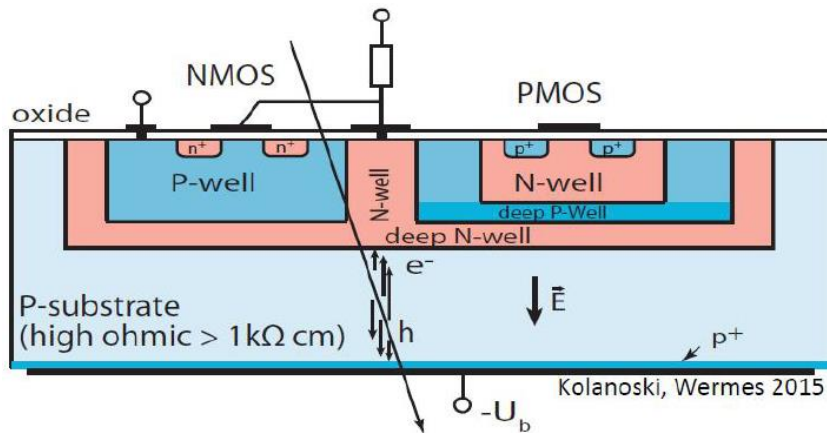
	ATLAS-Pixel	
	Outer	Inner
Fluence [n_{eq}/cm^2]	10^{15}	10^{16}
Ion. Dose [Mrad]	80	1000
Total area [m^2]	10	1

Monolithic CMOS Sensor

- **Commercial** process (mass production technology).
- No hybridization (**reduced material budget and costs, easier procurement**).
- **Considerable depleted regions** in high resistive substrates, **fast charge collection by drift**.

Two design approaches

“Large Collection Diode”



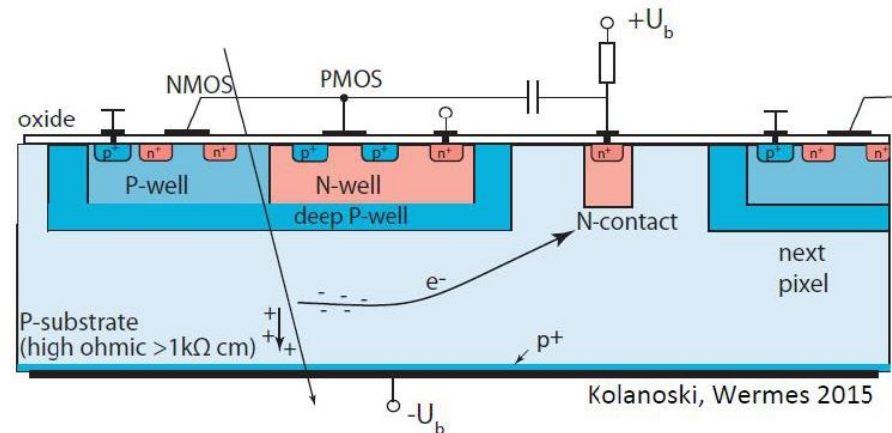
PROS: Short drift distances → radiation tolerant

CONS: Large sensor capacitance → noise & speed (power) penalties

$$ENC_{thermal}^2 \propto \frac{4 kT}{3 g_m} \frac{C_d^2}{\tau} \quad \tau_{CSA} \propto \frac{1}{g_m} \frac{C_d}{C_f}$$

LF foundry technology

“Small Collection Diode”



PROS: Small sensor capacitance → Low analog front-end power

CONS: Long drift distances → Less radiation hard

LF technology development line

- The process:
 - DeepNW/DeepPW 150nm LF process
 - 7 metal layers
 - High resistivity (> 2kΩ.cm)

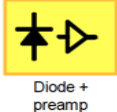
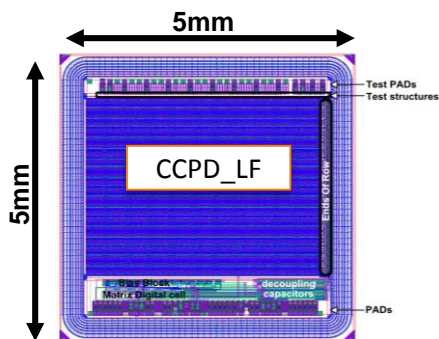
Characterization and irradiation results (today !)

2014~2015

Small size demonstrator

CCPD LF:

33×125μm² pix ; 6pix → 2 FEI4 pix
5×5 mm² IC, **bondable to FE-I4**
Bonn / CPPM / KIT

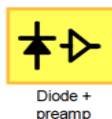
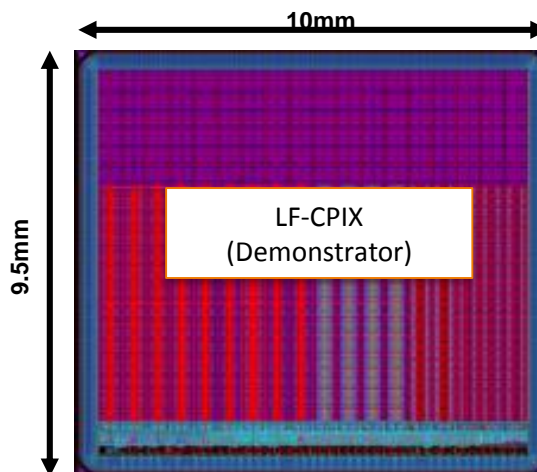


2016~2017

Large size demonstrator

LF-CPIX:

50×250μm² pix ; diff. pix flavors
10×10 mm²; 2 versions -Guard-Ring-
Bonn / CPPM / IRFU

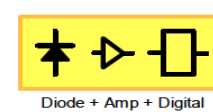
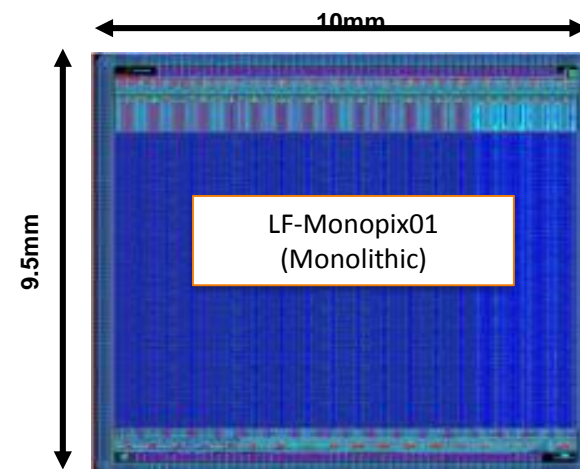


2017~Present

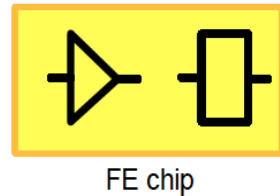
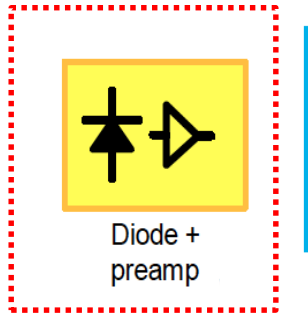
Large Monolithic demonstrator

LF-Monopix:

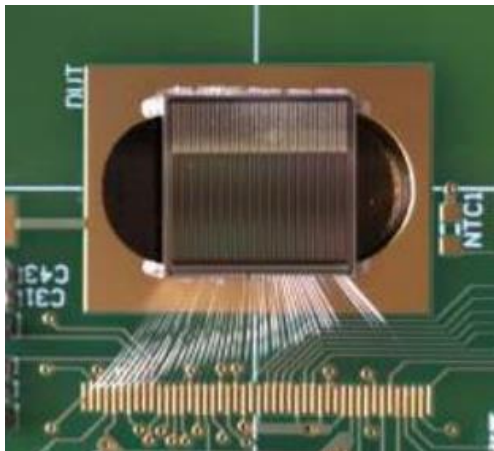
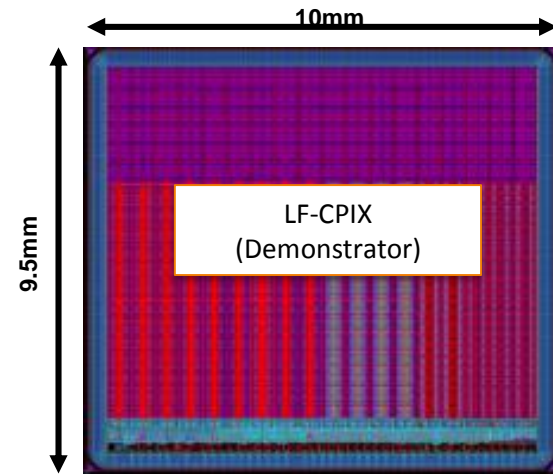
50×250μm² pix
10×10 mm² IC
1st full monolithic demonstrator!
Bonn / CPPM / IRFU



LF-CPIX



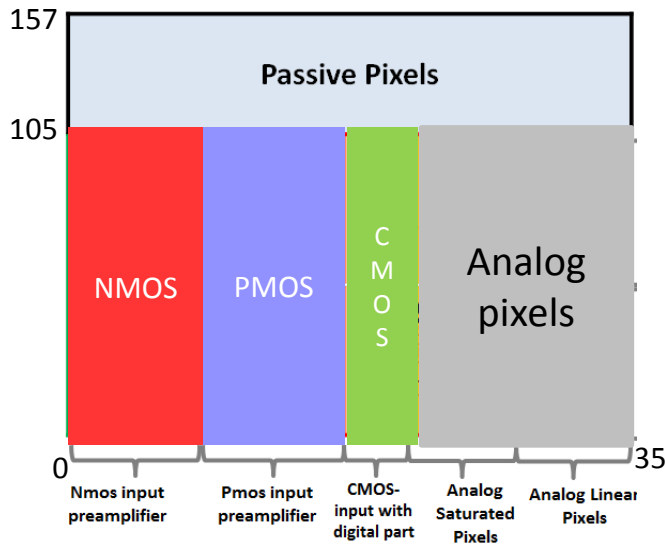
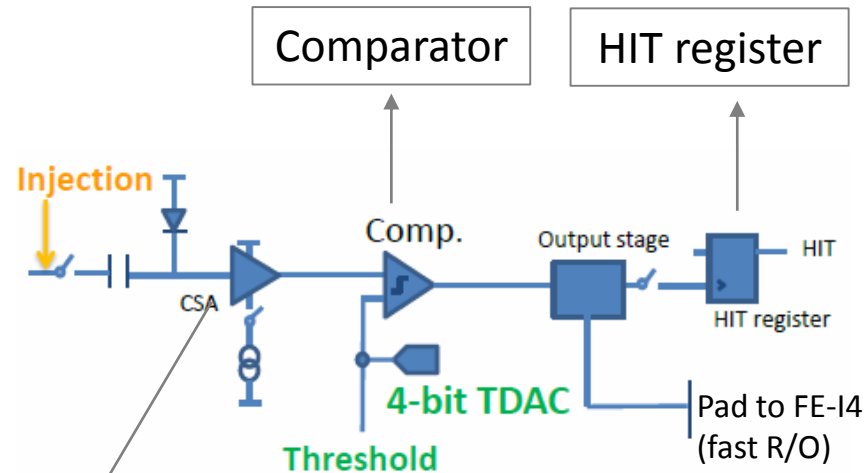
LF-CPIX:
 50×250μm² pix ; diff. pix flavors
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 Bonn / CPPM / IRFU



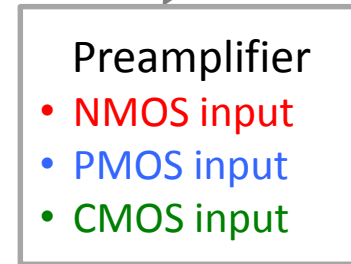
- LF-CPIX:
 - Testing of **sensor diode collection** part.
 - Testing of **analog part** of pixels.

LF-CPIX pixel and matrix architecture

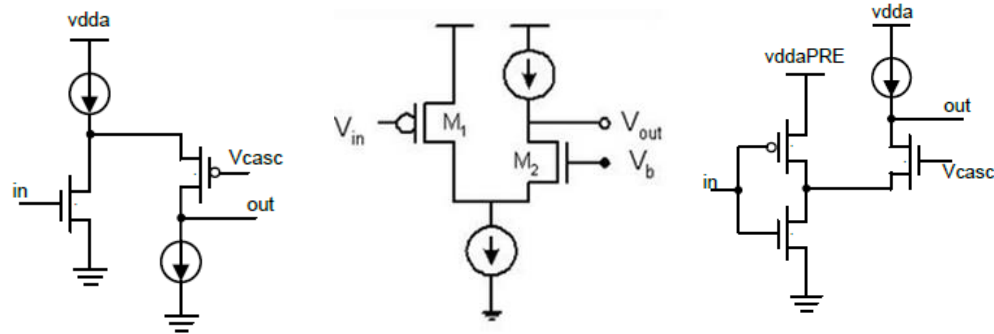
- Process: LFoundry 150 nm CMOS process.
- Wafer resistivity: >2kΩ cm.
- Pixel size: 250 μm x 50 μm (= FE-I4 readout chip size).
- Digital Matrix: 23 x 106.
- Flavor: Active pixel (3 types of CSA).



Pixel flavors in the matrix



Readout circuitry LF-CPIX



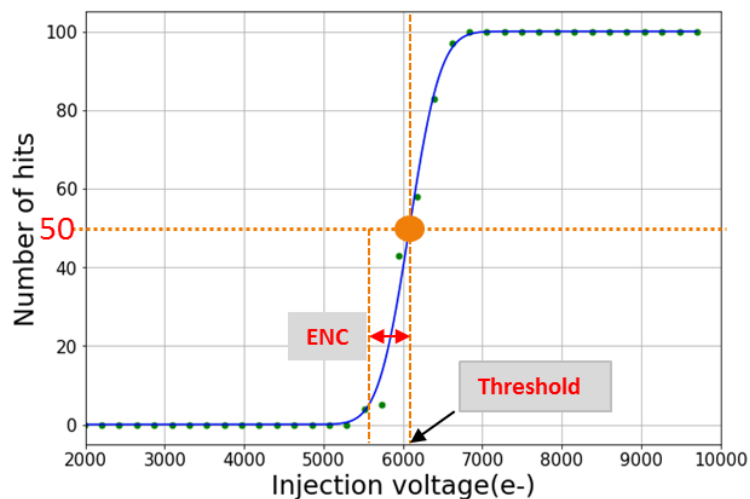
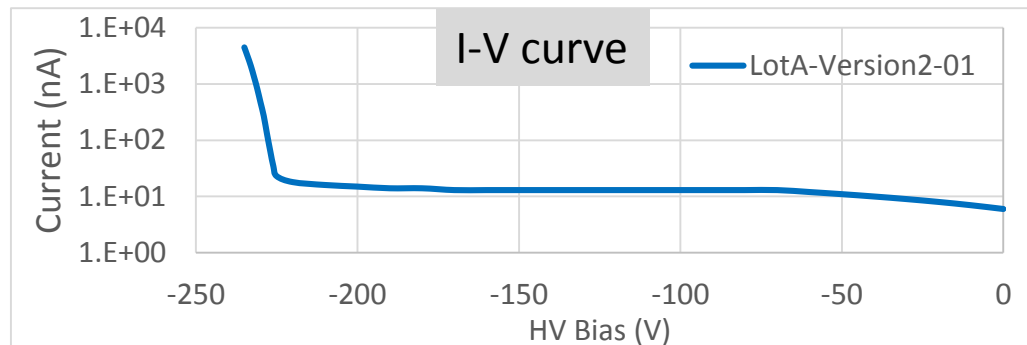
• NMOS input

• PMOS input

• CMOS input

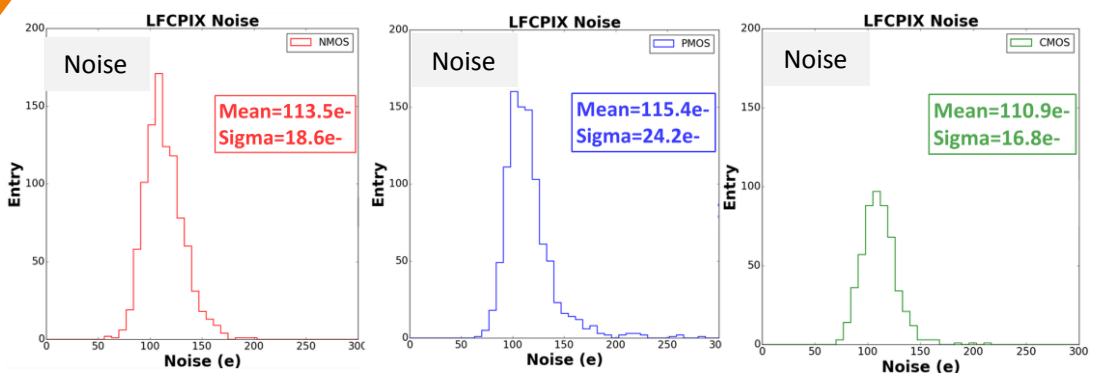
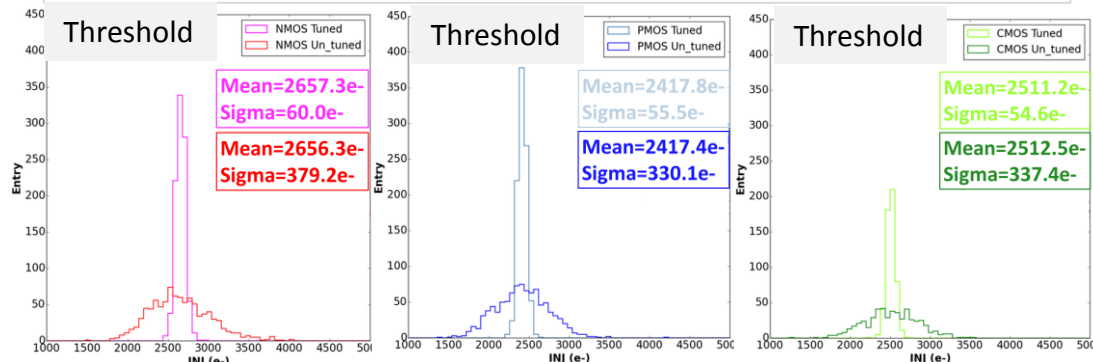
LF-CPIX: Laboratory results

- The **breakdown voltage** $\sim -220V$.
- All 3 flavors are working well and the **threshold can be tuned**, the threshold dispersion can be tuned down to **60e-**.
- Typical **noise** mean value less than **120e-**.



S-curve

- S-curve fit to extract effective threshold and noise



NMOS flavor

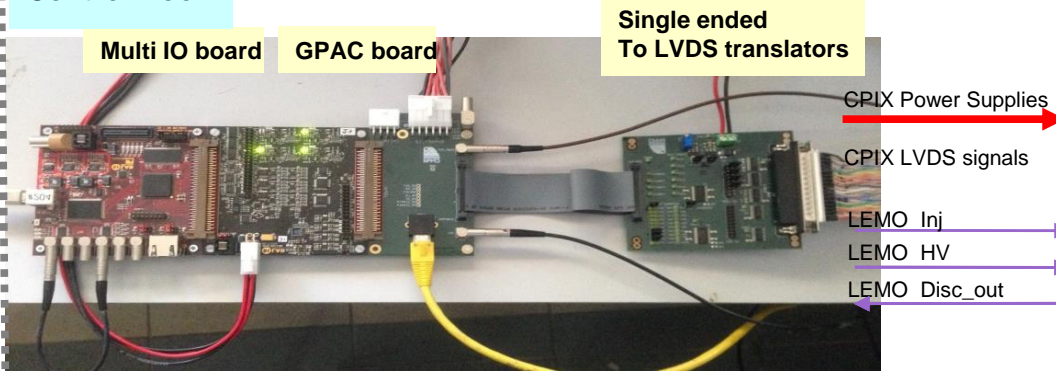
PMOS flavor

CMOS flavor

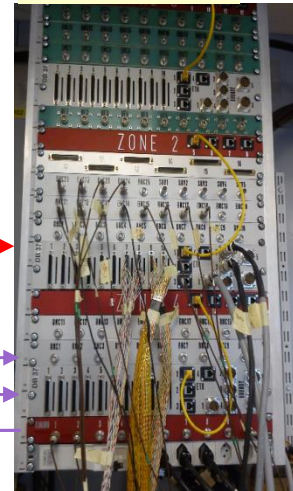
Setup under proton beam @ CERN PS

- Aug → Sep 2017 :
- 24 GeV protons irradi.
- ~150 MRad reached (roughly 2 times the dose expected for the ITk 4th layer).
- Fluence: $1.71 \times 10^{15} n_{eq}/cm^2$.

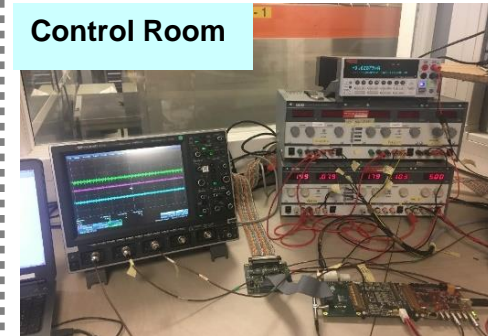
Control Room



Control Room Patch Panel

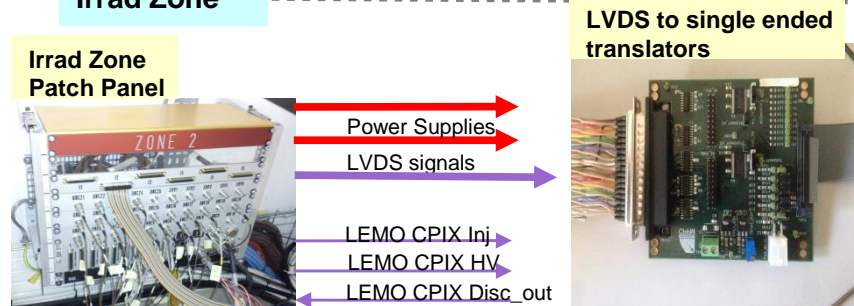


Control Room



distance of 20m

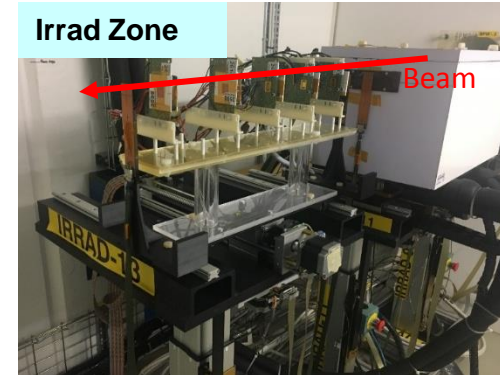
Irrad Zone



DUT board LFCPIX



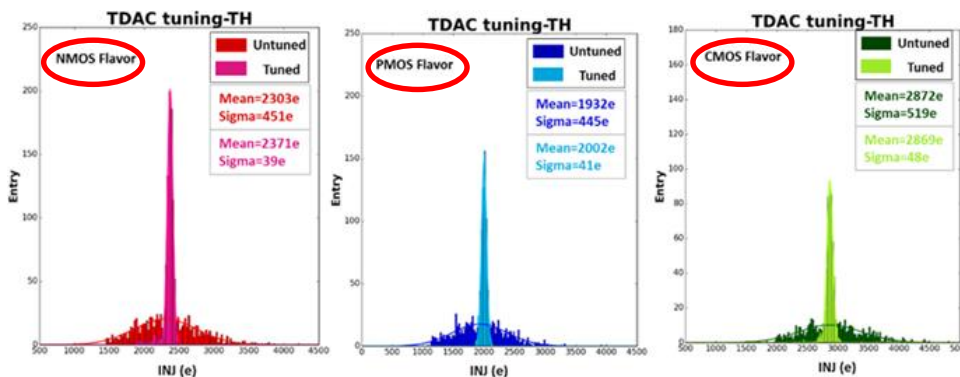
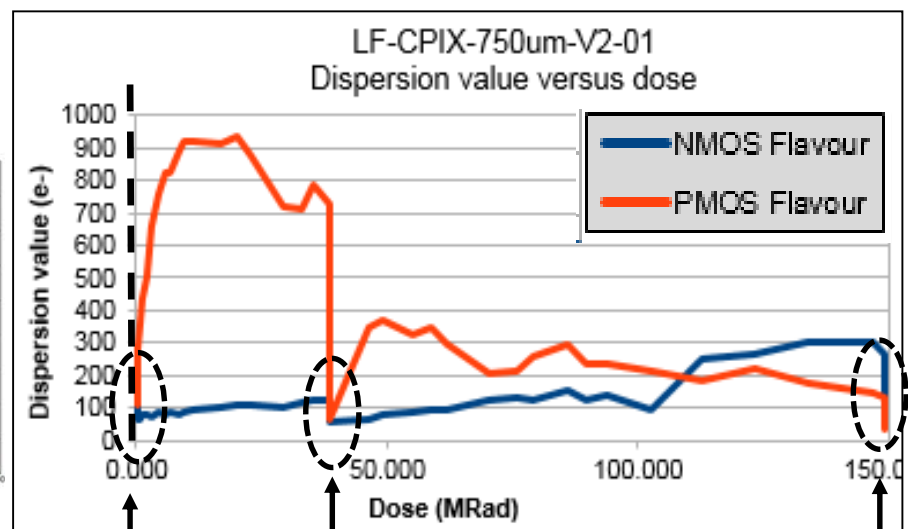
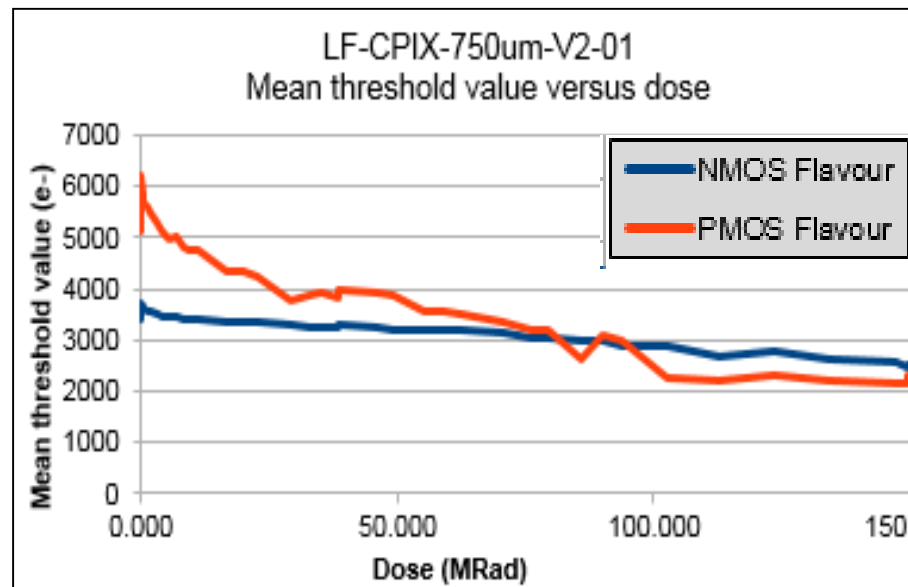
Irrad Zone



Threshold Dispersion vs. Dose

PS irradiation → 150 MRad

- The threshold mean value for the 3 flavors are **2000e-** after proton beam irradiation up to 150MRad.
- The threshold dispersion for the 3 flavors can be tuned to less than **50e-** after proton beam irradiation up to 150MRad.



Threshold scan and tuning after radiation

Initially tuned @ 0 MRad

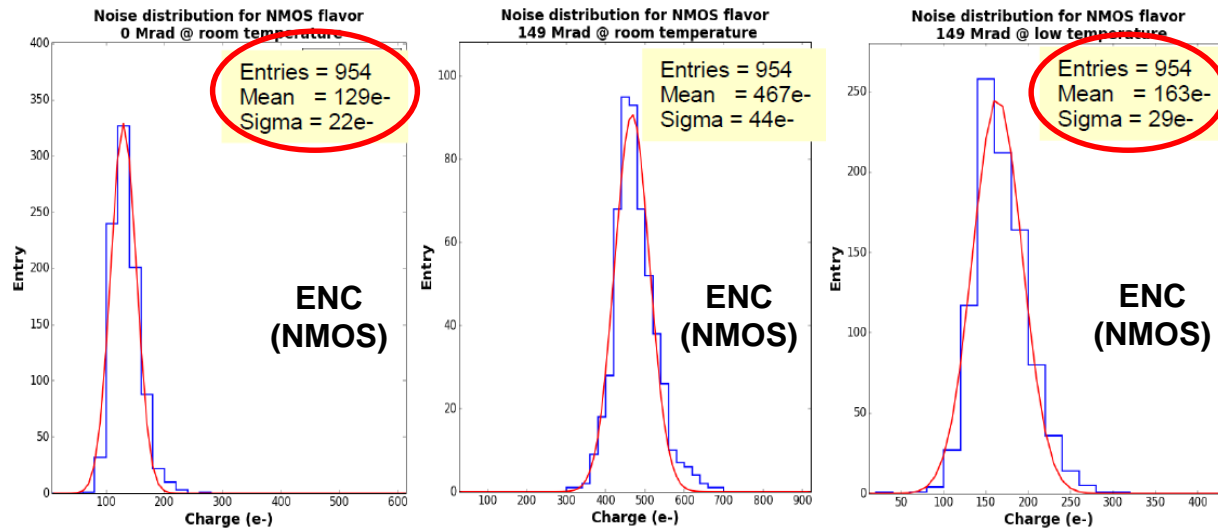
Retuned @ 38 MRad

Retuned @ 149 MRad

Noise after 150 Mrad proton beam irradiation

PS irradiation → 150 MRad

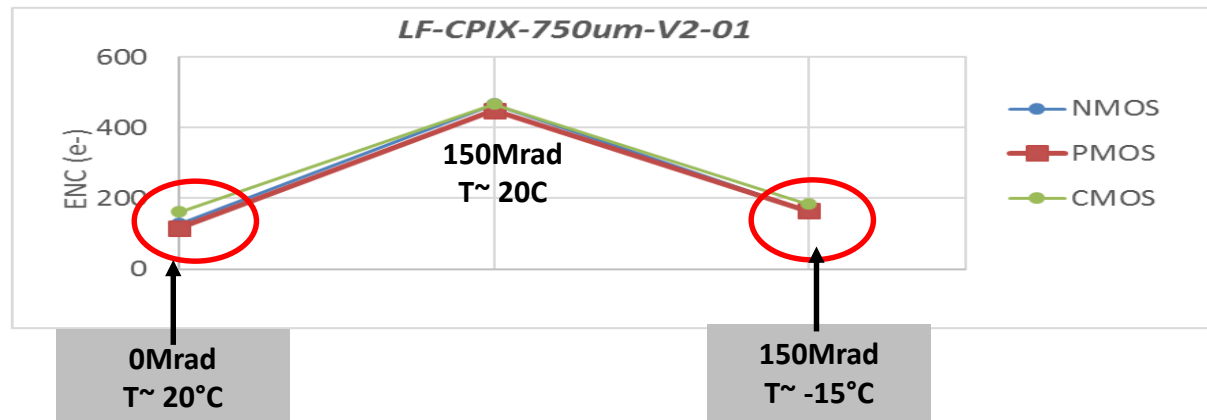
- The noise mean values for all flavors are **less than 200e-** at low temperature after proton beam irradiation up to 150Mrad.



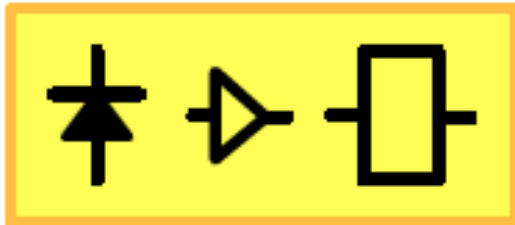
Pre-rad T~ 20°C

150 Mrad T~ 20°C

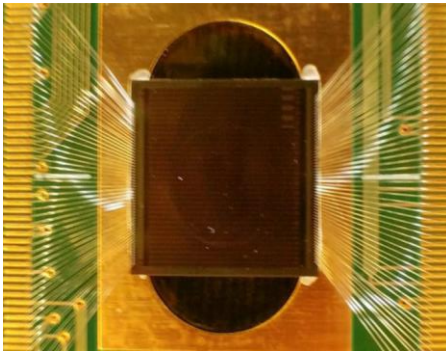
150 Mrad T~ -15°C



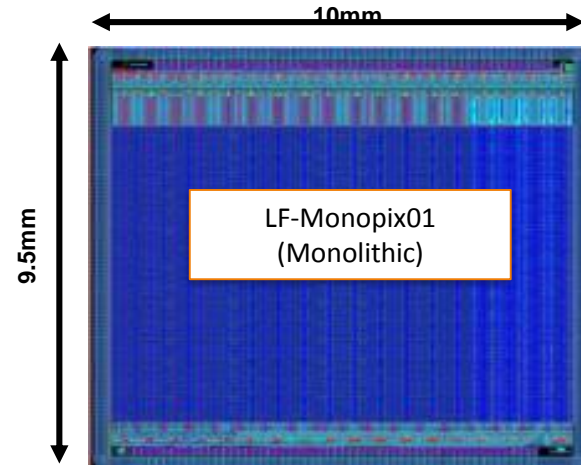
LF-Monopix



Diode + Amp + Digital

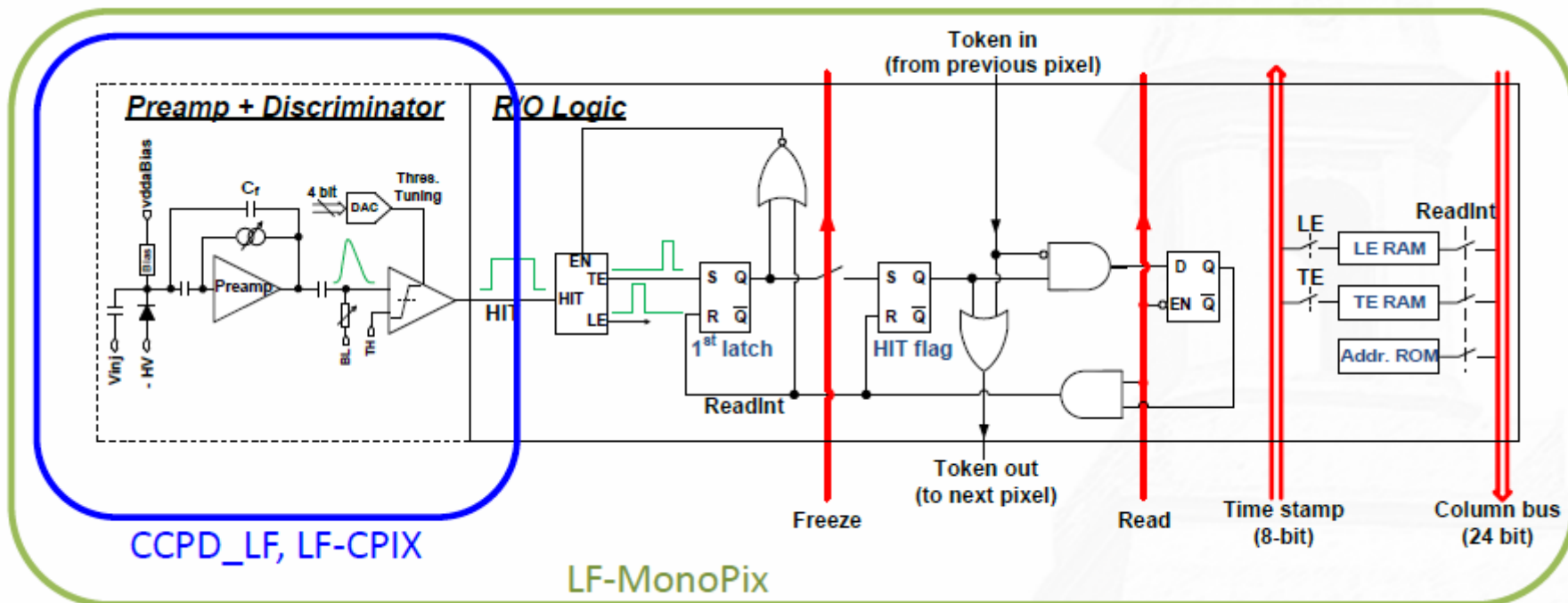


LF-Monopix:
 $50 \times 250 \mu\text{m}^2$ pix
 $10 \times 10 \text{ mm}^2$ IC
1st full monolithic demonstrator!
 Bonn / CPPM / IRFU



- LF-Monopix:
 - 1st **full monolithic** concept.
 - 1st test of the **digital architecture**.

LF-Monopix: Pixel design

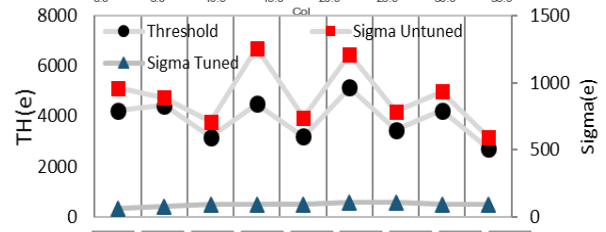
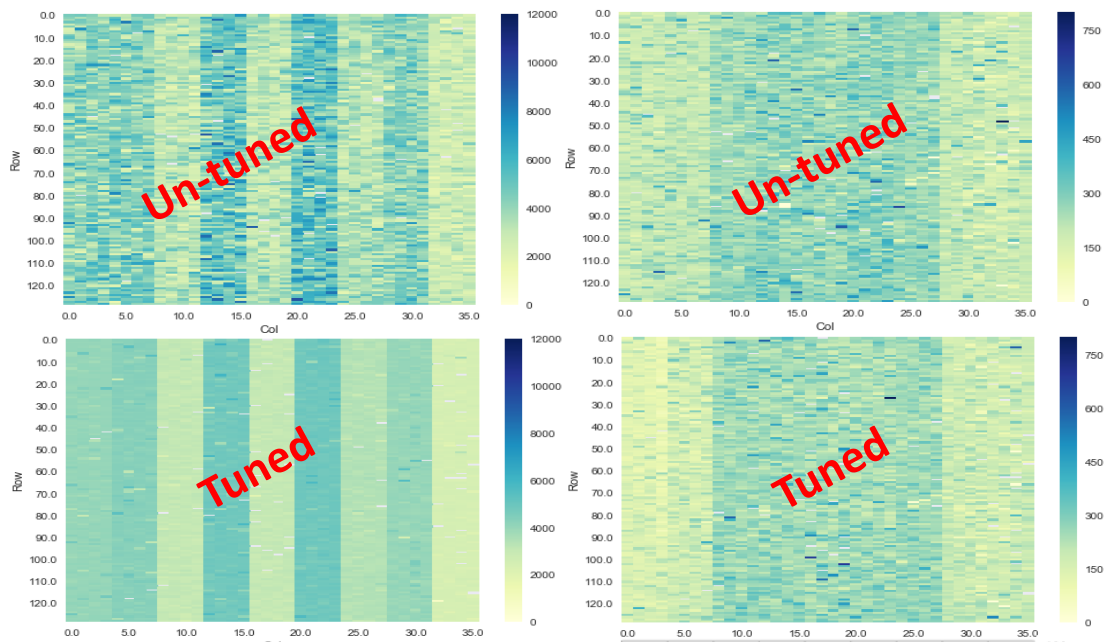
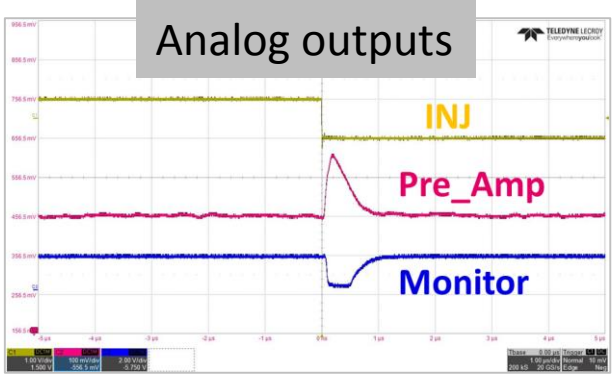
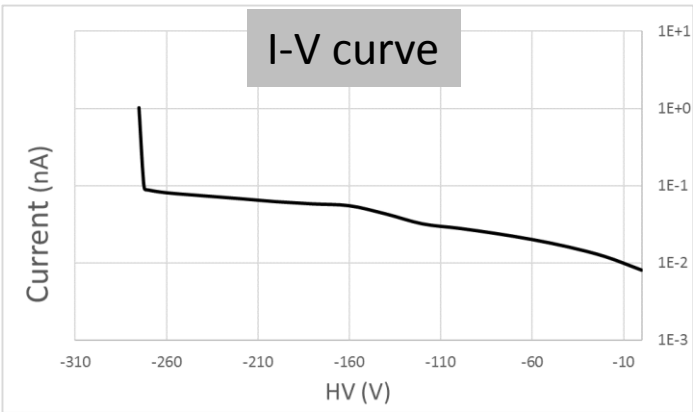


- 150nm CMOS process, LFoundry (Resistivity >2kΩ.cm).
- **Similar diode and analog** front end circuitry design **as in LF-CPIX**.
- 129 x 36 pixel array (**9 sub matrices** with different pre-amplifiers, discriminators, R/O concepts ...).
- **Column-drain R/O logic (FE-I3 like)**.
- 40 MHz (up to 160MHz by design) LVDS serial output.

Flavor No	1	2	3	4	5	6	7	8	9
R/O logic	Out		In-Pixel						
Amplifier	CMOS							NMOS	
Discriminator	V2	V1	V2	V1	V2	V1	V2	V1	
Discriminator Domain	Dig		A+D		Dig		A+D		
Token	CMOS				Current Steering				
Source Follower	P	N							

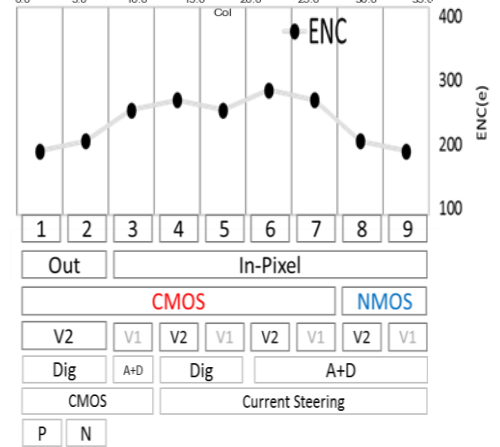
LF-Monopix: Laboratory results

- Breakdown $\sim -280\text{ V} \Rightarrow$ up to $\sim 300\ \mu\text{m}$ depletion.
- The threshold and dispersion can be tuned down to 2000e^- and 100e^- respectively.
- The typical noise $\sim 200\text{e}^-$.



Flavor No	1	2	3	4	5	6	7	8	9
R/O logic	Out	In-Pixel							
Amplifier	CMOS				NMOS				
Discriminator	V2	V1	V2	V1	V2	V1	V2	V1	
Discriminator Domain	Dig	A+D	Dig		A+D				
Token	CMOS				Current Steering				
Source Follower	P	N							

Threshold mapping

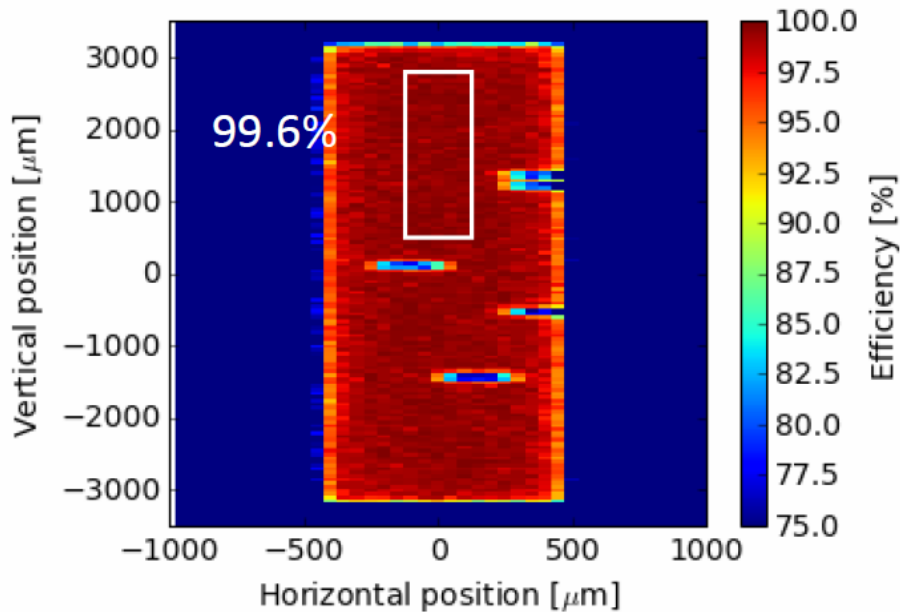


Noise mapping

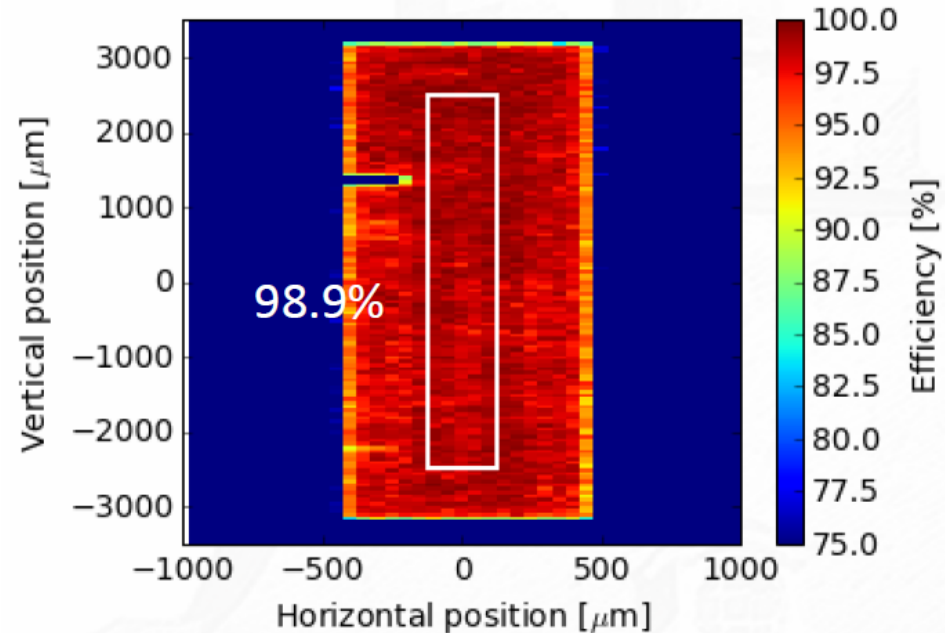
LF-Monopix: Efficiency under ELSA test beam

- ELSA beam:
 - 2.5GeV electron
 - Nov 8-10, 2017

T. Hirono, Bonn



Un-irradiated chip



Neutron irradiated (NIEL= 10^{15} neq/cm²)

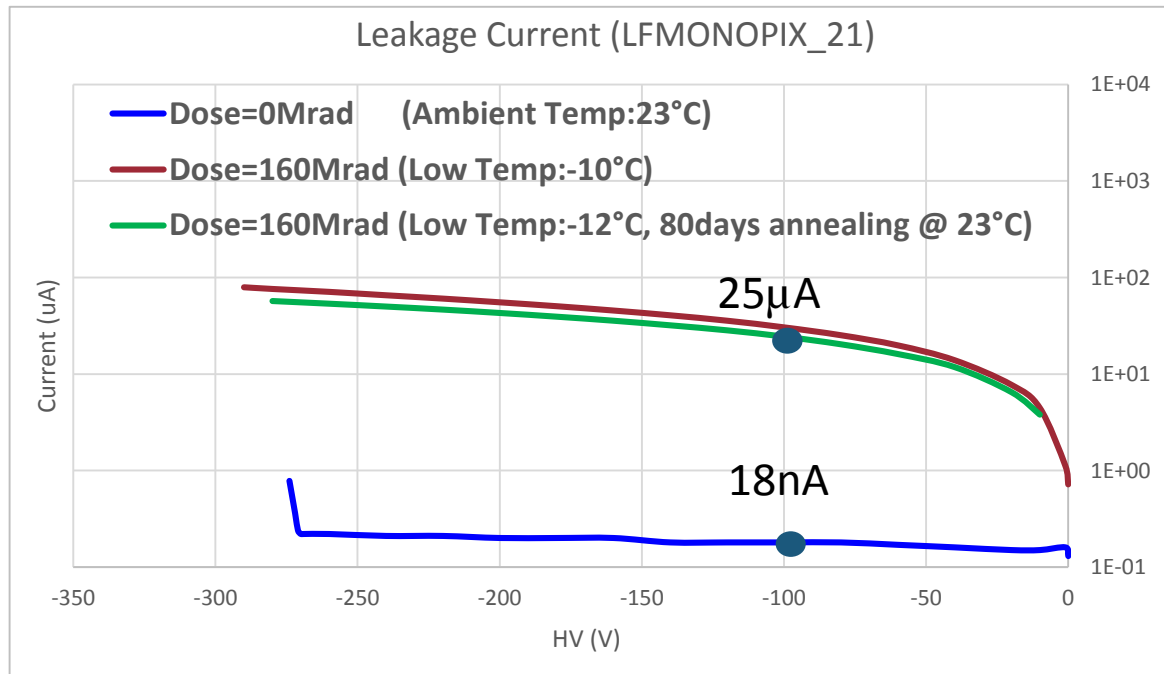
Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix
 DAC setting: default
 HV: -200V
 Temp: -25°C
 Beam: 2.5GeV electron

Flavor: CMOS-CSA, V1-D-Discr. Curr-Token In-pix
 DAC setting: default
 HV: -130V
 Temp: -25°C
 Beam: 2.5GeV electron

Leakage Current (LF-Monopix)

Proton beam @ CERN PS

- The set-up was similar to the one of LF-CPIX
- June → Sep 2018 :
- 24 GeV protons irradiad
- ~160 MRad reached (roughly 2 times the dose expected for the 4th layer)

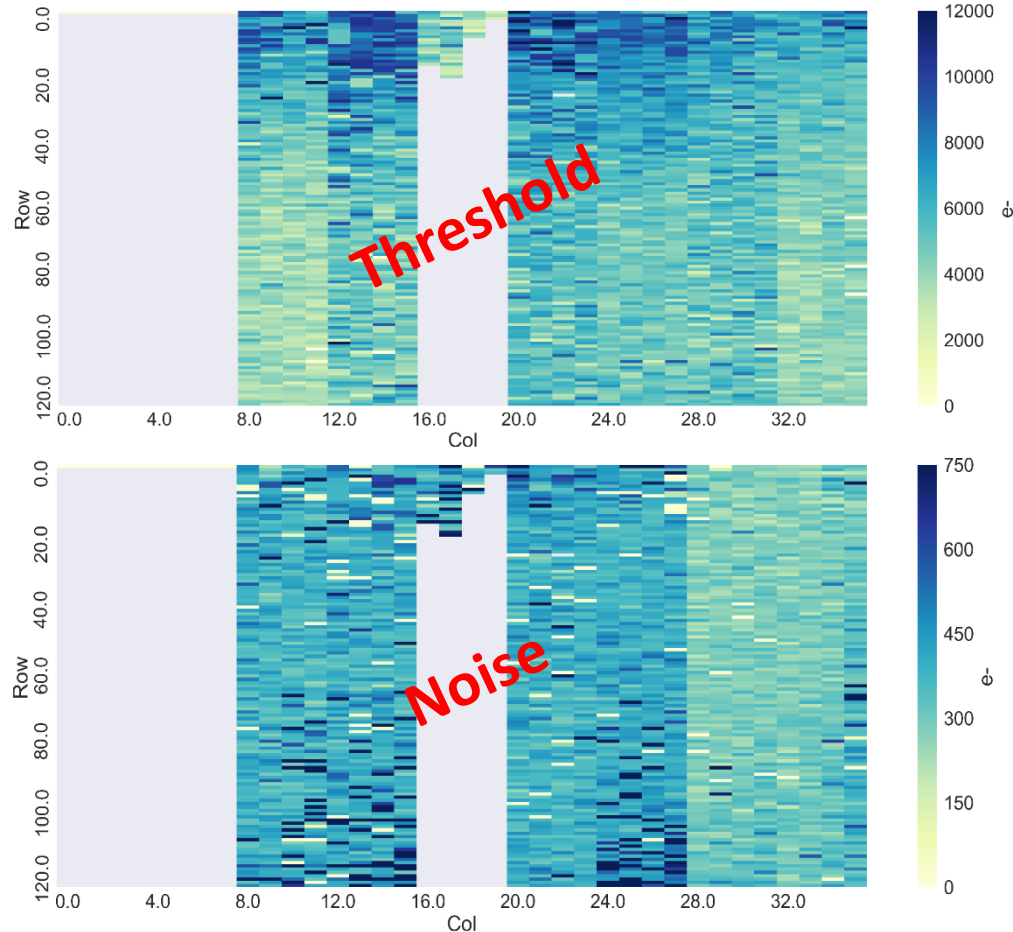
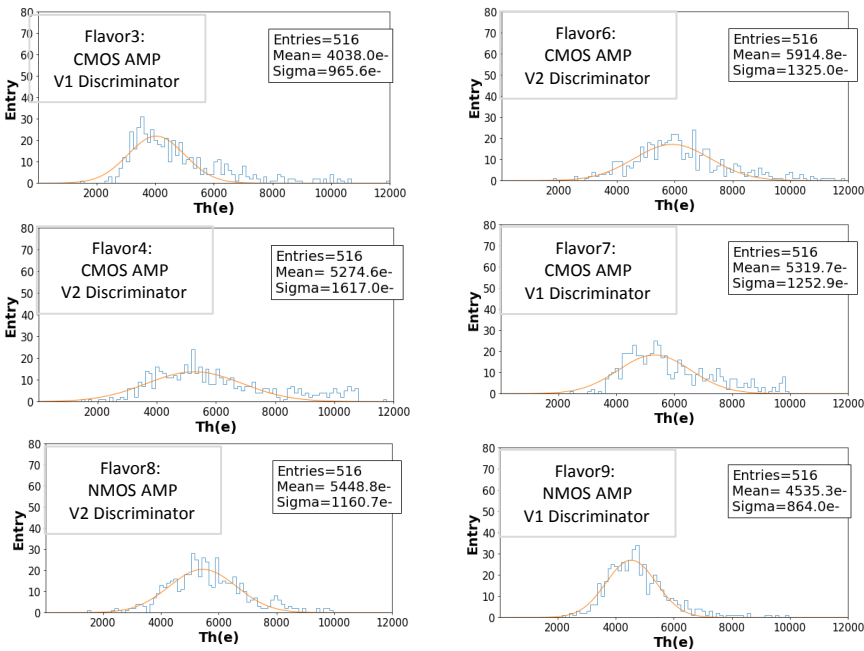


IV Curves

The leakage current increase after irradiations seems acceptable

Threshold scan after 160Mrad proton irradiation

- Low Temp:-12°C
- 80days annealing @ 23°C



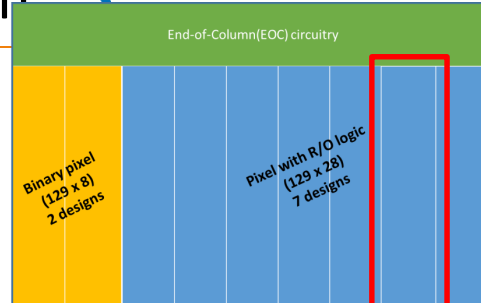
Threshold histograms for 6 flavors

Flavor No	1	2	3	4	5	6	7	8	9
R/O logic	Out		In-Pixel						
Amplifier	CMOS						NMOS		
Discriminator	V2	V1	V2	V1	V2	V1	V2	V1	
Discriminator Domain	Dig		A+D	Dig		A+D			
Token	CMOS			Current Steering					
Source Follower	P	N							

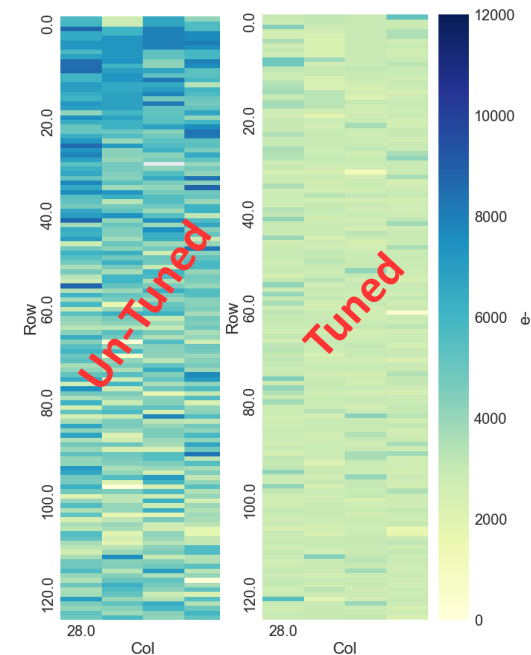
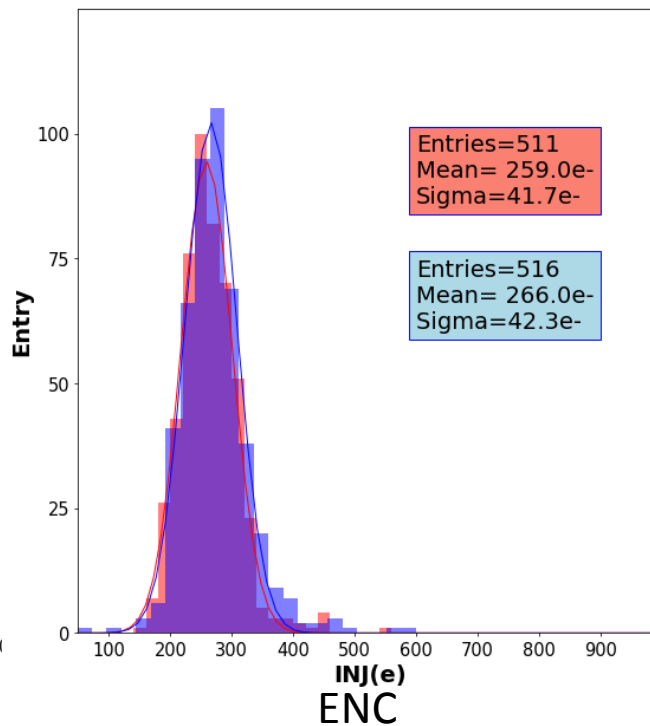
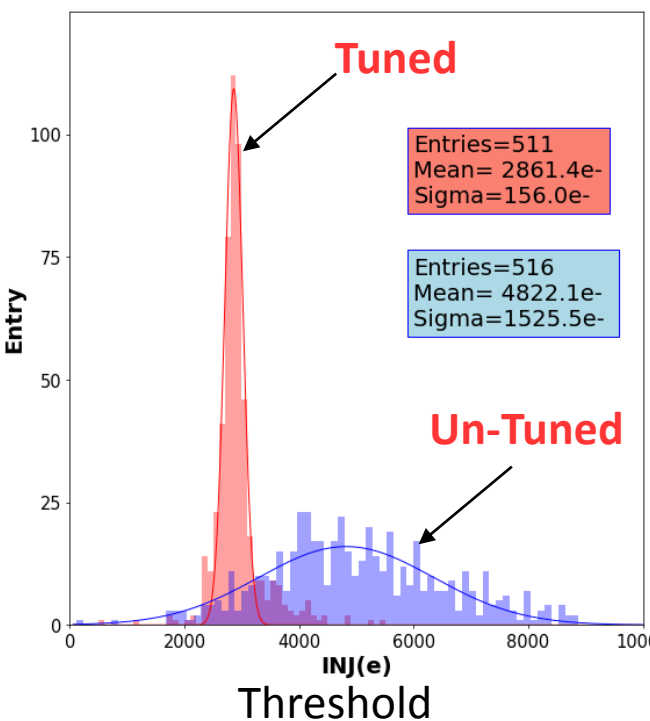
Threshold tuning after 160Mrad proton irradiation

- Flavor8: NMOS AMP+ V2 Discriminator
- TH=0.80V, Temp:-12°C,HV=-40V, 80 days room temperature annealing.
- After tuning, the flavor8 could be tuned to target **thresholds (~2800 e-)** with a **dispersion 156e-**.

End-of-Column(EOC) circuitry



Flavor No	1	2	3	4	5	6	7	8	9
R/O logic	Out		In-Pixel						
Amplifier	CMOS							NMOS	
Discriminator	V2	V1	V2	V1	V2	V1	V2	V1	V2
Discriminator Domain	Dig	A+D	Dig			A+D			
Token	CMOS		Current Steering						
Source Follower	P	N							



Conclusion & outlook

- Promising results of **LF-CPIX** were shown in terms of:
 - **Good breakdown voltage** characteristics (BV below -200V).
 - **Radiation hardness** of the technology:
 - Tuning of all the 3 flavors possible (threshold dispersion < 50e).
 - **Limited noise increase after 150 Mrad** (noise < 200e).
- **LF-Monopix**: fully functional demonstrator chip with column drain readout.
 - **Good breakdown voltage** characteristics (BV below -270V).
 - **Limited threshold dispersion** (can be tuned within 110e~148e depending on flavor).
 - **ENC** for different flavors is between 190e- to 280 e-.
 - **Good irradiation** performances:
 - **High efficiency ~99% after 1×10^{15} neq/cm².**
 - **Limited leakage current increase after 160MRad.**
 - After 160 Mrad proton irradiation, **tuning down to 2860e- with a dispersion 156e-.**
- **Next step and Outlook.**
 - Need to understand the radiation effect on different parts of the chip.
 - Need to reduce the pixel size and leakage current (layout optimization).
 - Based on the results of the LF-MONOPIX, find best strategy for the next demonstrator.

The collaboration works on an improved full size LF CMOS prototype that could be used in ATLAS ITk layer 4 → target: submission in 2019

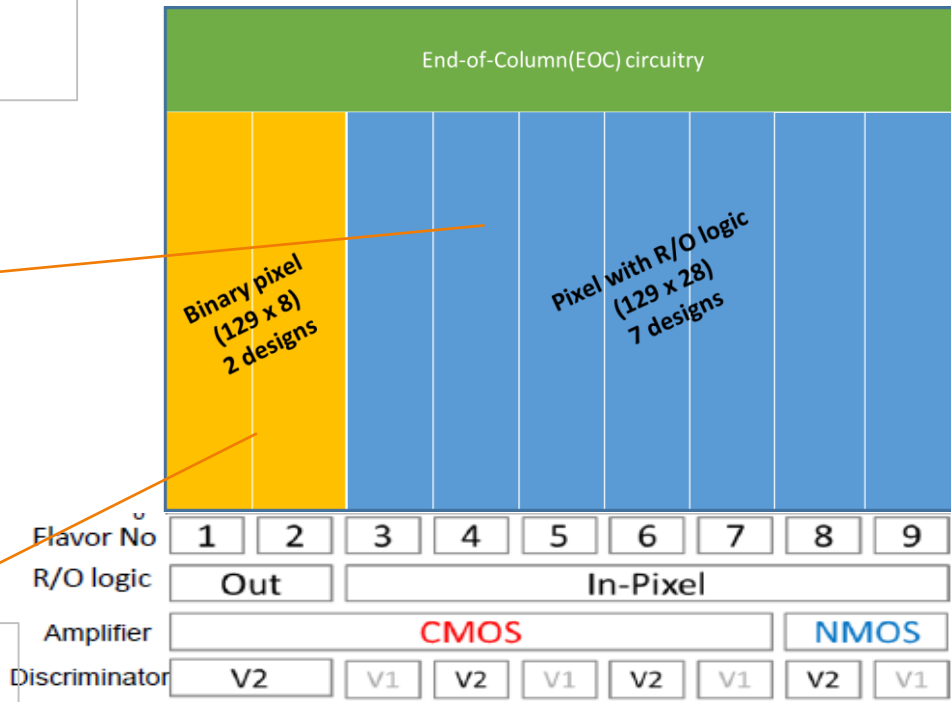
Thanks for your attention!

General description of the LF-MONOMPIX

- 150nm CMOS (Resistivity >2 kOhm-cm)
- **129 x 36** pixel array
- 40 MHz (160MHz by design) LVDS serial output

- 7 flavors with “in-pixel” R/O logic: NMOS or CMOS amplifier, “V1” or “V2” discriminators, current steering or CMOS token transmission.

- 2 flavours with off-matrix(“external”) R/O logic: CMOS amplifier, “V2” discriminator, NMOS or PMOS source followers.



Calibration of the capacitance (LF-Monopix)



Calibration of the Capacitance Setup

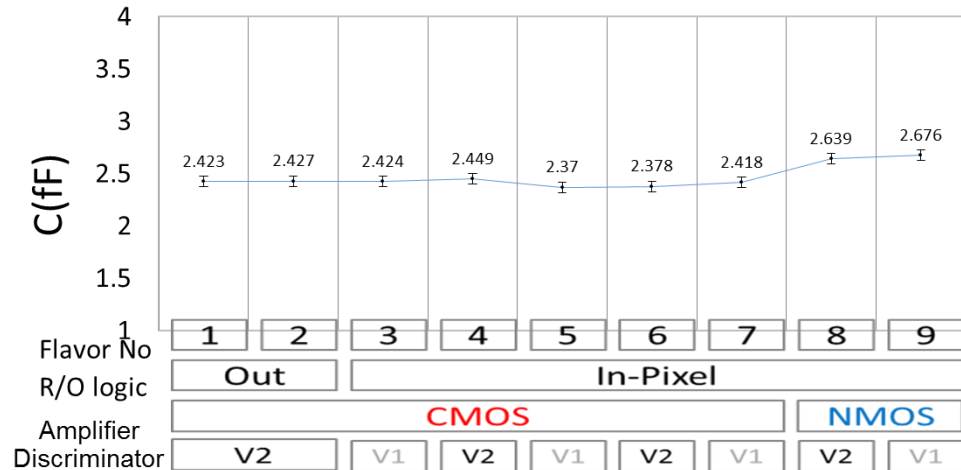
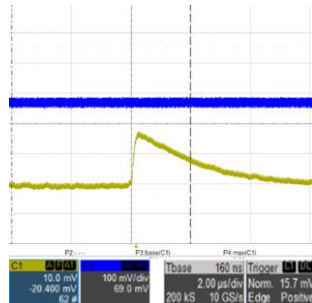
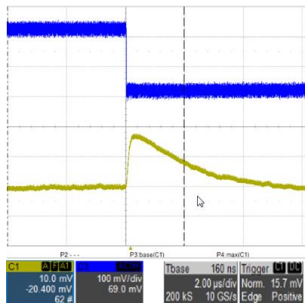
$$C_{inj} = Q/V = N * e / V$$

C_{inj} : Injection Capacitance

N : Number of ⁵⁵Fe electrons (1619e⁻)

e : elementary charge

V : external injection



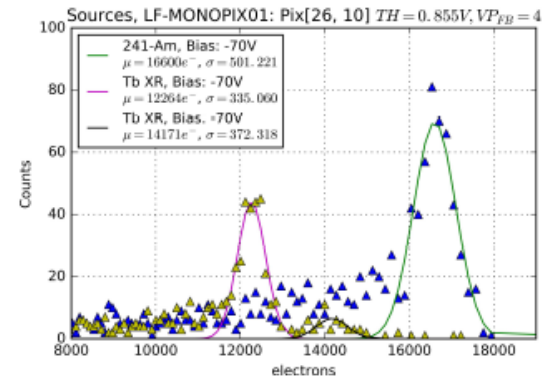
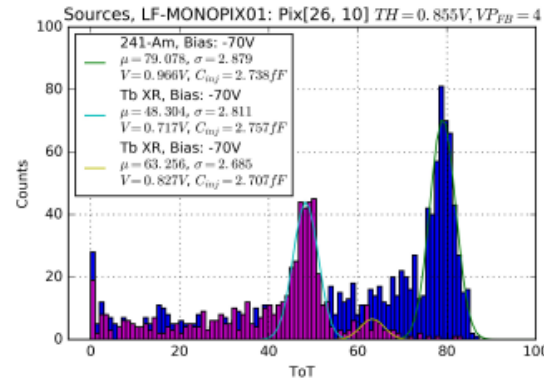
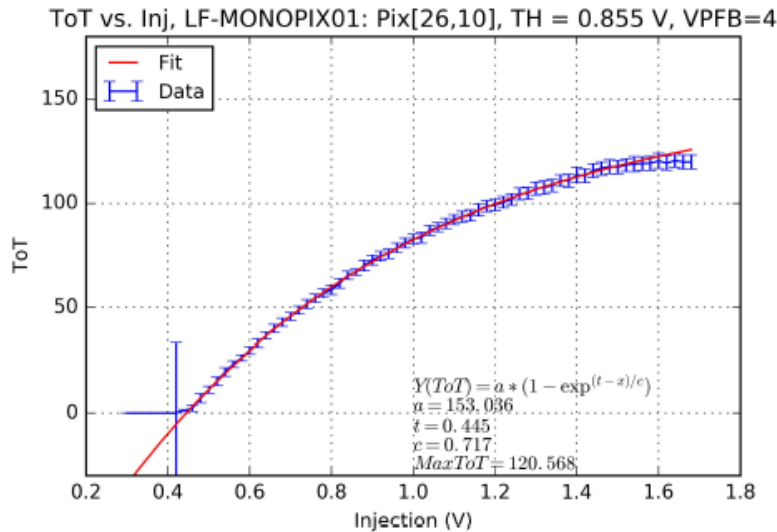
External Injection

55Fe Source Signal

Determination of Injection Capacitance

-> Injecting charge directly to the pre-amplifier.

+ **Low feedback voltage (VPFB): Longer ToT**
(sampling with **higher resolution**)



(Assuming 3.6 eV/e-)

²⁴¹Am:

16539 e-

Tb X-rays:

K $_{\alpha}$ 12353 e-

K $_{\beta}$ 13997 e-

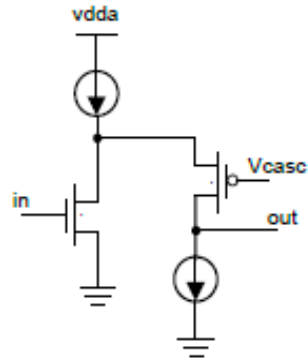
$$C_{inj} = Q / V \sim 2.75 \text{ fF}$$

Resolution:

(1175 e-) 4.2 keV FWHM
(For ²⁴¹Am x-rays)

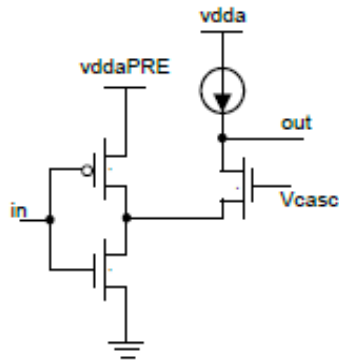
LF-Monopix01: Pixel design

- Pre-amplifiers => aimed at peaking time $\lesssim 25$ ns with 400 fF C_d
 - NMOS input: modified from LF-CPIX in order to deal with the increased C_d

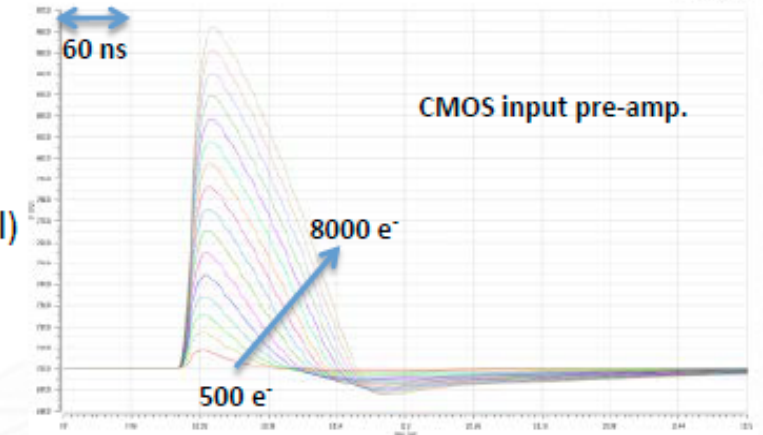
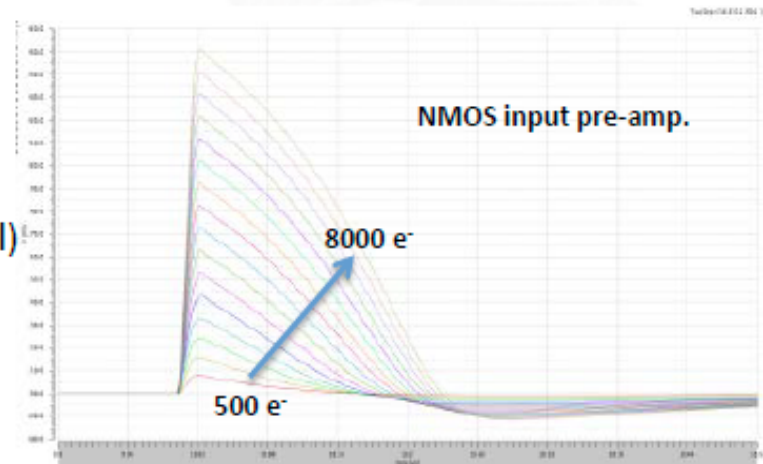


- Bias current $\sim 17 \mu\text{A}$
- peaking time ~ 20 ns (4 ke⁻ signal)
- ENC $\sim 170 e^-$

- CMOS input: same as LF-CPIX

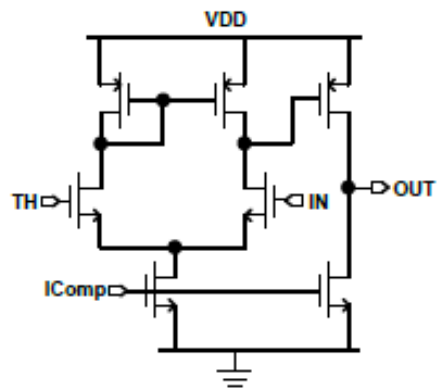


- Bias current $\sim 15 \mu\text{A}$
- peaking time ~ 25 ns (4 ke⁻ signal)
- ENC $\sim 135 e^-$



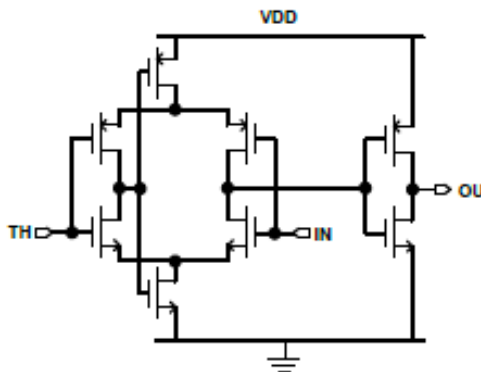
LF-Monopix01: Pixel design

- Discriminator => influence on the time walk
 - Discriminator V1: same as LF-CPIX

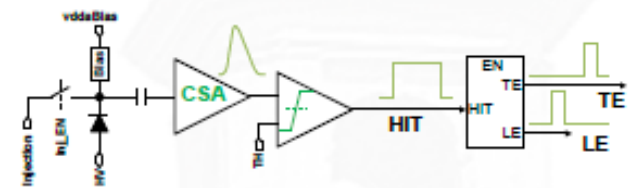


- 2-stage amplifier as comparator
- bias current: 4.5 μA
- slow at threshold edge

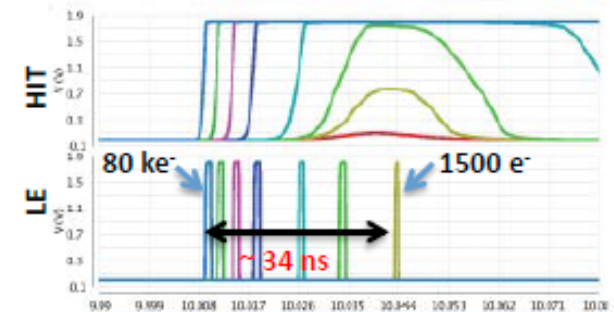
- Discriminator V2:



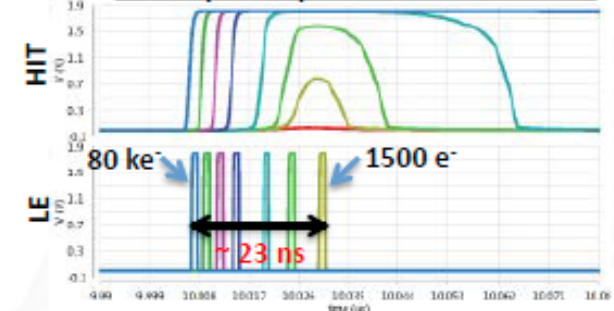
- Two amplifiers load each other
- self biased: < 4 μA
- CMOS inverter as 2nd stage



NMOS pre-amp. + Dis. V1, TH=1500e⁻

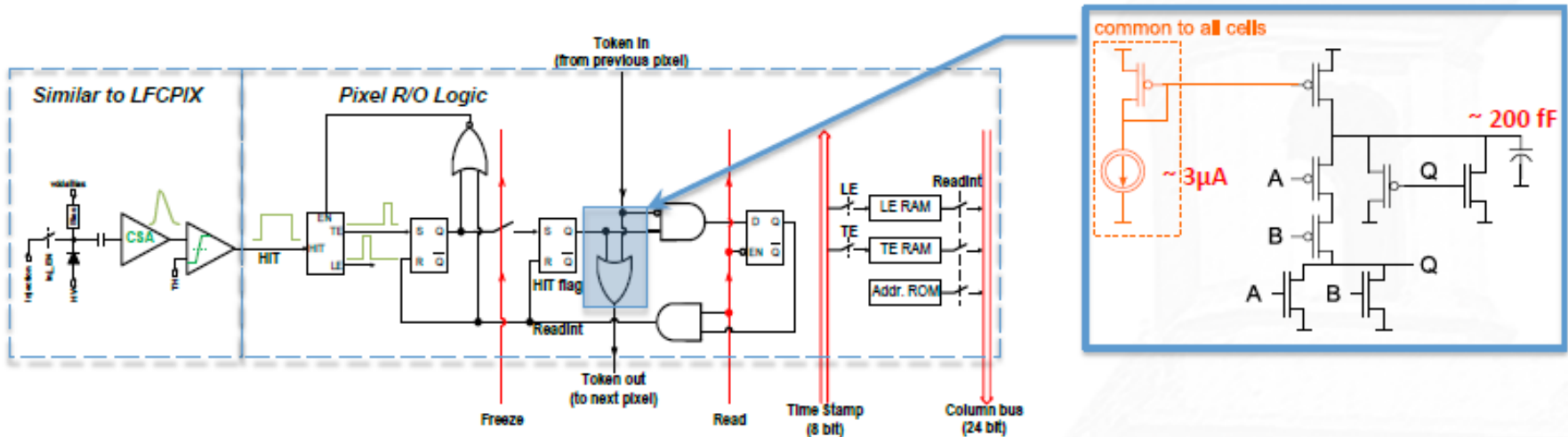


NMOS pre-amp. + Dis. V2, TH=1500e⁻

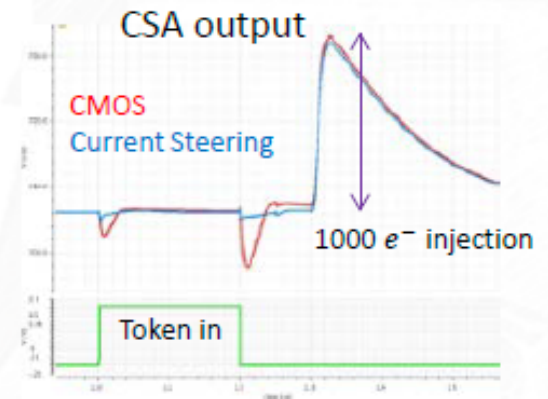


LF-Monopix01: Pixel design

- Low noise is critical for some digital blocks

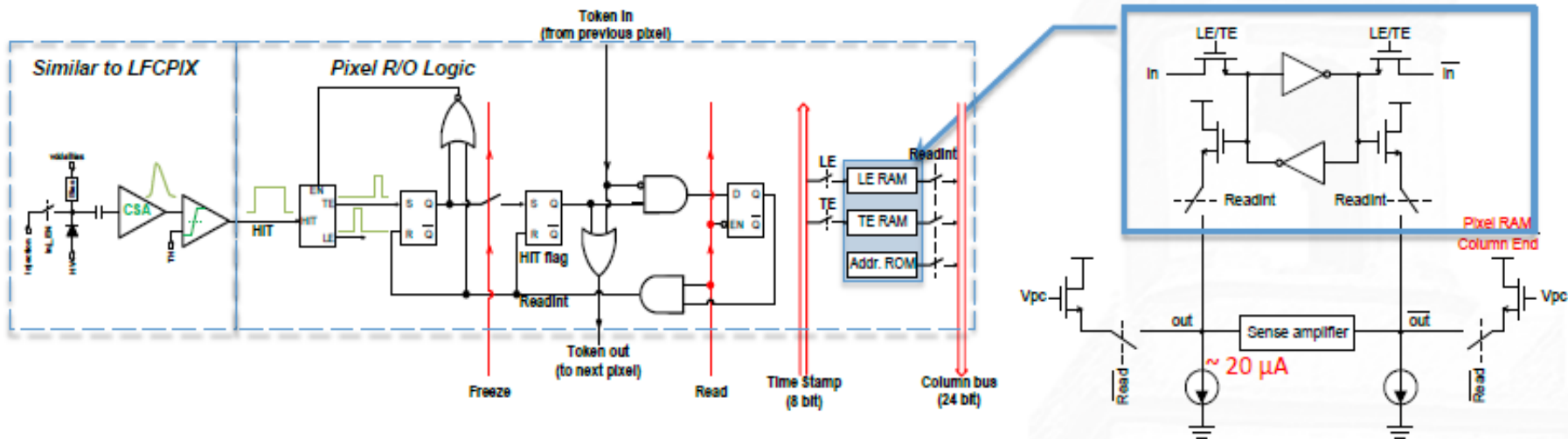


- Token propagates while pixels are sensitive
 - Current Steering (CS) logic
 - => constant current => less noise



LF-Monopix01: Pixel design

- Low noise is critical for some digital blocks



- Data R/O with source follower
=> avoids high current injection into the PW during high to low transition
- SF bias at column end $\sim 20\mu\text{A}$
 - 24 pairs per column => LE, TE, Addr.

