Characterization of the MPA prototype,
a 65 nm pixel readout ASIC with on-chip quick transverse momentum discrimination capabilities.

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Mykyta Haranko
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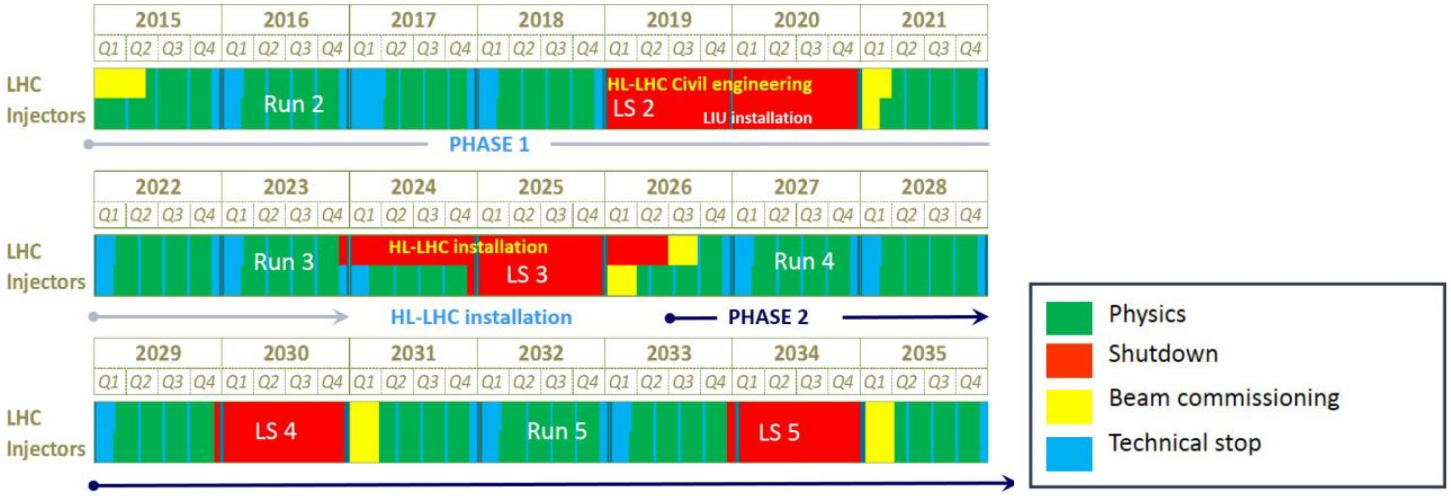
TWEPP 2018 Topical Workshop on Electronics for Particle Physics

18th September 2018

High Luminosity LHC

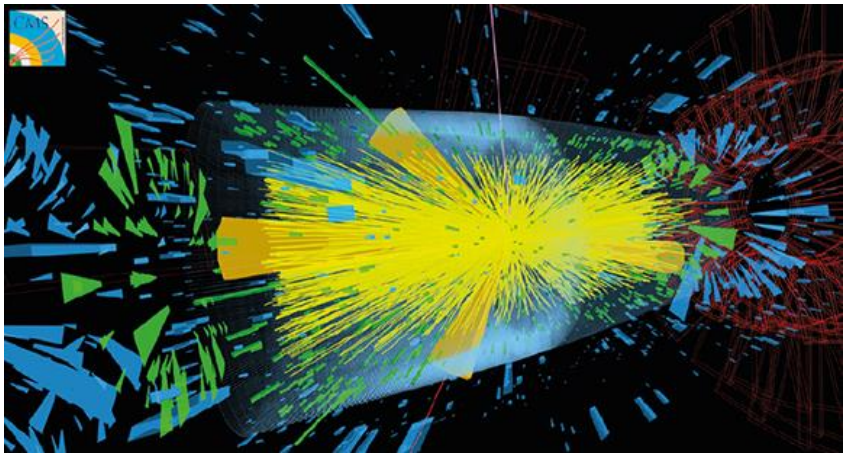
10x the nominal luminosity
up to 200 collision every 25 ns.

Major upgrades to the LHC experiments are necessary



CMS Outer Tracker upgrade

200 pile-up event



40 MHz Bunch Crossing rate

Phase-II upgrade of CMS Outer Tracker requirements:

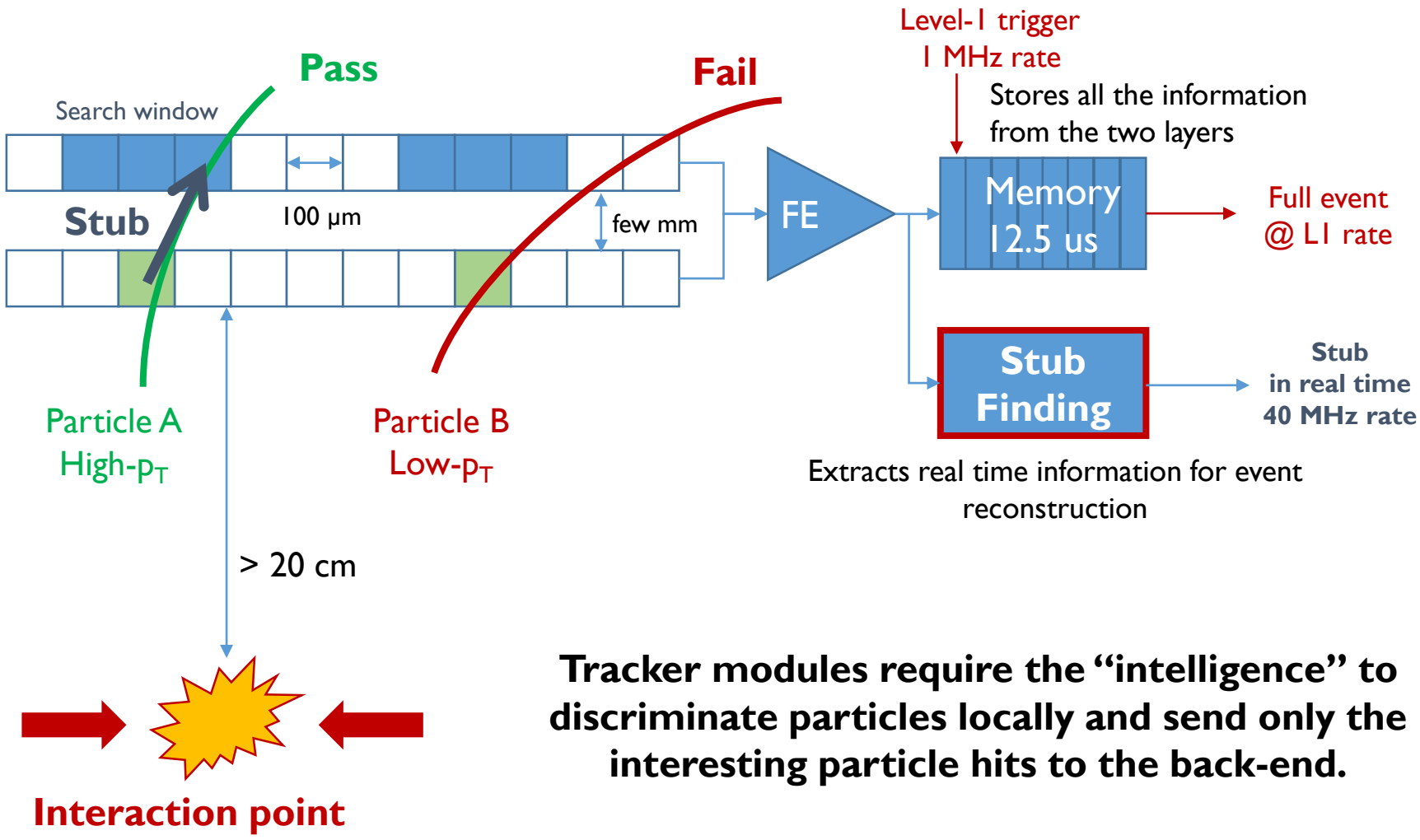
- Increase granularity
- Increase radiation tolerance
- ***Participate in the L1 trigger***
- Improve trigger performance
- Reduction of material budget

Tracker module requirements:

- Introduction of a pixelated sensor
- Radiation tolerance up to 100 Mrad
- ***Quick and on-chip particle discrimination***
- Higher trigger rate and longer latency
- Power density < 100 mW/cm^2

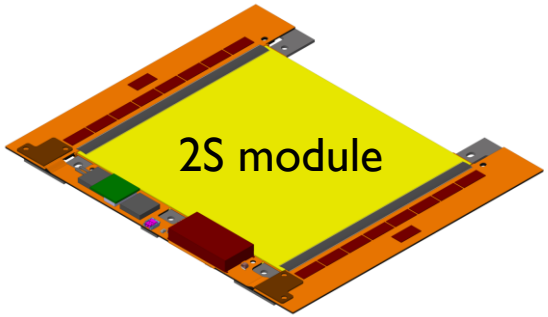
Need to reduce data for L1 trigger

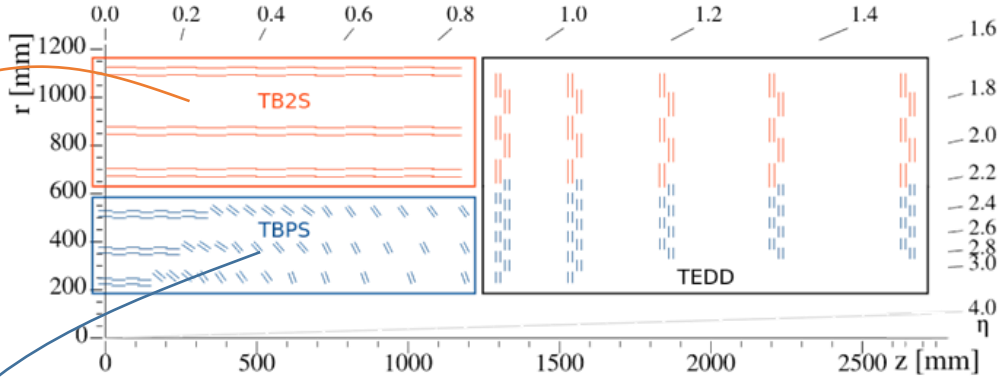
CMS Outer Tracker p_T module concept



Tracker modules require the "intelligence" to discriminate particles locally and send only the interesting particle hits to the back-end.

CMS Outer Tracker layout



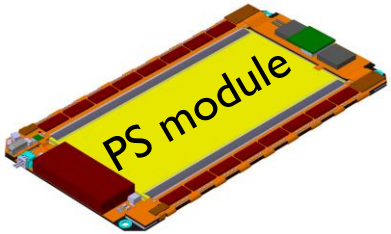


2S module
$\sim 2 \times 90$ cm^2 active area
2×1016 strips: ~ 5 cm $\times$ 90 μm
2×1016 strips: ~ 5 cm $\times$ 90 μm
Front-end power ~ 5 W
Sensor power ($-20\,^{\circ}$C) ~ 1.0 W

# of Modules = 13296

# of channels = 44 M strip + **174 M pixels**

Silicon Area ~ 200 m^2

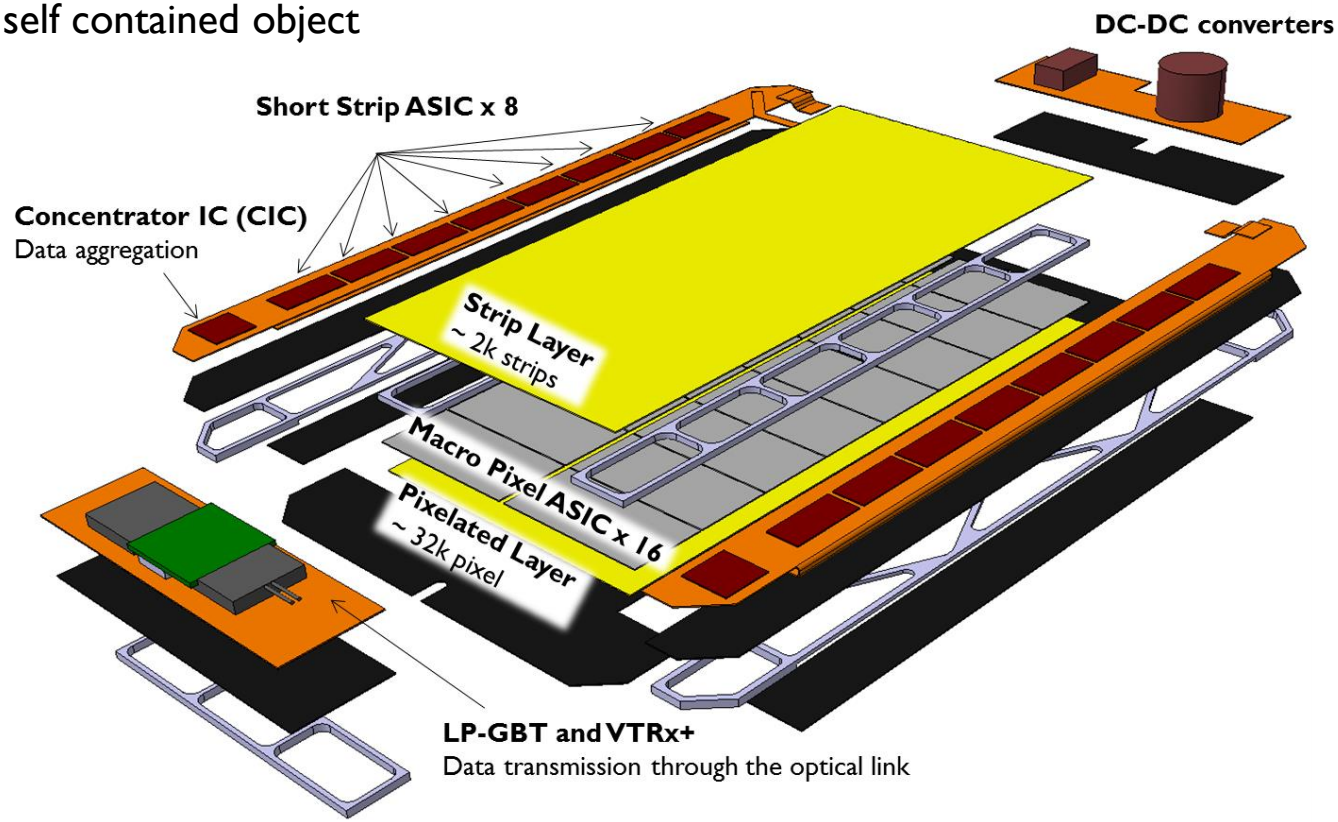


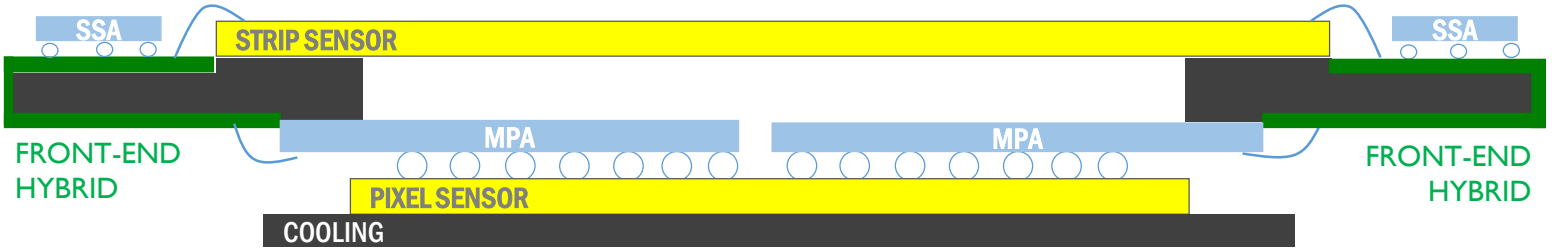
PS module
$\sim 2 \times 45$ cm^2 active area
2×960 strips: ~ 2.4 cm $\times$ 100 μm
32×960 macro-pixels: ~ 1.5 mm $\times$ 100 μm
Front-end power ~ 8 W
Sensor power ($-20\,^{\circ}$C) ~ 1.4 W

Tables and pictures from The Phase-2 Upgrade of the CMS Tracker [cds.cern.ch/record/2272264]

Pixel + Strip module

PS module is a self contained object



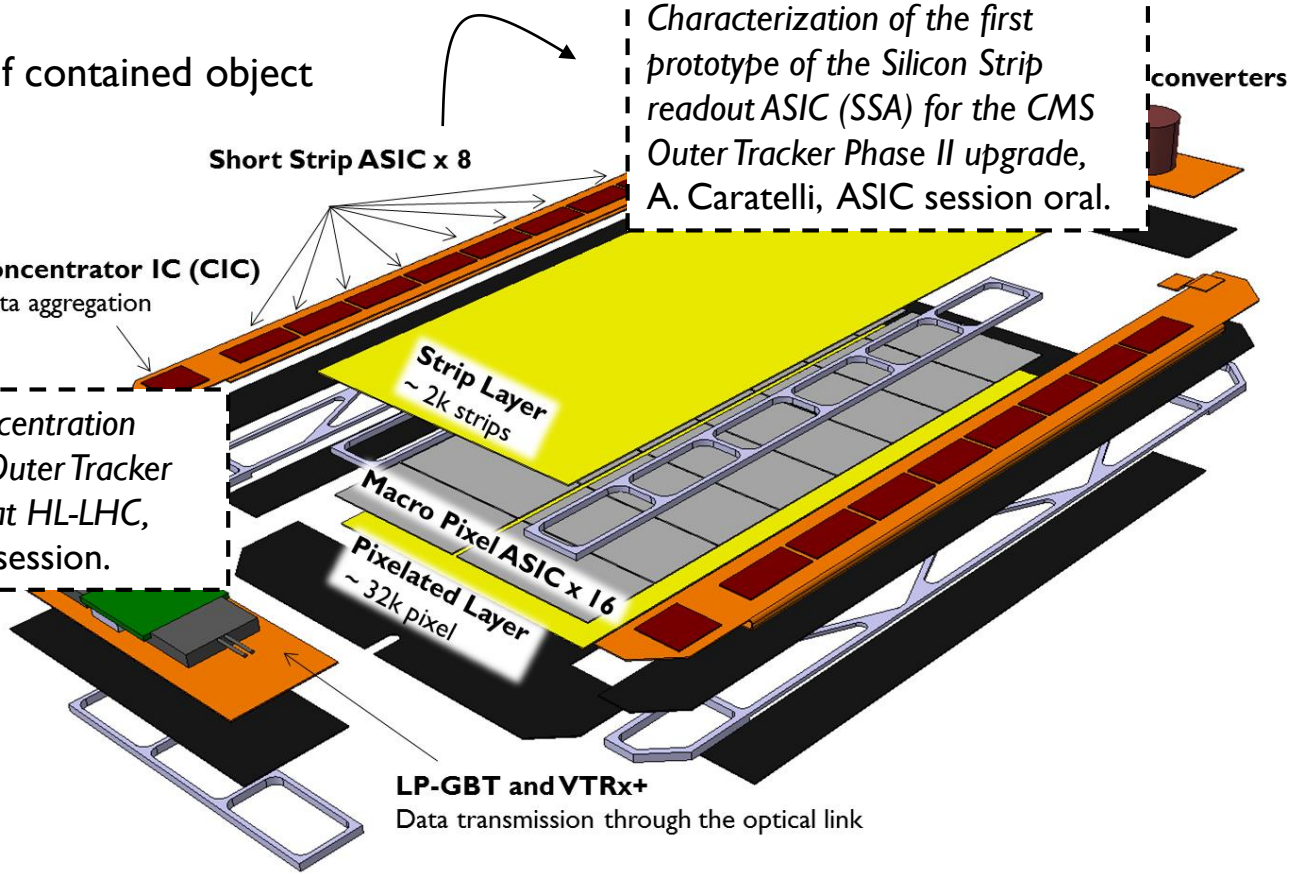


Pixel + Strip module

PS module is a self contained object

Characterization of the first prototype of the Silicon Strip readout ASIC (SSA) for the CMS Outer Tracker Phase II upgrade,
A. Caratelli, ASIC session oral.

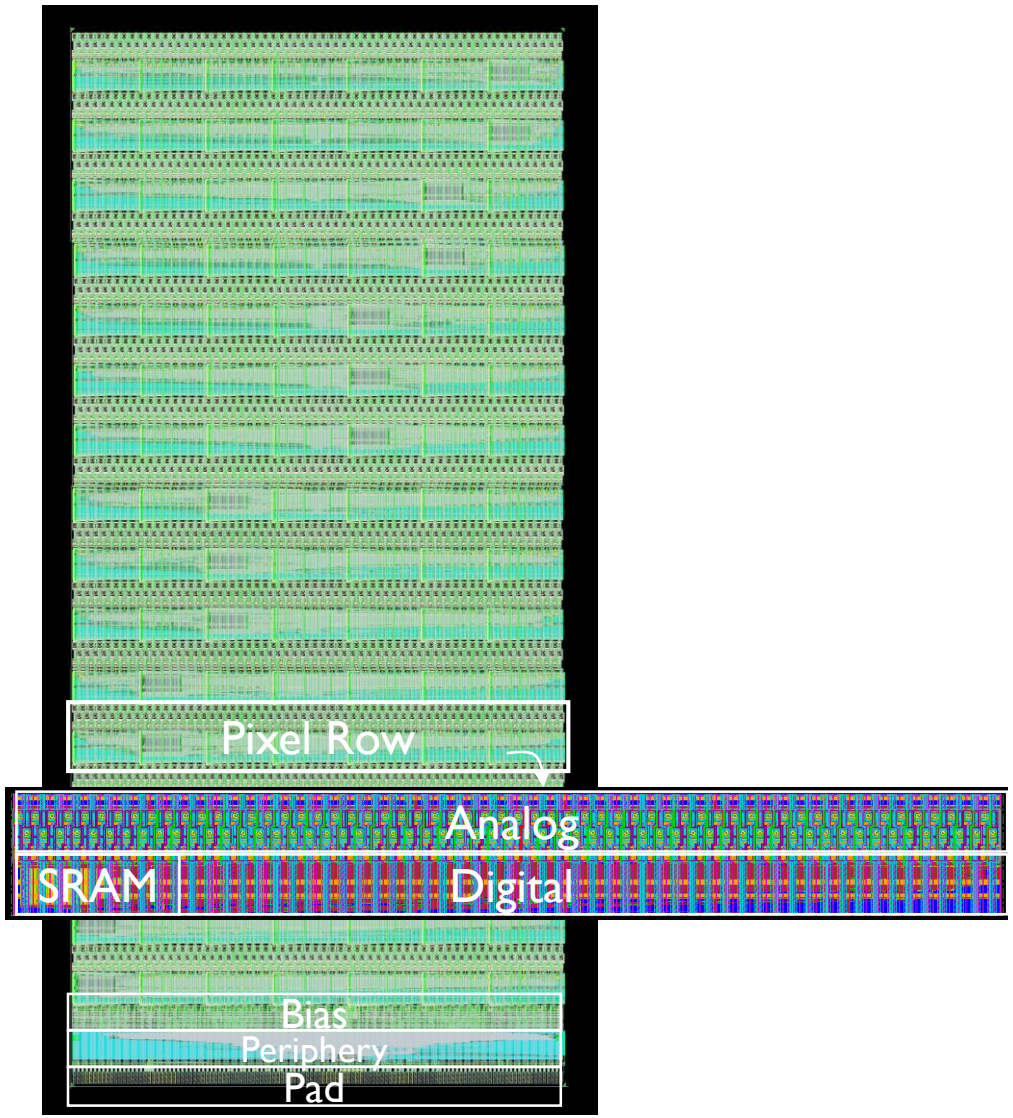
A 65 nm Data Concentration ASIC for the CMS Outer Tracker Detector Upgrade at HL-LHC,
B. Nodari, Poster session.



Module level verification SSA – MPA - CIC:

A System-Verilog Verification Environment for the CIC Data Concentrator ASIC of the CMS Outer Tracker Phase II Upgrades,
S. Scarfì, Poster session.

Macro Pixel ASIC implementation



IC Technology:

65 nm CMOS technology

Implementation technique:

Digital-on-Top architecture

Triplicated Control logic (TMR)

Clock-Gated configuration

Multi voltage supply design

Multi-VT design

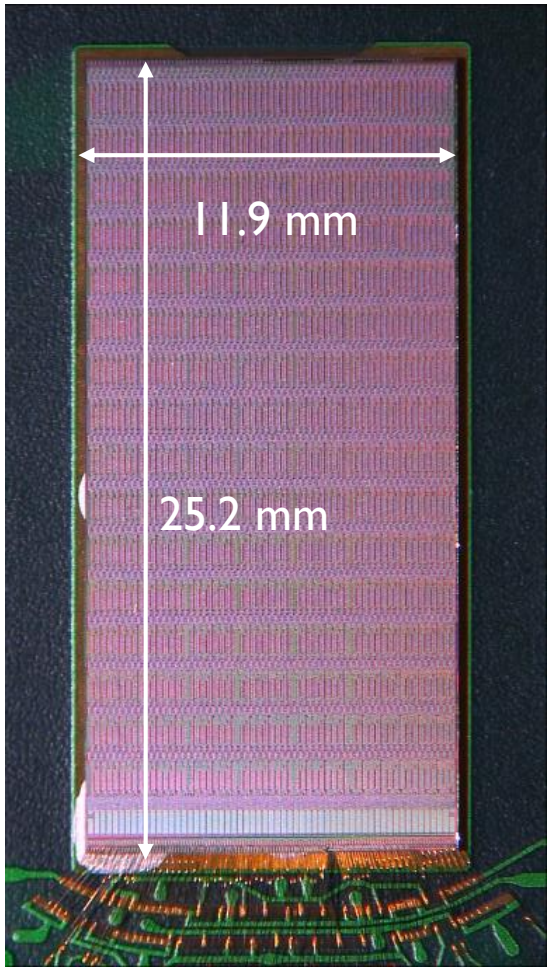
Trunk-based clock distribution

Hierarchical design

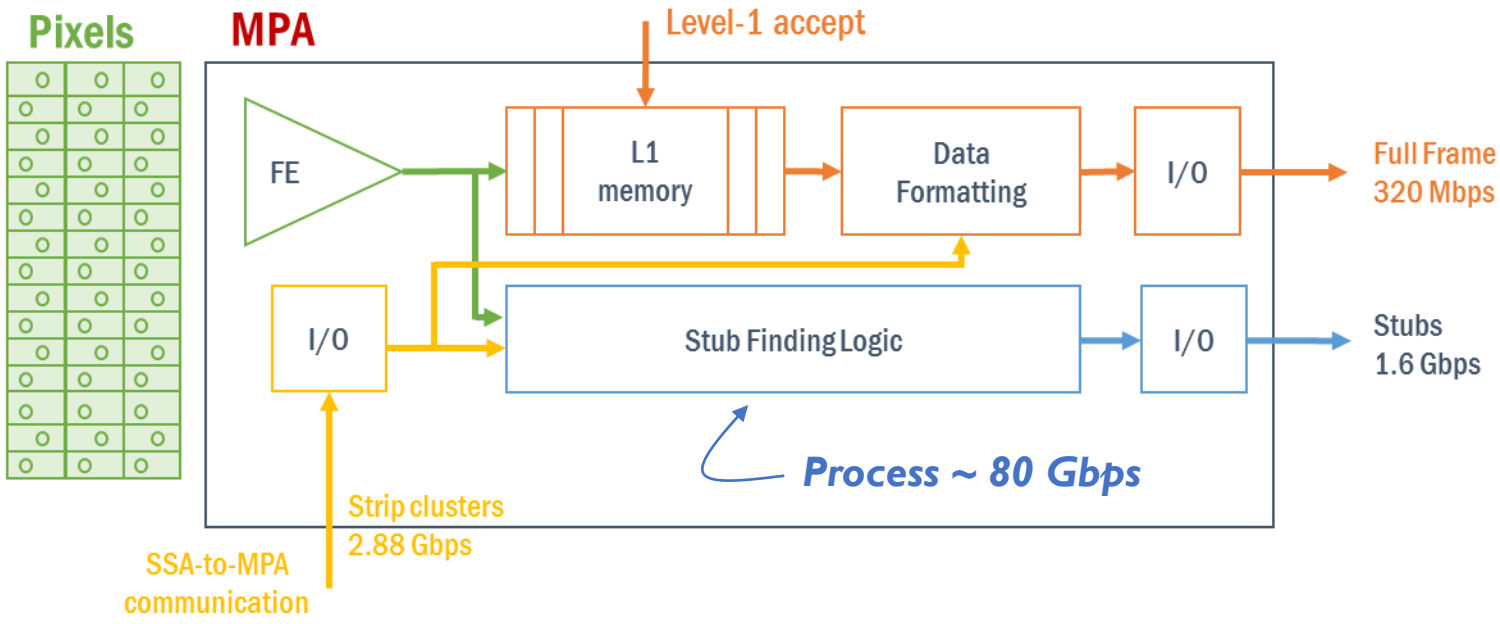
- Top
  - Analog Bias Block
  - Row (x16)
    - Digital Pixel Electronics
    - Analog Front-End
    - SRAM

Macro Pixel ASIC

Pixel Arrangement	118 x 16 = 1888 pixels
Macro Pixel Size	100 um x 1446 um
Sensor Area	5 cm x 10 cm (16 x MPA)
Acquisition Type	Continuous @ BX rate (40 MHz)
Hit Rate (Pixel hit Occupancy)	53 MHz / cm^2
Readout types	1) Triggered for full frame (L1-Trigger) 2) Continuous for high-pT information
Acquisition Mode	Binary readout
L1-Trigger latency	< 12.8 us
L1-Trigger rate	<750 kHz
Input data types	1) Raw strip data 2) Strip clusters
Output data types	1) Pixel and strip clusters 2) Stubs
Trigger data storage	Pixel frame for L1 Latency (~2048b x 512w)
Input data port	9 x Custom-sLVS @ 320 Mbps = 2.88 Gbps
Output data port	6 x Custom-sLVS @ 320 Mbps = 1.92 Gbps
Power budget	< 90 mW/cm^2
Radiation Tolerance	56 Mrad (No safety factor)
Technology	65 nm with 1p7m (4x1z1u + RDL)



MPA functionalities in a nutshell



Simulated MPA power consumption :
< 200 mW
< 100 mW/cm²

High-p_T particles @ BX rate 40 MHz with very low latency: ~ 500 ns

Full frame @ L1 trigger 1 MHz rate

MPA/SSA test system @ CERN

First full-size prototypes incorporating all functionalities required for system operation were submitted in Sept. 2017

Prototype tests started in February 2018 at CERN using bare dies.

IP-bus

FC7

Test Firmware from CMS DAQ team

Thanks to J. De Clercq, M. Haranko

VHDCI

Interface Board

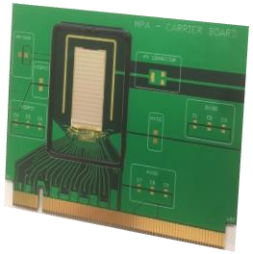
Designed by Rutgers Univeristy

Thanks to Ed Bartz, Yuri Gershtein

PCI Express

Carrier Board

Designed and produced by *Novapack*



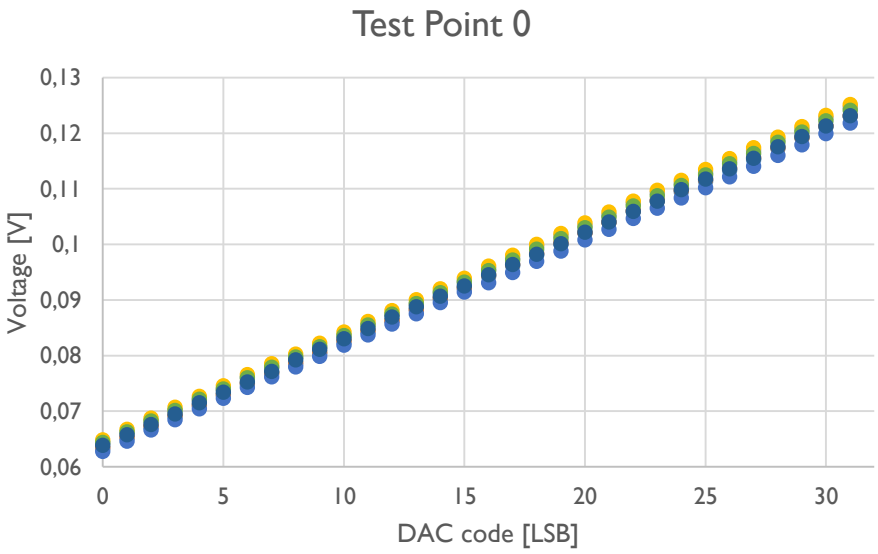
Bias Circuitry

Reminder:

- 7x bias block
- 5x DAC (with test point) for calibration

Automatic procedure:

- Measure test point
- Modify DAC to match nominal values
- Measure and validate calibration



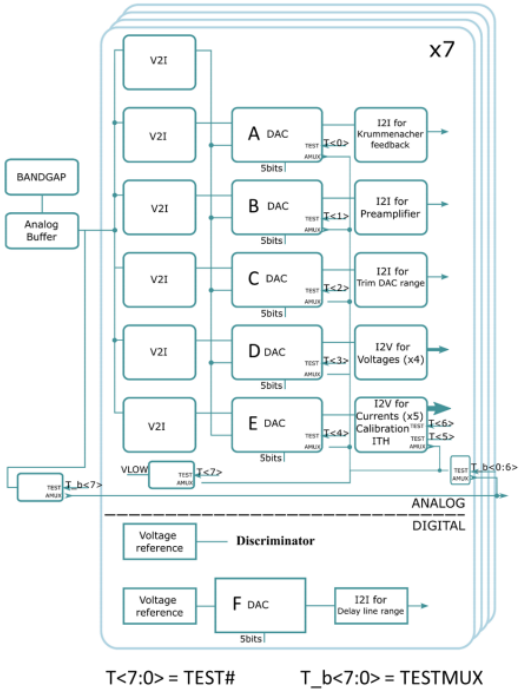
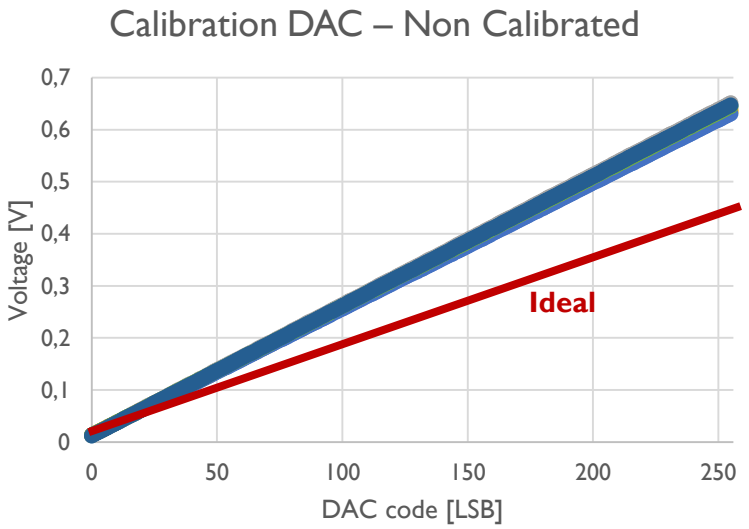


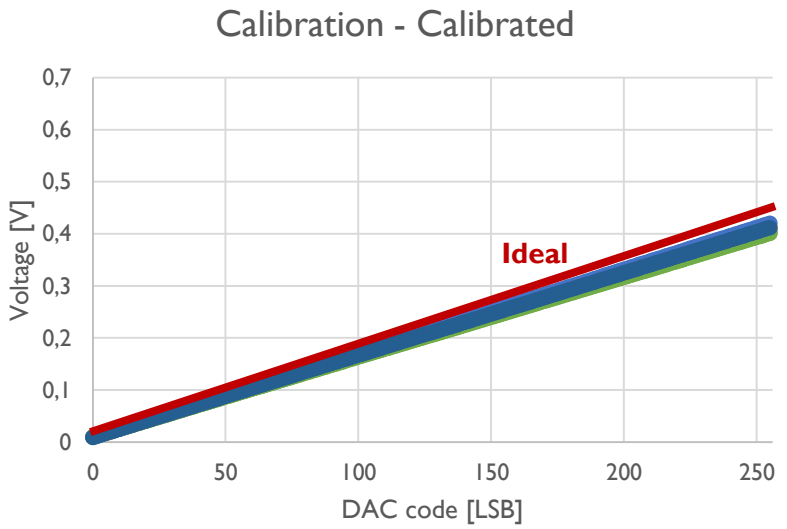
Figure 6 Bias Structure

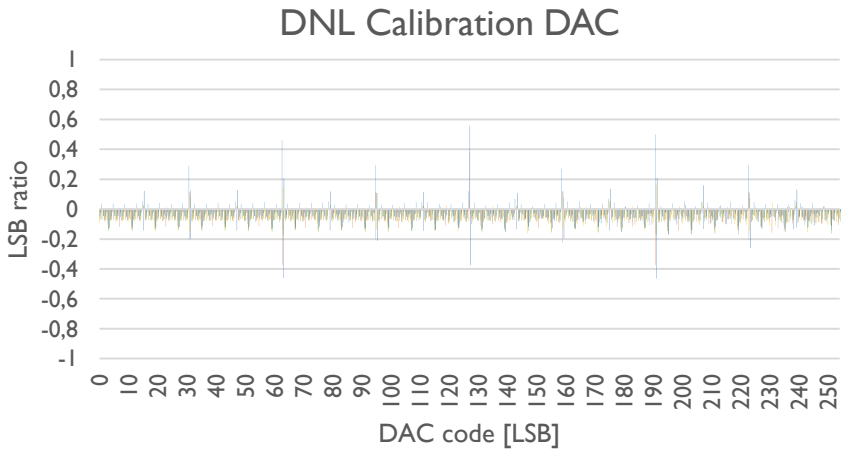
TEST# BIT	DAC PVT adj.	Description	Expected Value
0	A	Krummenacher feedback bias (80nA) : 0F	82mV
1	B	Preamplifier bias (15uA) : 0F	82mV
2	C	TRIM DAC range 65mV/153mV/250mV: 00/0F/1F	48mV/108mV/172mV
3	D	DAC for voltage biases: 0F	82mV
4	E	DAC for current biases: 0F	82mV
5	E	ITH (threshold) -10mV to +370mV: 00-FF	0 to 380mV
6	E	CALIBRATION level (0 to FF)	0 to 450mV
7	/	Local reference (GND)	0 +/-5mV

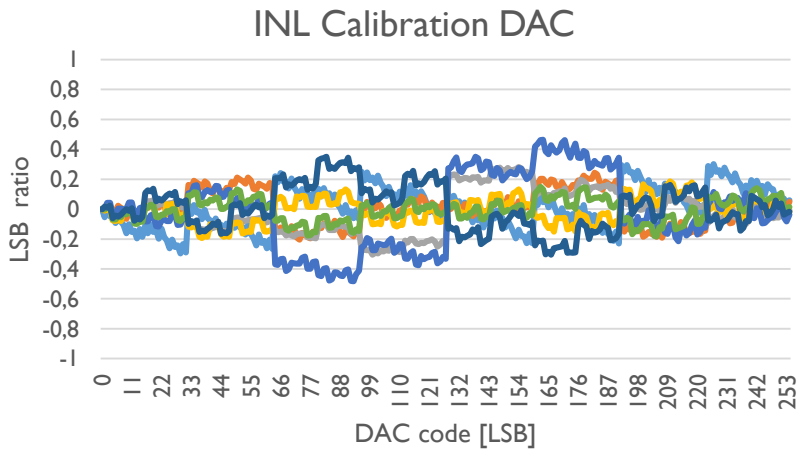
Table 2 Summary of bias DACs and test points (measured through Test Analog)

Calibration & Threshold DAC





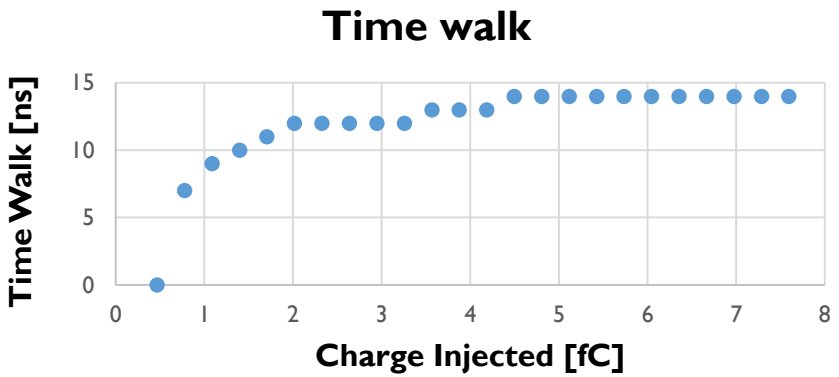


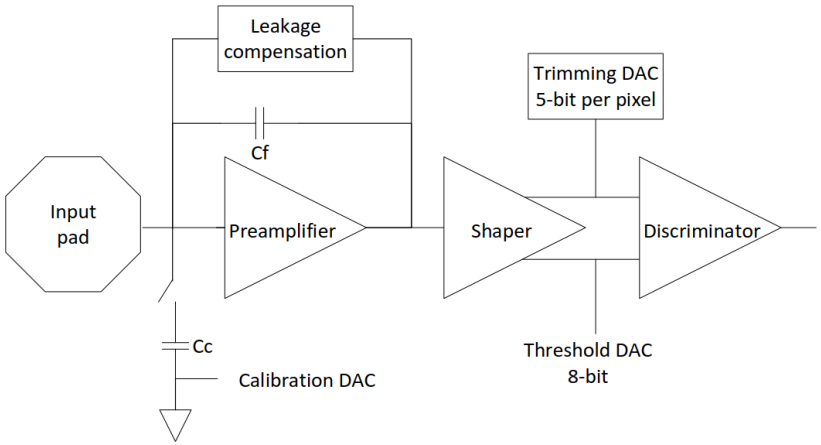


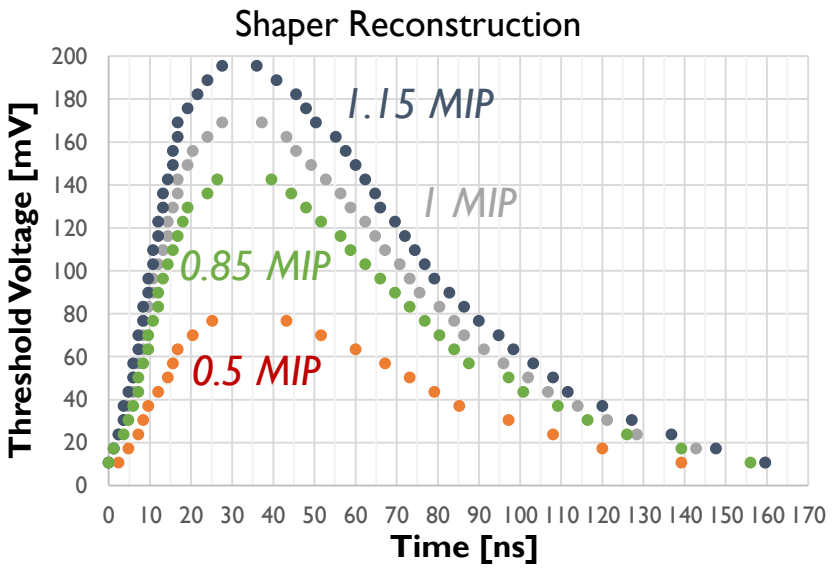
Analog Front-End results MPA

Front-End designed by J. Kaplon.
Simulation results:

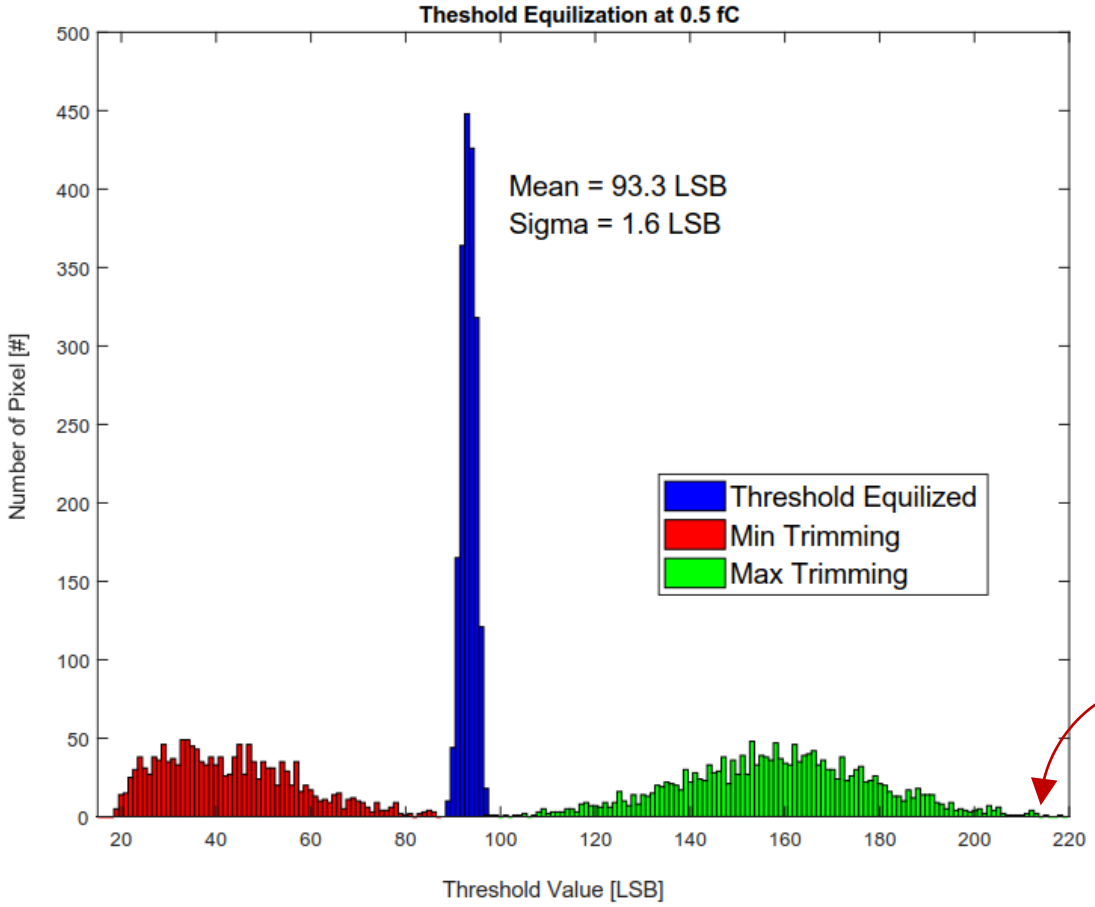
- ENC < 200 e-
- Peaking time ~ 25 ns
- SNR >> 20
- Time walk < 15 ns



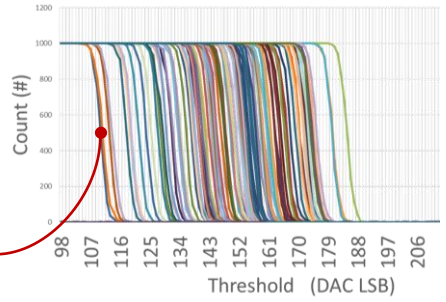




MPA Threshold Equalization test



Bin *x* counts how many pixels show the mid-point of the Scurve at a the threshold value = *x*

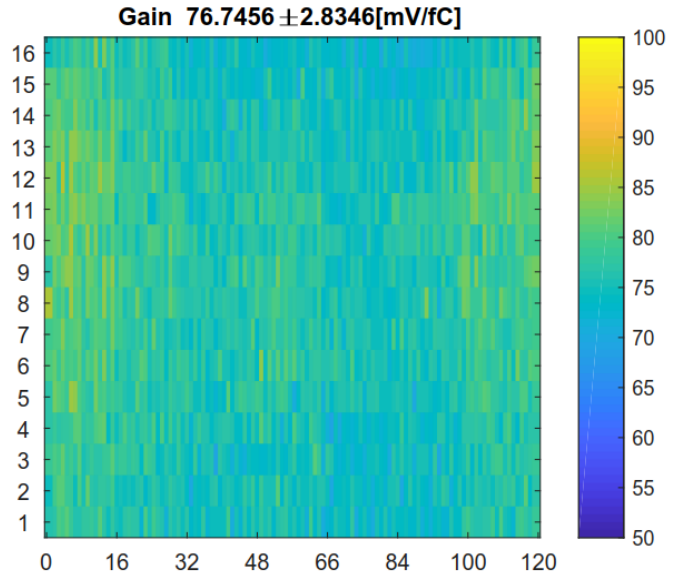


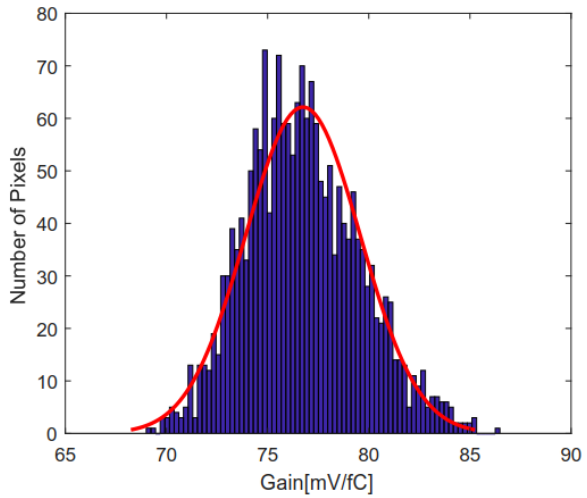
S-Curve Trimming Spread @ 0.5 fC: ±1.6 Threshold DAC LSB
± 0.55 Trimming DAC LSB ~ 150 electrons

MPA Gain and Noise results

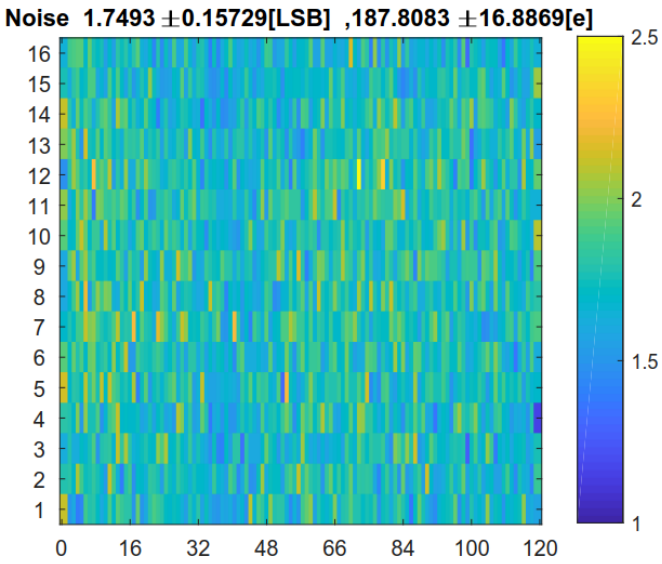
Measurements provide a good agreement with simulation and reduced-size prototype called MPA-Light (reference: http://iopscience.iop.org/article/10.1088/1748-0221/11/01/C01054)

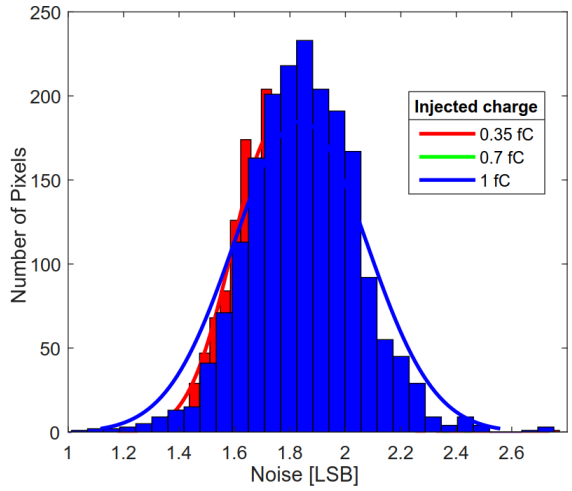
GAIN





NOISE





Power consumption measurement

Operative conditions:

Nominal Voltage

No input data

Analog FE calibrated

SLVS max. current

Measured power consumption

Analog power @ 1.25 V = 67 mW

Digital power @ 1.0 V = 91 mW

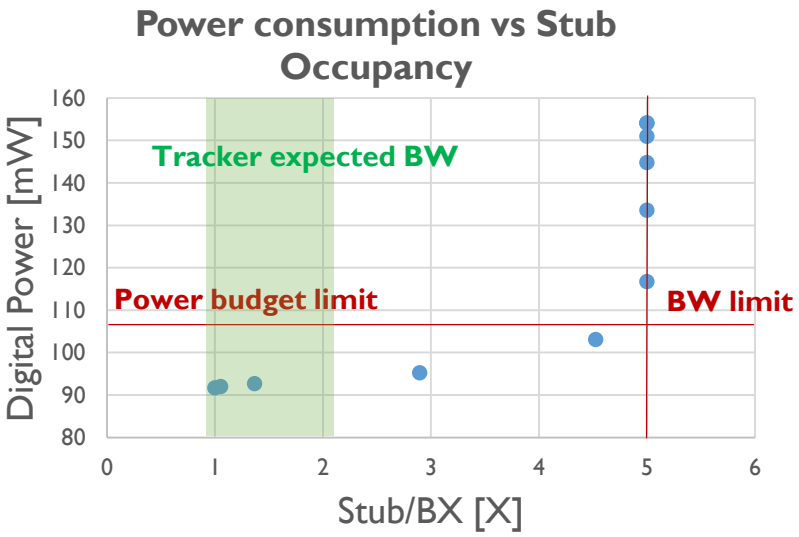
IO power @ 1.25 V = 26 mW

Total power consumption:

184 mW

Power budget < 200 mW

What happens with occupancy?



Simulation analysis power

Analog power @ 1.25 V = 70 mW

Digital power @ 1.0 V = 88 mW

IO power @ 1.25 V = 27 mW

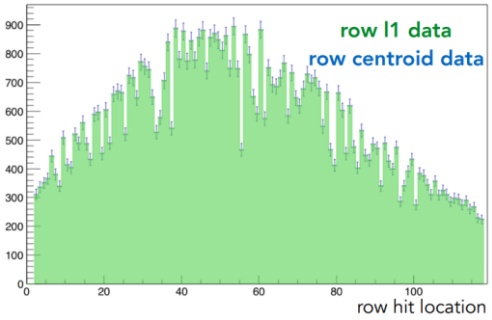
First test beam by D. Schell and J. Clercq

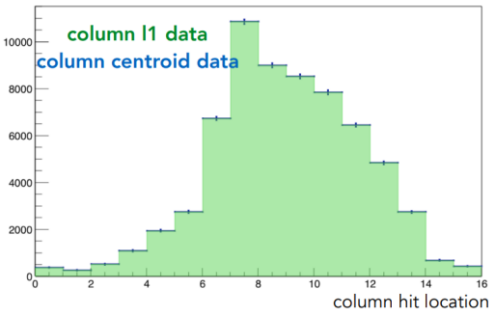
- 2 test beams:
  CERN (first time running chip, fw, sw testing, first physics results)
  DESY (testing different sensor layouts)

- Chip was operated in all three read-out modes: asynchronous, synchronous (edge sensitive) and synchronous (level sensitive)

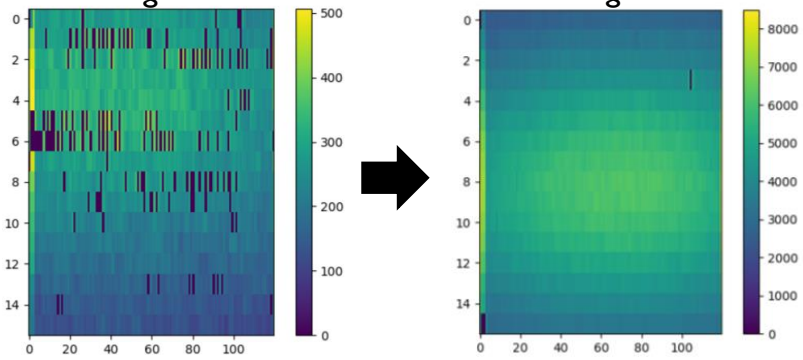
- Single sensor —> no stub data yet. Chip operated in pixel-pixel mode —> get centroid data on the stub lines

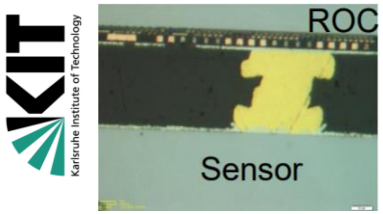
Beam Profile 30°:



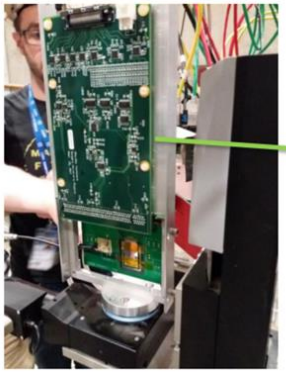


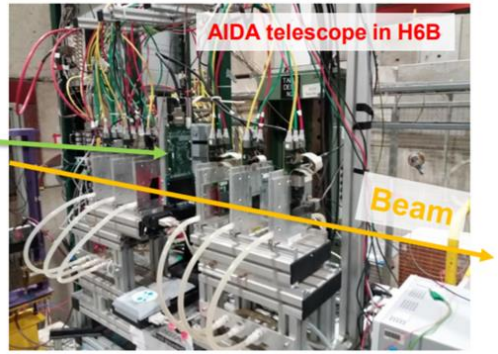
First single-MaPSA *New single-MaPSA*





gold stud bonding
by KIT





Wafer probing results

Thanks to J. Alozy, M. Osherson, A. Apresyan and D. Giovinazzo.

4 Wafer tested (with and without bumps)

- Fully automatized procedure (python)
- 3.5 mins/chip for complete characterization

Run example:

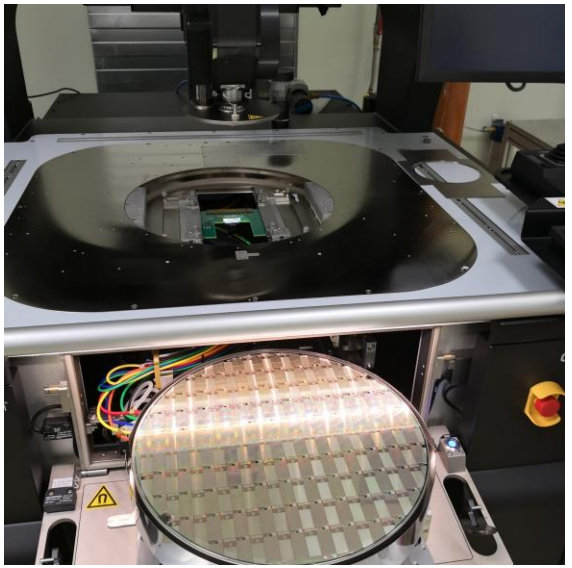
88 chips tested (one chip does not power up).

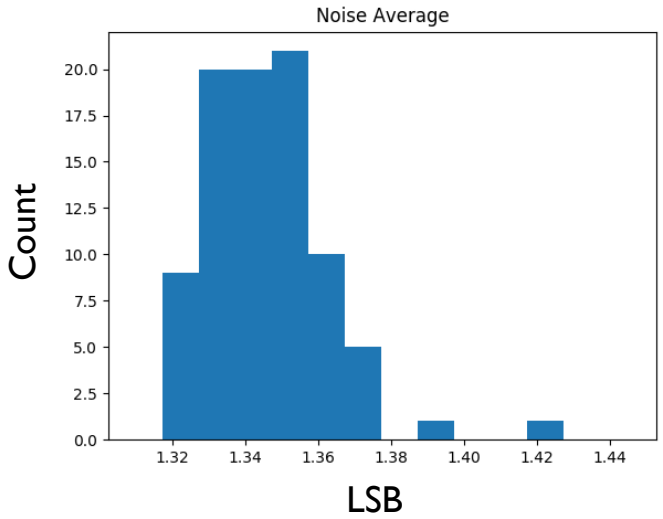
Performance of the 87 remaining chips analysed:

- Control: all chips passed basic checks (I2C, output alignment, bias calibration).
- Analog: all chips show working fast readout;
  - Three chips show bad pixels (yield ~ 95%).
- Digital: Trigger and L1 path tested (SRAM at 1.2V):
  - 71 good chips (yield ~ 81%);
  - Loss related with memory issue.

Final Yield **69 good chips** (yield ~ 78%)

Expected yield from foundry model ~ 65%





MPA results with TID

Thanks to G. Borghello and H. Koch

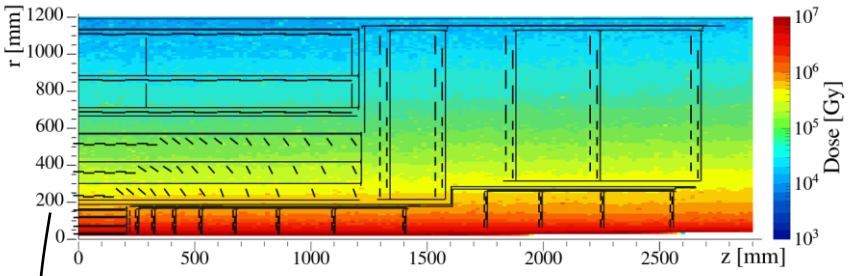
Irradiation performed using the new CERN X-Ray facility (~1.5 Mrad/h on ~3 cm^2).

Room temperature

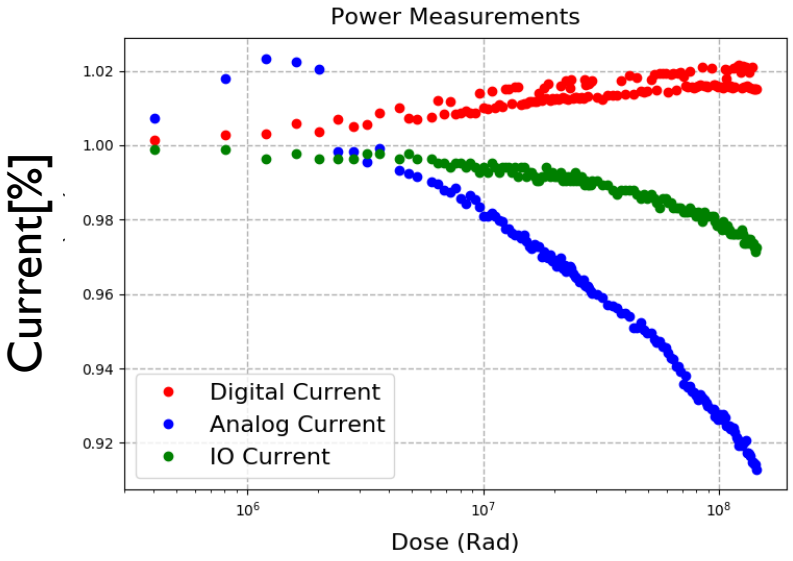
3 runs 100, 150, 200 Mrad

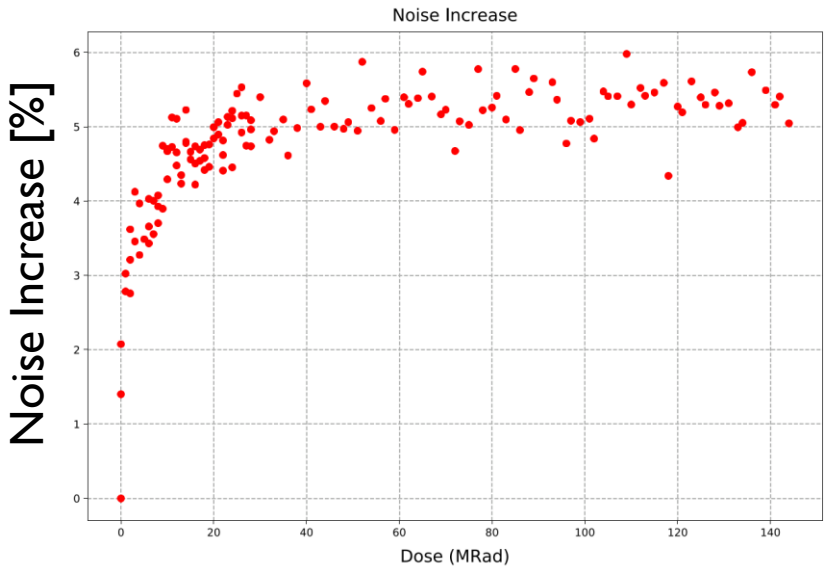
Digital functionalities were not degraded

Analog degradation was within expectation <10 %



Max TID: 560 kGy → 56 Mrad
(without safety factor from TDR 2017)





Conclusions

- First full-size and full-functionality MPA prototype was fabricated in 65 nm CMOS technology
- Functional verification and performance characterization test results are very promising
- High quality Test beam results produced using MPA-sensor assemblies
- First TID test on the MPA confirms radiation harness up to 200 Mrad
- These prototypes enable the development of the first PS module assemblies

Davide.Ceresa@cern.ch

Thanks to…

MPA-SSA design team at CERN:

Alessandro Caratelli, Davide Ceresa, Jan Kaplon, Kostas Kloukinas, Jan Murdzek and Simone Scarfi'

to our collaborators for design:

CERN: *Stefano Michelis* for the bandgap design

University of Bergamo and INFN Pavia: *Francesco De Canio and Gianluca Traversi* for the sLVS TX and RX design

SMU: Gong Datao, Yang Dongxu and Jian Wang for the DLL design

RAL: Stephen Thomas for the Analog buffer design

to our collaborators for testing :

M. Osherson(Fermilab), B. Harrop (Princeton), E. Bartz (Rutgers), A. Apresyan (Fermilab), S. Los (Fermilab), Y. Gershtein (Rutgers), J. Alozy (CERN).

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Reference

- D Abbaneo and A Marchioro, *A hybrid module architecture for a prompt momentum discriminating tracker at HL-LHC,* Journal of Instrumentation, Volume 7, September 2012
- D. Ceresa et Al., *Macro Pixel ASIC (MPA): the readout ASIC for the pixel-strip (PS) module of the CMS outer tracker at HL-LHC*, Journal of Instrumentation, Volume 9, November 2014
- D. Ceresa et Al., *Readout architecture for the Pixel-Strip (PS) module of the CMS Outer Tracker Phase-2 upgrade*, PoS(Vertex 2016)066 .
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Reference

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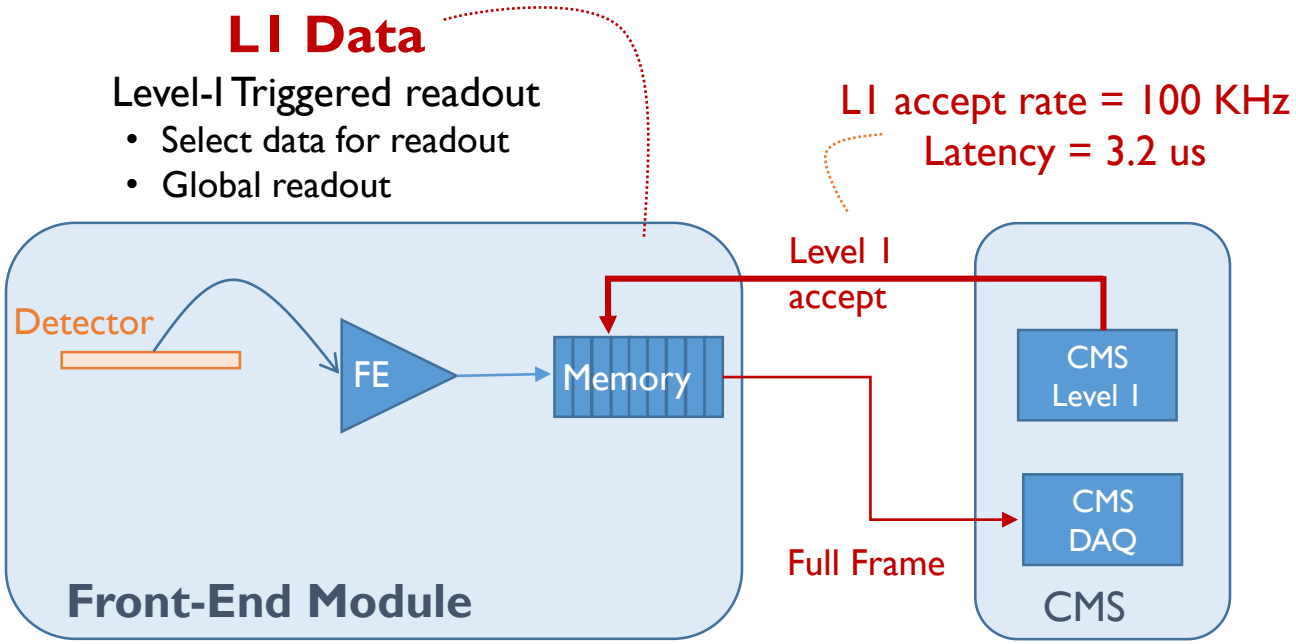
Spare slides

Current Silicon Strip Tracker



Outer Tracker principle of operation

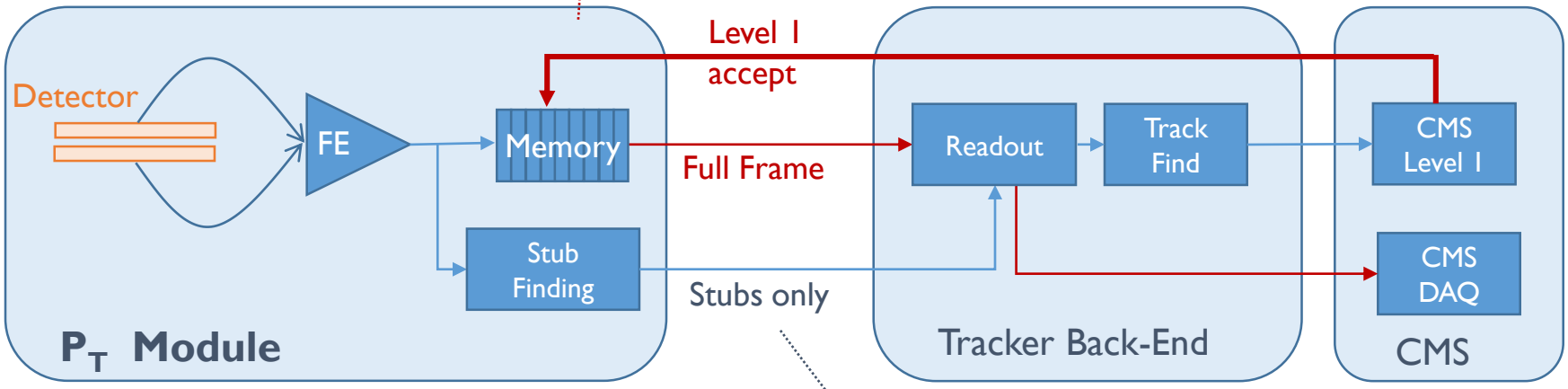
L1 Data

Level-1 Triggered readout

- Select data for readout
- Global readout

L1 accept rate = **750 KHz**

Latency = **12.8 us**

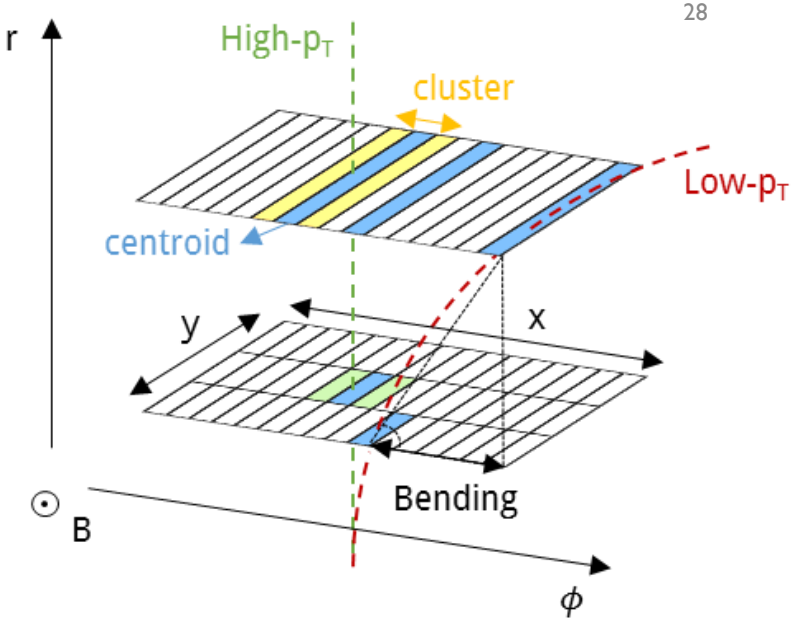


Stub Finding

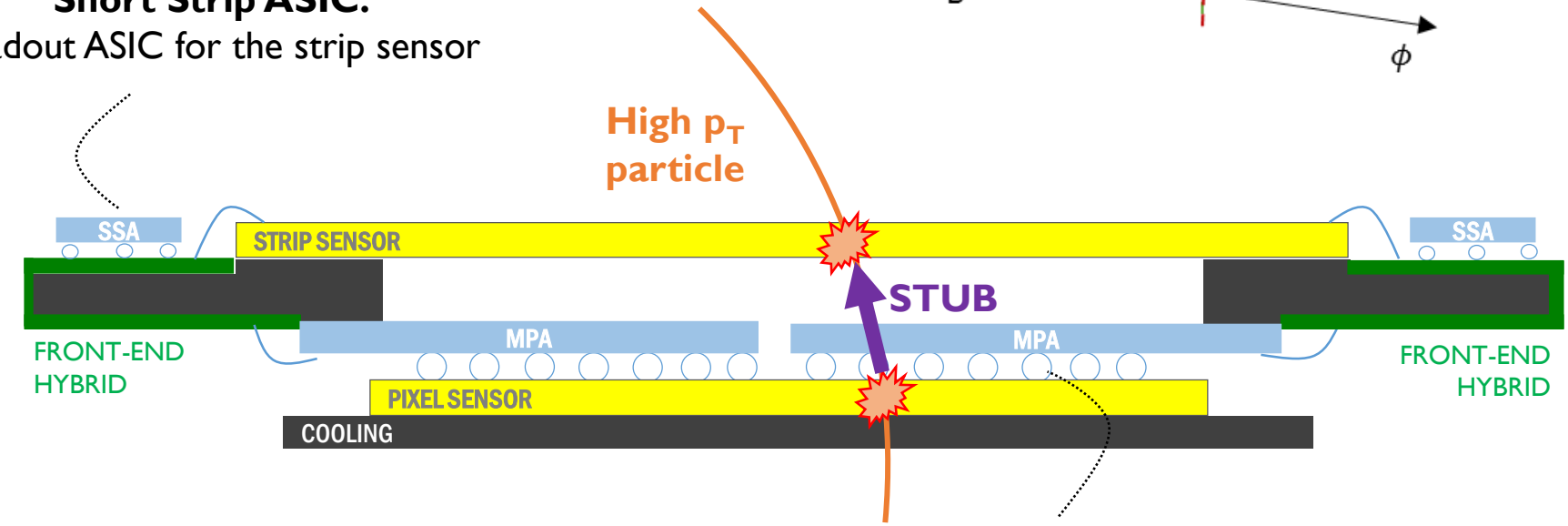
High-pT (stub) event-driven readout:

- Continuous readout
- ***Quick and on-chip data selection***

What is a P_T module?



Short Strip ASIC:
readout ASIC for the strip sensor



Macro Pixel ASIC
readout ASIC for the pixel sensor

Slow Control

MPA and SSA uses an I2C protocol for external interfacing and an Wish Bone protocol for internal configuration

⇩

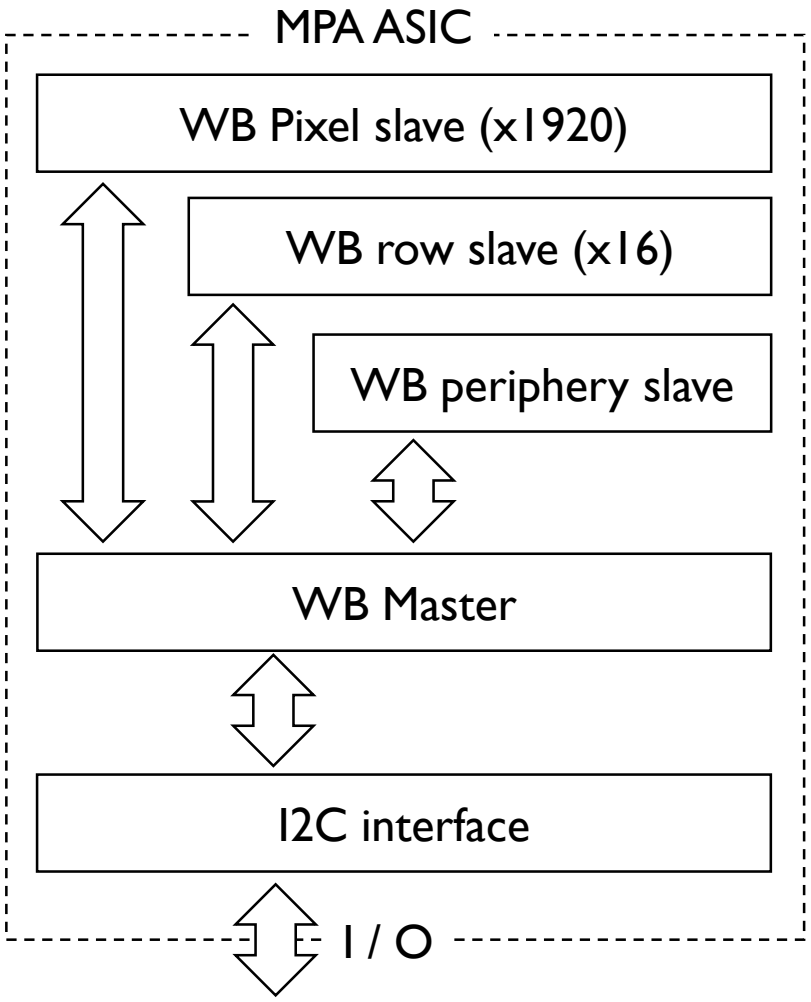
MPA 10 bit x 1920 pixels + periphery
= 13 mW
(15% of digital power budget)

⇩

The I2C interface is activated only when a I2C command is received and **only the addressed WB slave is activated**.

⇩

Configuration power consumption
< 1 mW



Clock distribution

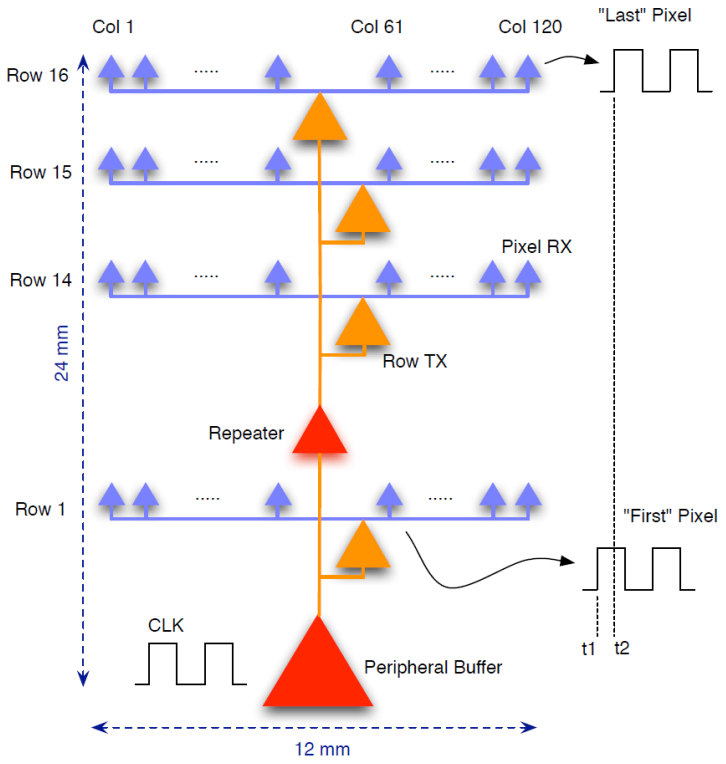
Clock distribution design:

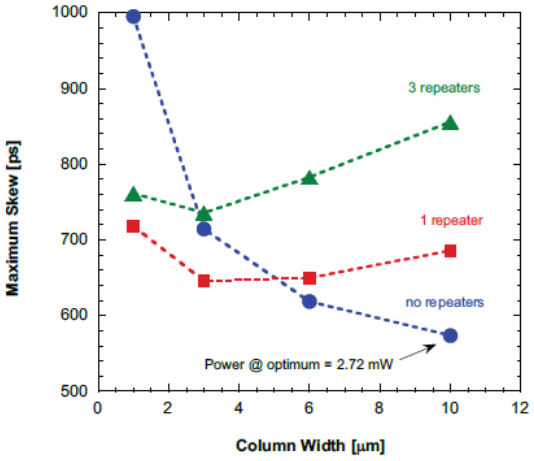
A clock distribution with one column saves a factor ~10 in power consumption. Simulation shows that the skew can be kept below 1 ns which is enough for the application.

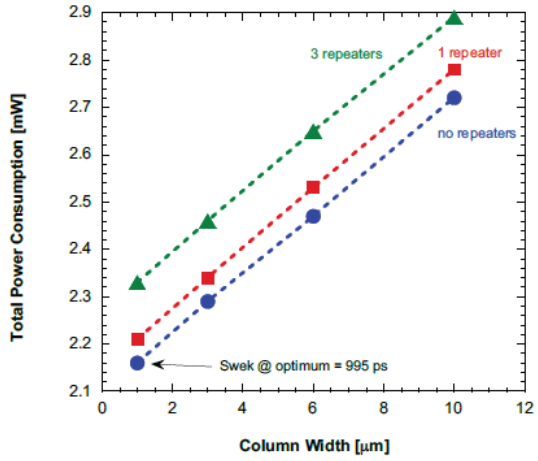
Open Issue:

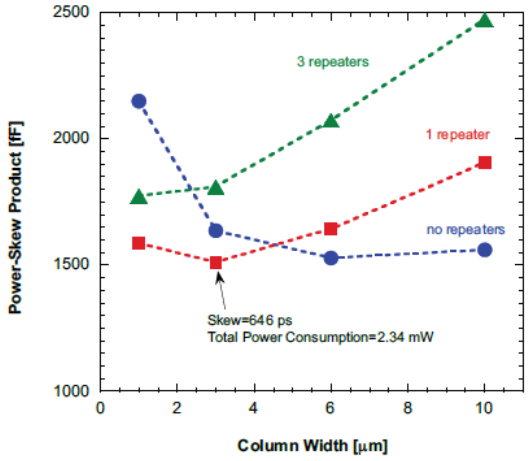
How to implement in digital-on-top design?

The clock tree in the pixel array should follow the dimension and the structure defined by the study.









Strip Centroid identification logic

Firmware

SSA emulator on FC7 allows to send single/multi programmable strip centroid

Study single/multi cycle line alignment and processing

ASIC

Strip-Strip mode: the MPA sends in output the strip centroids.

Check SSA data and I/O data bus
(8 x 320 MHz input, 5 x 320 MHz output)

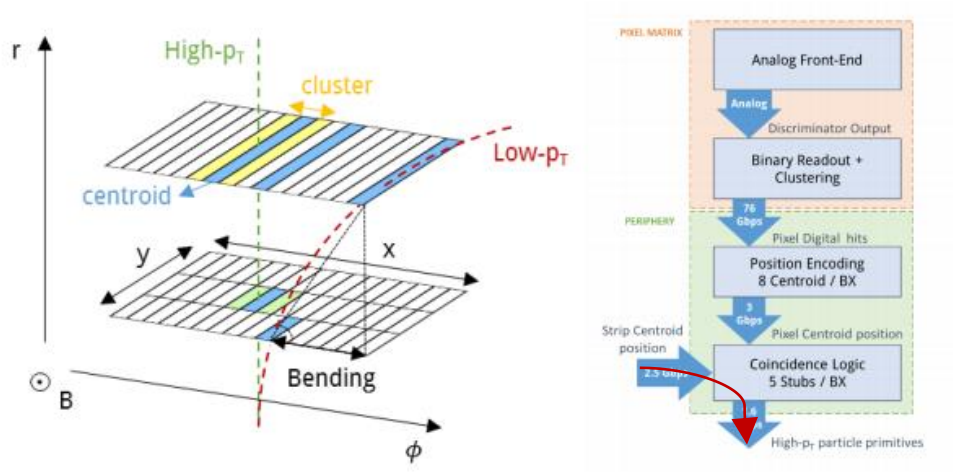


Figure 8 Stub Finding in PS-module scheme (left) and block diagram (right)

Define Strip Centroid and line in firmware: 64

Stub Position
BX 1: 0,0,0,0,0
BX 2: 0,0,0,0,0
…
BX 21: 64, 0, 0,0,0

Pixel Centroid identification Logic

Tested

ASIC

Pixel-Pixel Mode: the MPA sends out Pixel Centroid

- Configure ***Digital Calibration*** Input
- Send Pulse
- Observe Output Stub (Clustering, Encoding, BX Averaging, etc)
- Observe Data Latency

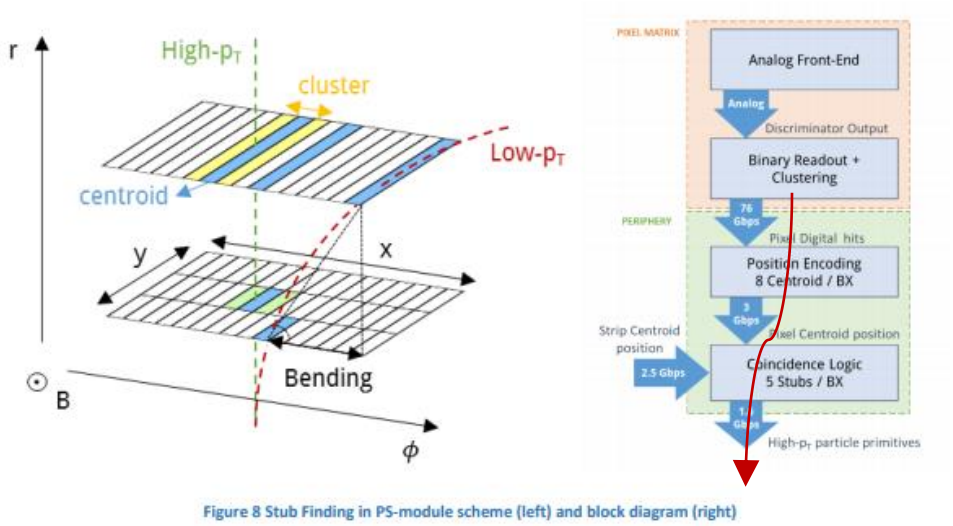


Figure 8 Stub Finding in PS-module scheme (left) and block diagram (right)

Pulse injection in:
17, 18,19,20, 25,26

Stub Position
BX 1: 0,0,0,0,0
BX 2: 0,0,0,0,0
…
BX 21: 34, 38, 51,0,0

Stub Processing Logic

Firmware

SSA emulator on FC7 allows to send single/multi programmable strip centroid

Test of coincidence logic and stub generation

ASIC

Tracker (Normal) Mode: the MPA sends out stubs

- Configure ***Digital Calibration*** Input
- Send Pulse

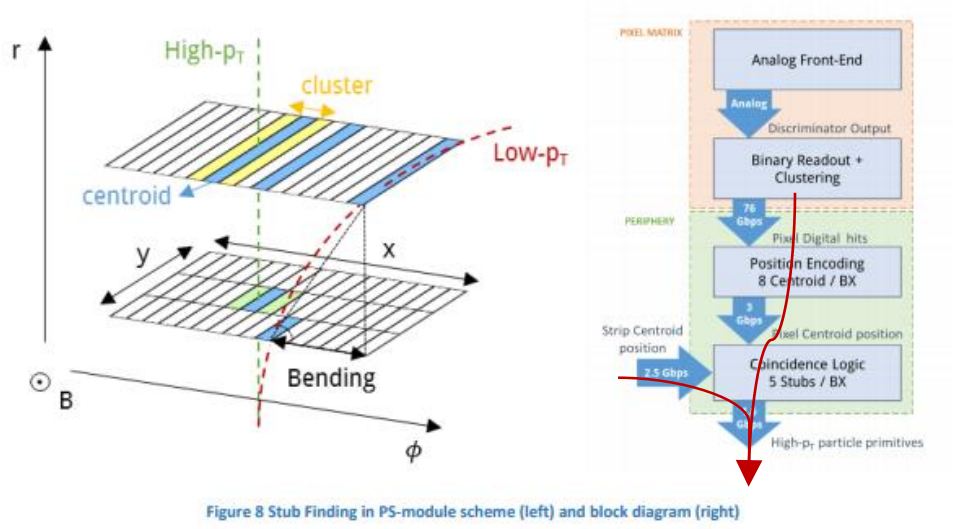


Figure 8 Stub Finding in PS-module scheme (left) and block diagram (right)

Pulse injection in:
17, 18,19,20, 25,26

Stub Position
BX 1: 0,0,0,0,0
BX 2: 0,0,0,0,0
…
BX 21: 34, 38, 51,0,0

Binary Readout Logic

- Configure Pixel-Pixel Mode
- Configure ***Analog Calibration*** Input
- Send Pulse
- Observe Output Stub (Sampling, HIP suppression, Clustering, Encoding, BX Averaging, etc)
- Observe Data Latency

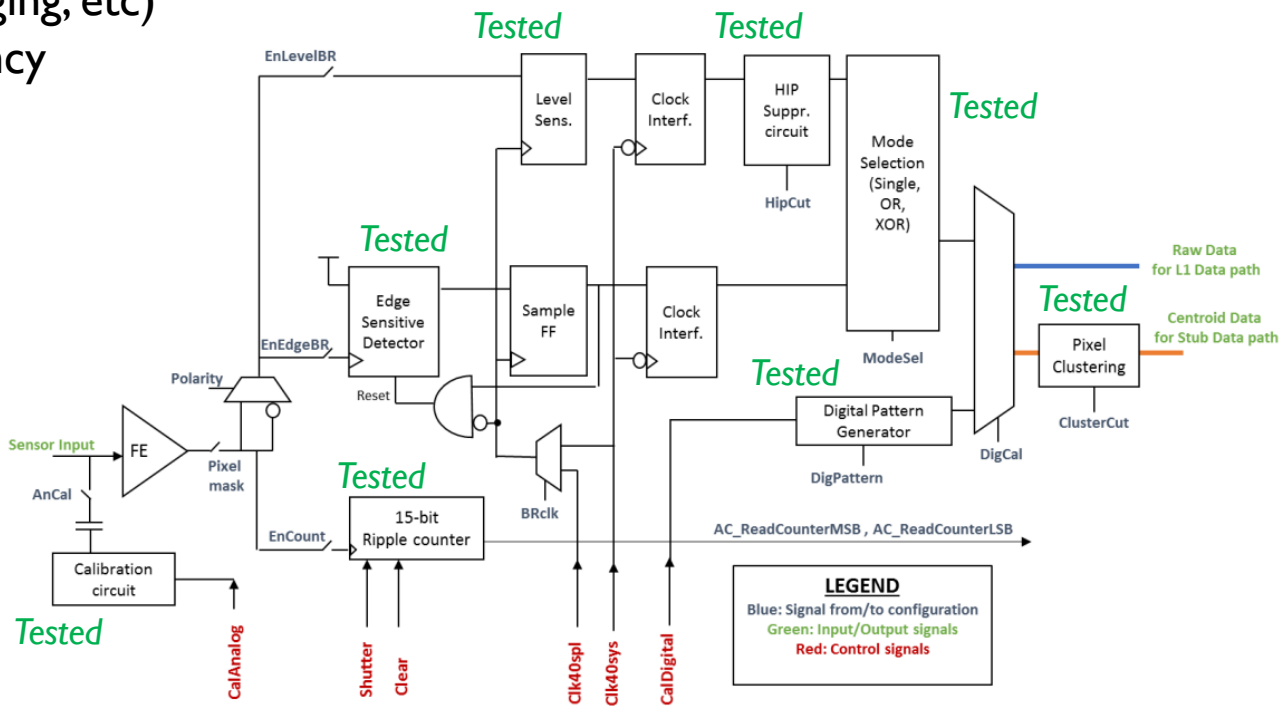


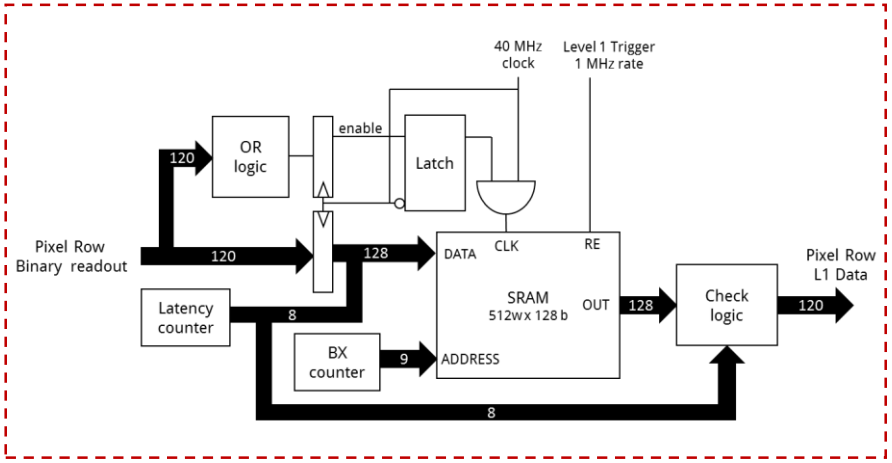
Figure 7 Binary Readout schematic

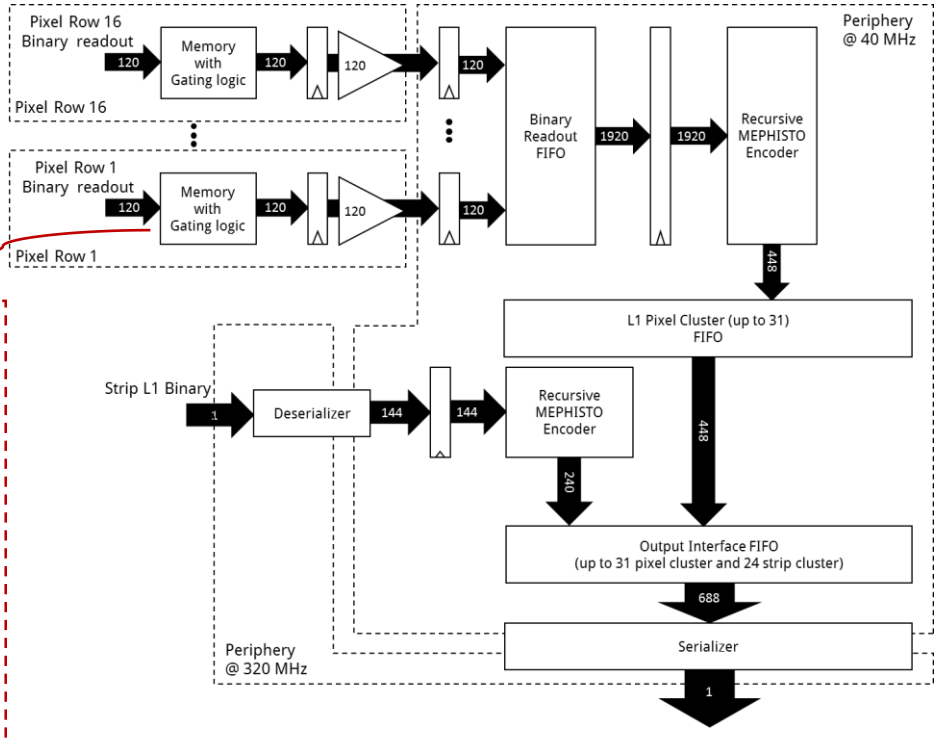
L1 Data with memory gating

Output Frame to data concentrator for L1 data:

- Triggered transmission
- Unique start sequence (19 bits)
- Variable packet size depending on event size (max. 32 Pixel/Strip clusters)
- Initial training with fixed or pseudo-random sequence capabilities (phase Aligner on receiver side)

Memory gating is a key feature for the power requirements



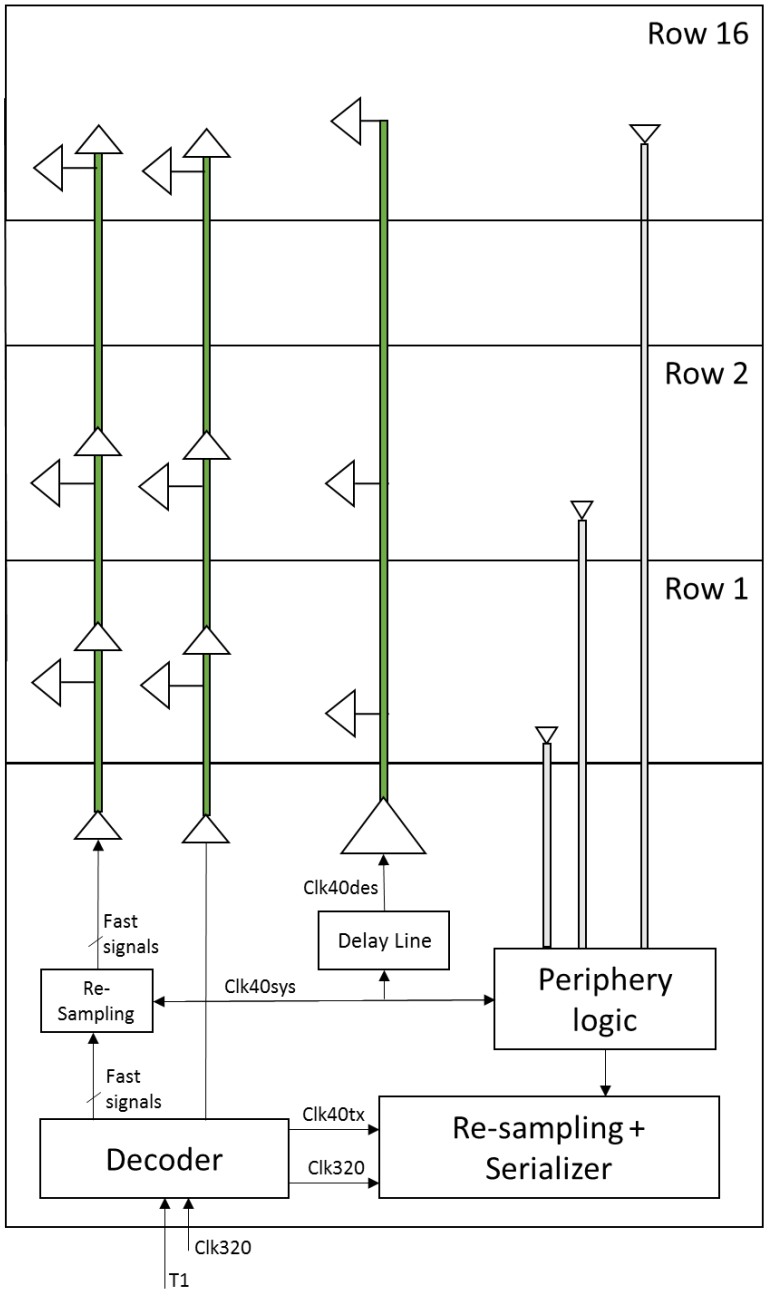


Clock distribution

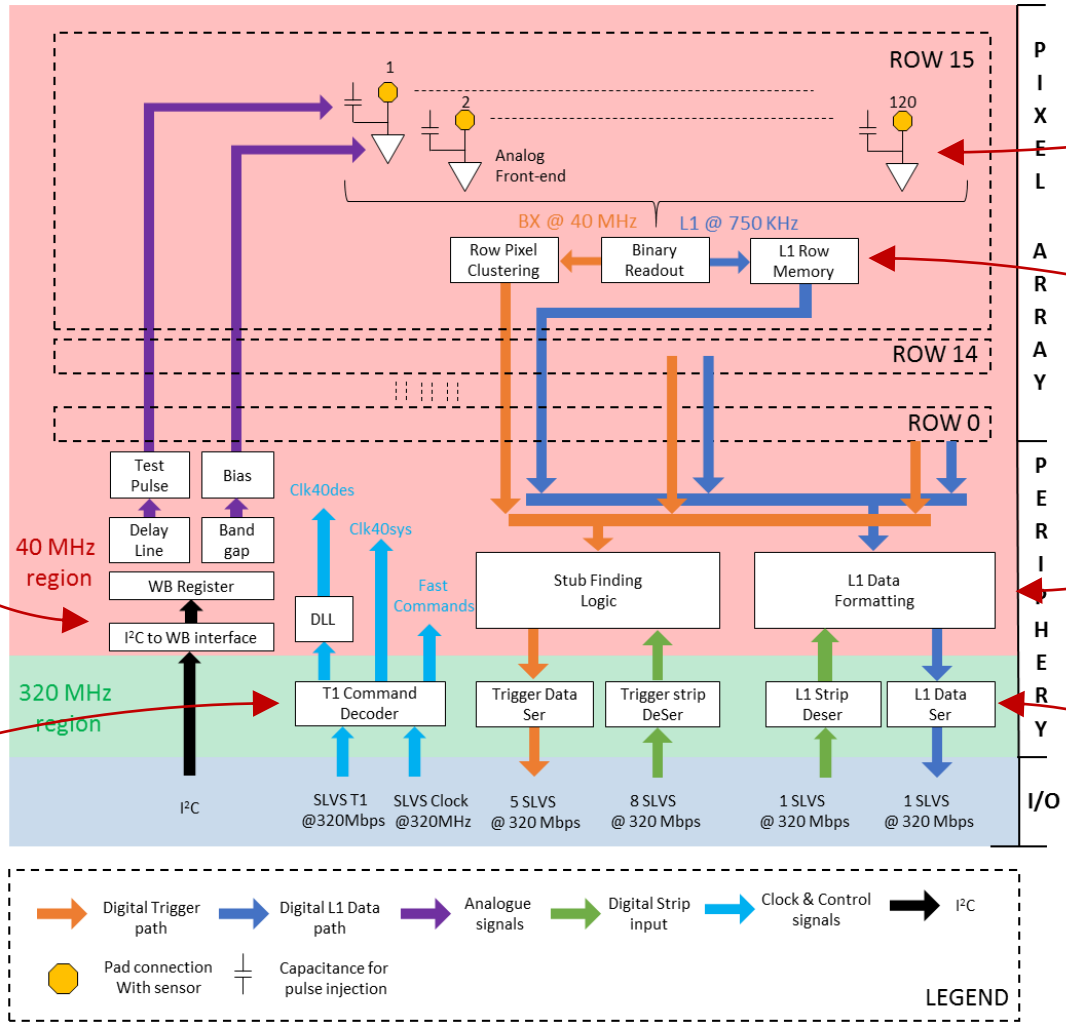
Clk40Des:
- 40 MHz clock for FE sampling
- Distributed with Clock Trunk approach
- Clock domain crossing to clk40sys in pixel core
- Δt respect clk40sys = 0-3.125 ns

Clk40sys
- 40 MHz system clock
- Distributed with re-buffering at each row
- Skewed to limit Voltage drop
- Triplicated
- Clock domain crossing to clk40tx before serializer
- Δt respect clk40sys = 0-21.875 ns

Clk40tx
- 40 MHz transmission clock
- Used to synchronise Serializer and Deserializer



MPA Block Diagram



1- Configuration

2- Fast control

5- Analog Front-End

4- Digital processing

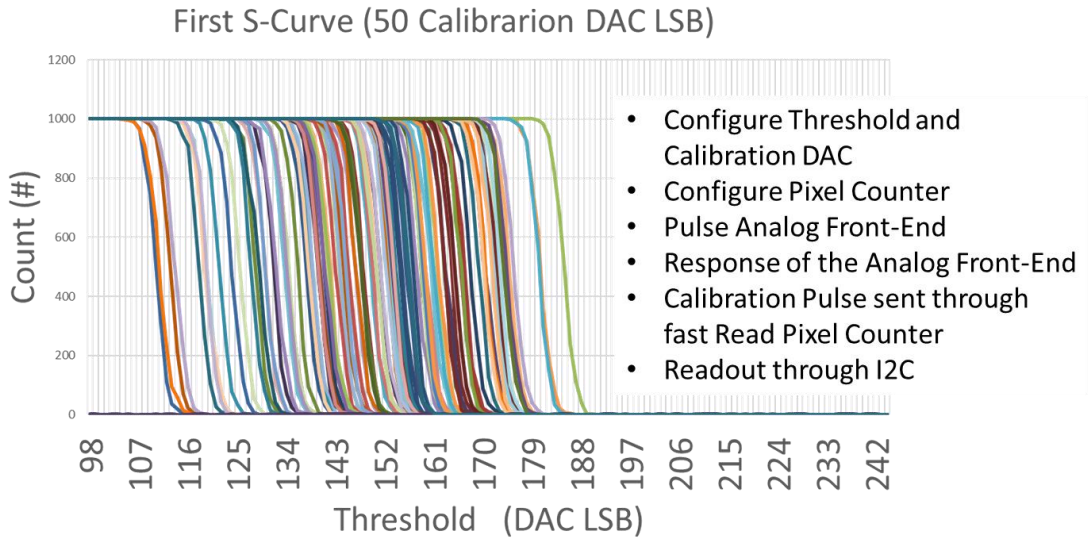
3- In/Out communication

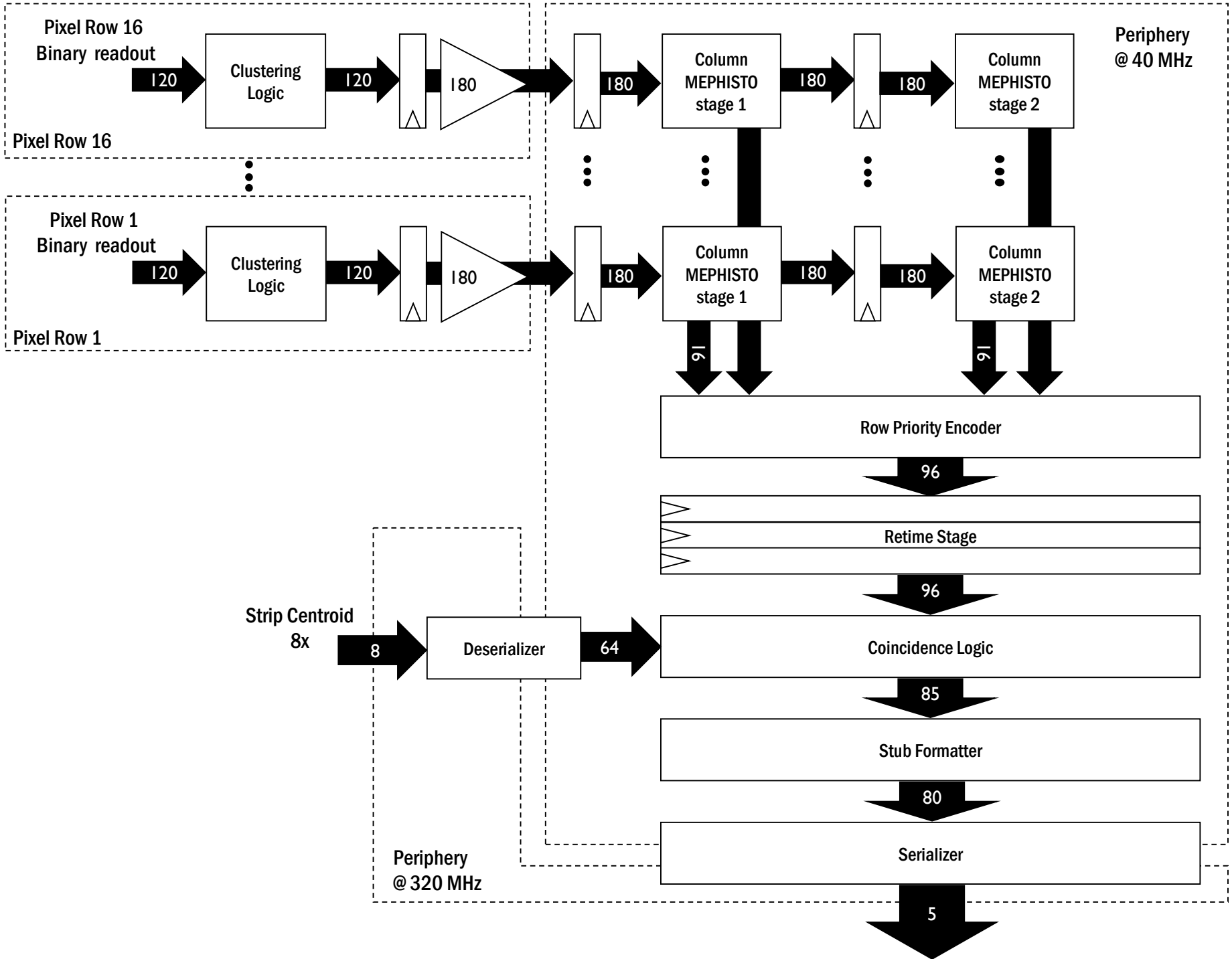
Fast Counter Readout

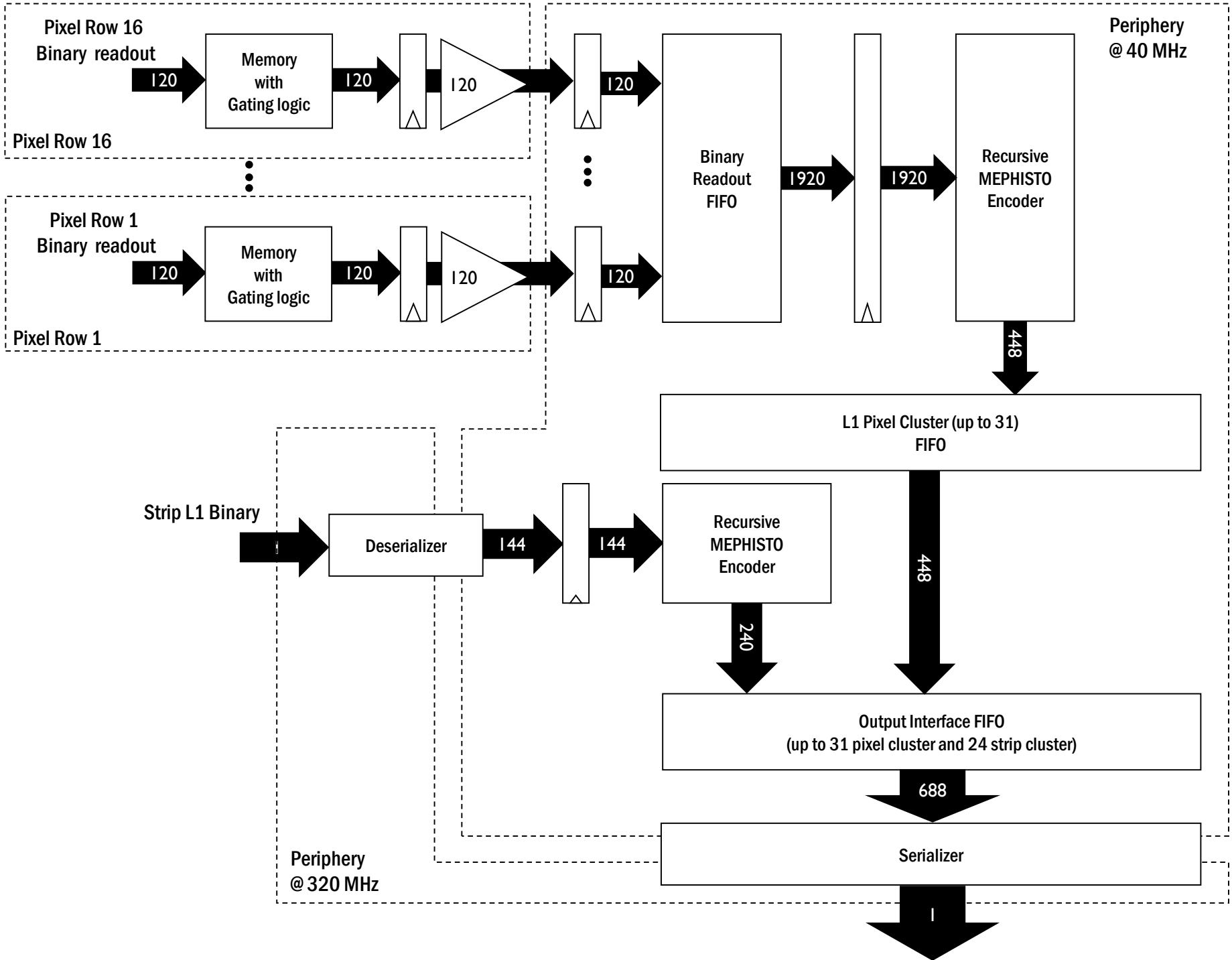
Readouts the full matrix counters (15 bits x 1920 pixels) in 400 us

- 1 counter / 8 BX
- Compatible with standard readout

Allow to produce quickly S-Curve and start performance study and trimming

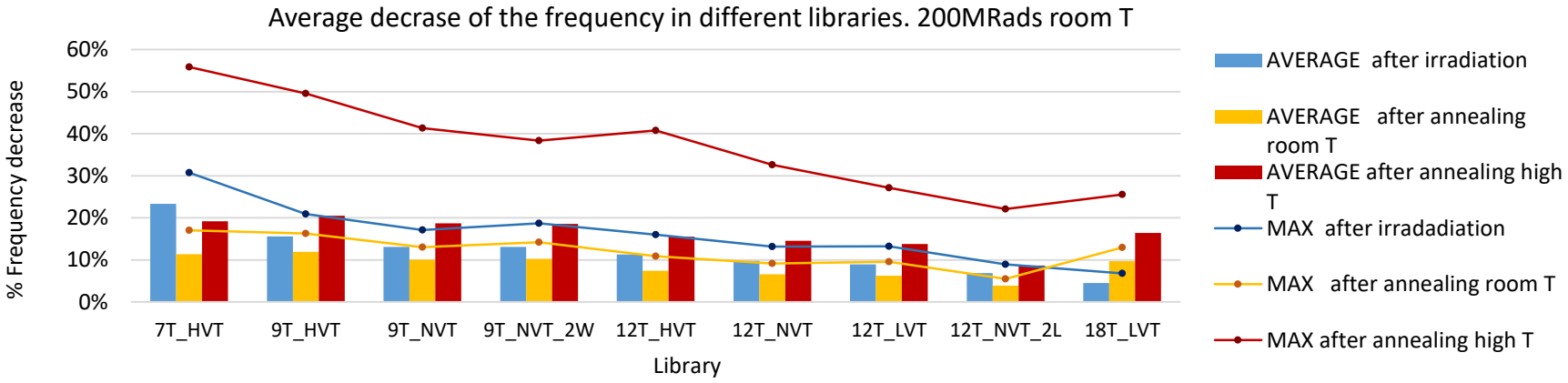


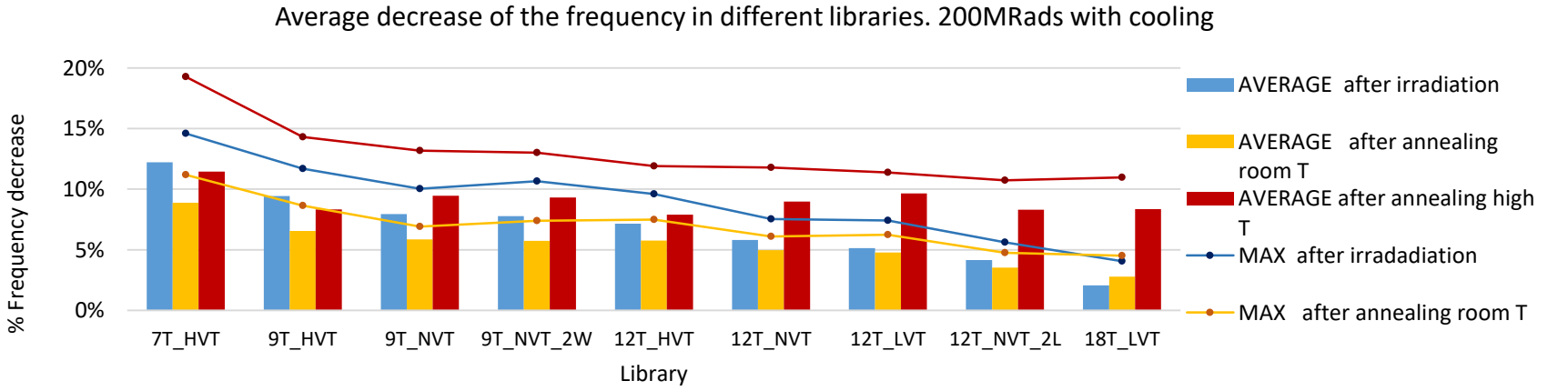

Pixel Row 16
Binary readout
120
Clustering Logic
120
180
Pixel Row 16
Pixel Row 1
Binary readout
120
Clustering Logic
120
180
Pixel Row 1
Periphery @ 40 MHz
180
Column MEPHISTO stage 1
180
180
Column MEPHISTO stage 2
180
Column MEPHISTO stage 1
180
180
Column MEPHISTO stage 2
16
16
Row Priority Encoder
96
Retime Stage
96
Strip Centroid 8x
8
Deserializer
64
Coincidence Logic
85
Stub Formatter
80
Serializer
5
Periphery @ 320 MHz


Pixel Row 16
Binary readout
120
Memory
with
Gating logic
120
120
Pixel Row 16
Pixel Row 1
Binary readout
120
Memory
with
Gating logic
120
120
Pixel Row 1
120
120
Binary
Readout
FIFO
1920
1920
Recursive
MEPHISTO
Encoder
Periphery
@ 40 MHz
448
L1 Pixel Cluster (up to 31)
FIFO
Strip L1 Binary
Deserializer
144
144
Recursive
MEPHISTO
Encoder
448
240
Output Interface FIFO
(up to 31 pixel cluster and 24 strip cluster)
688
Serializer
Periphery
@ 320 MHz
1

Radiation Hardness requirement

- **Outer Tracker Max. TID: 100 MRad** (with no safety margin)
- 200 MRad Radiation model available thanks to M. Menouni (CPPM, RD53)
- Digital library results from DRAD chip, plot courtesy of L. M. Jara Casas (CERN, RD53)



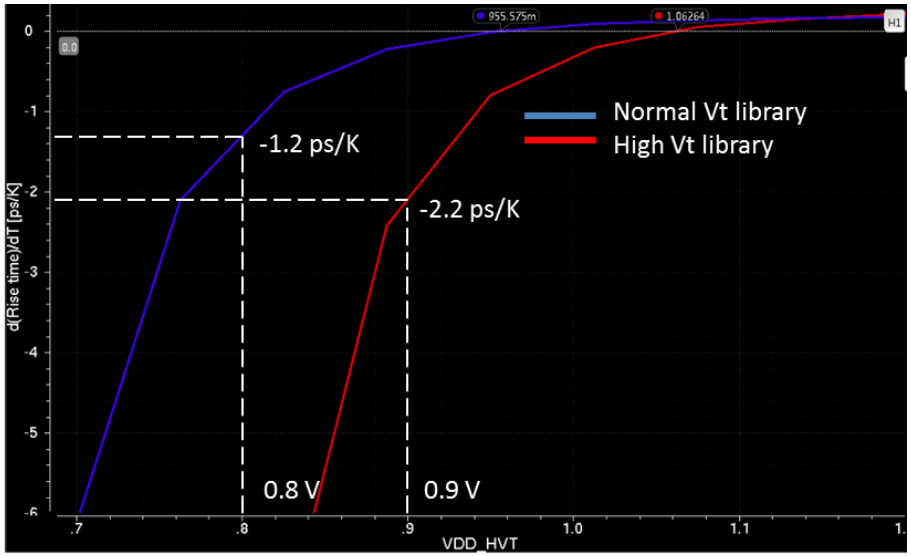


Corner requirements

Temperature inversion effect
"Under **low-voltage supplies**, the cell performance (delay, transition time, setup/hold time) at **-40 C is worse** than at 125." [from Tech.manual]

- Best: 1.1 V, 0 C FF
- Typical: 1 V, 25 C, TT
- Worst: 0.9 V, 125 C, SS
- **Worst Low Temperature: 0.9 V, -40 C ,** ⟵ **Slowest corner**

$\frac{\delta Delay}{\delta T}$

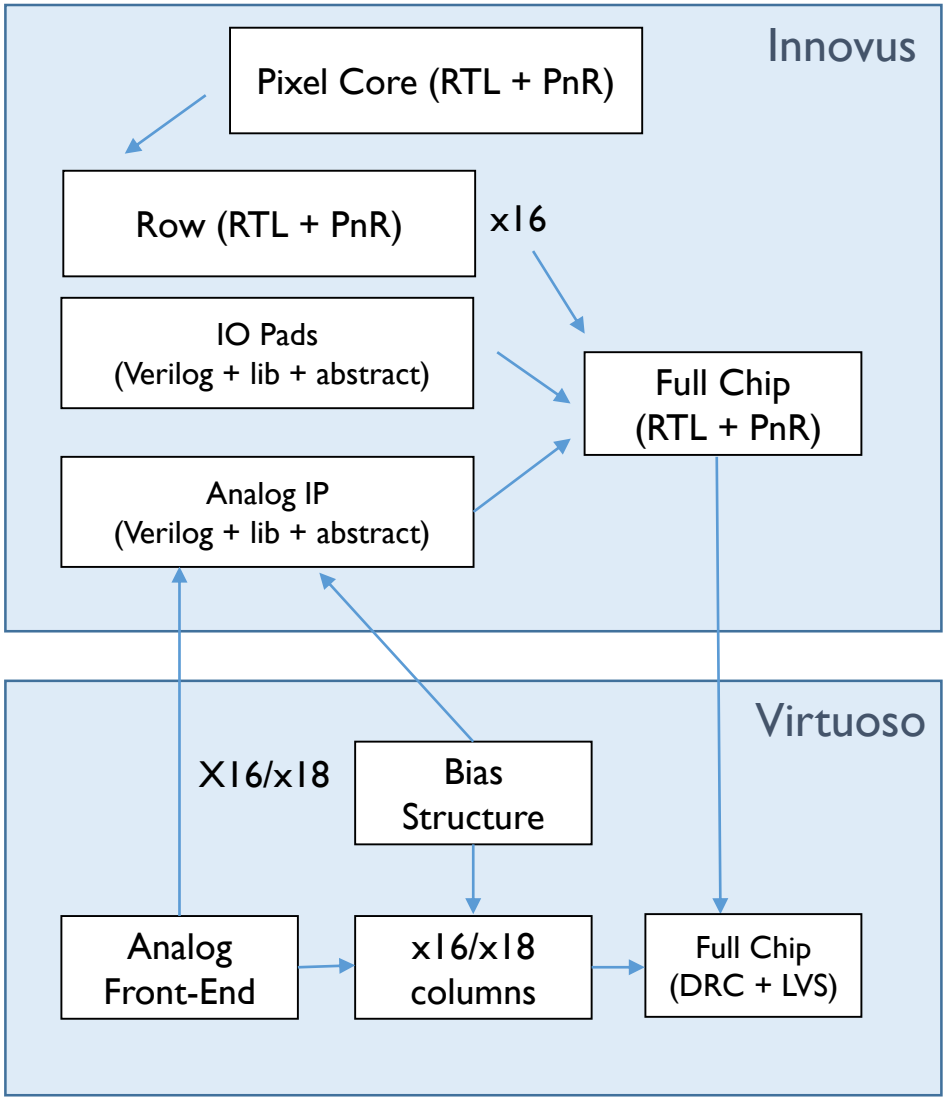


V_{DD}

Drain Current:

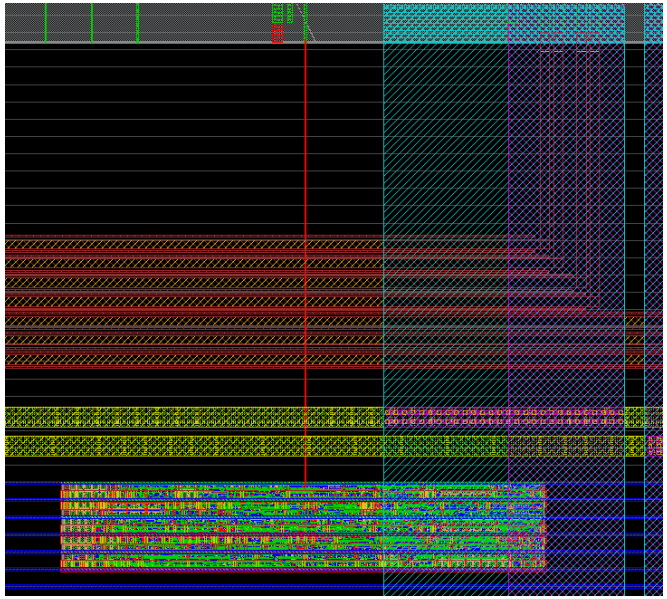
$$I_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

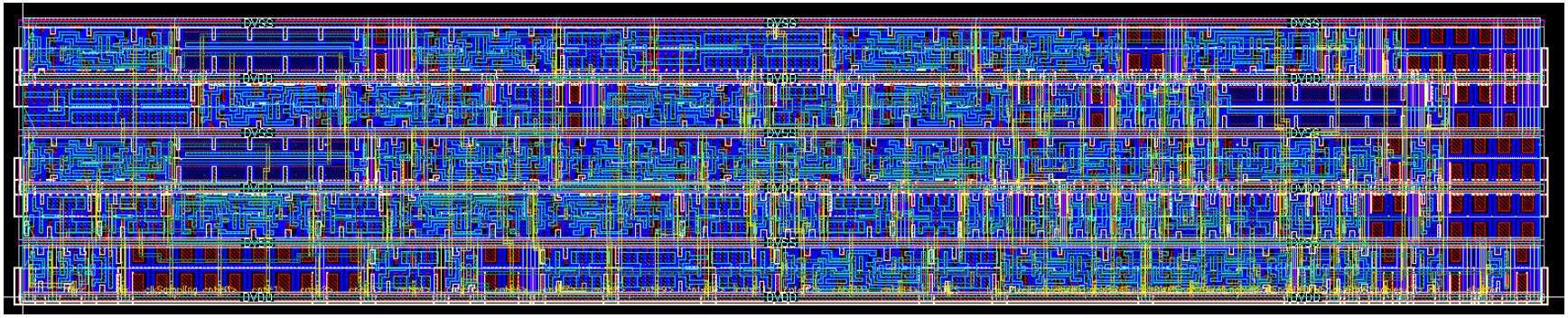
P&R Hierarchy



Pixel Core

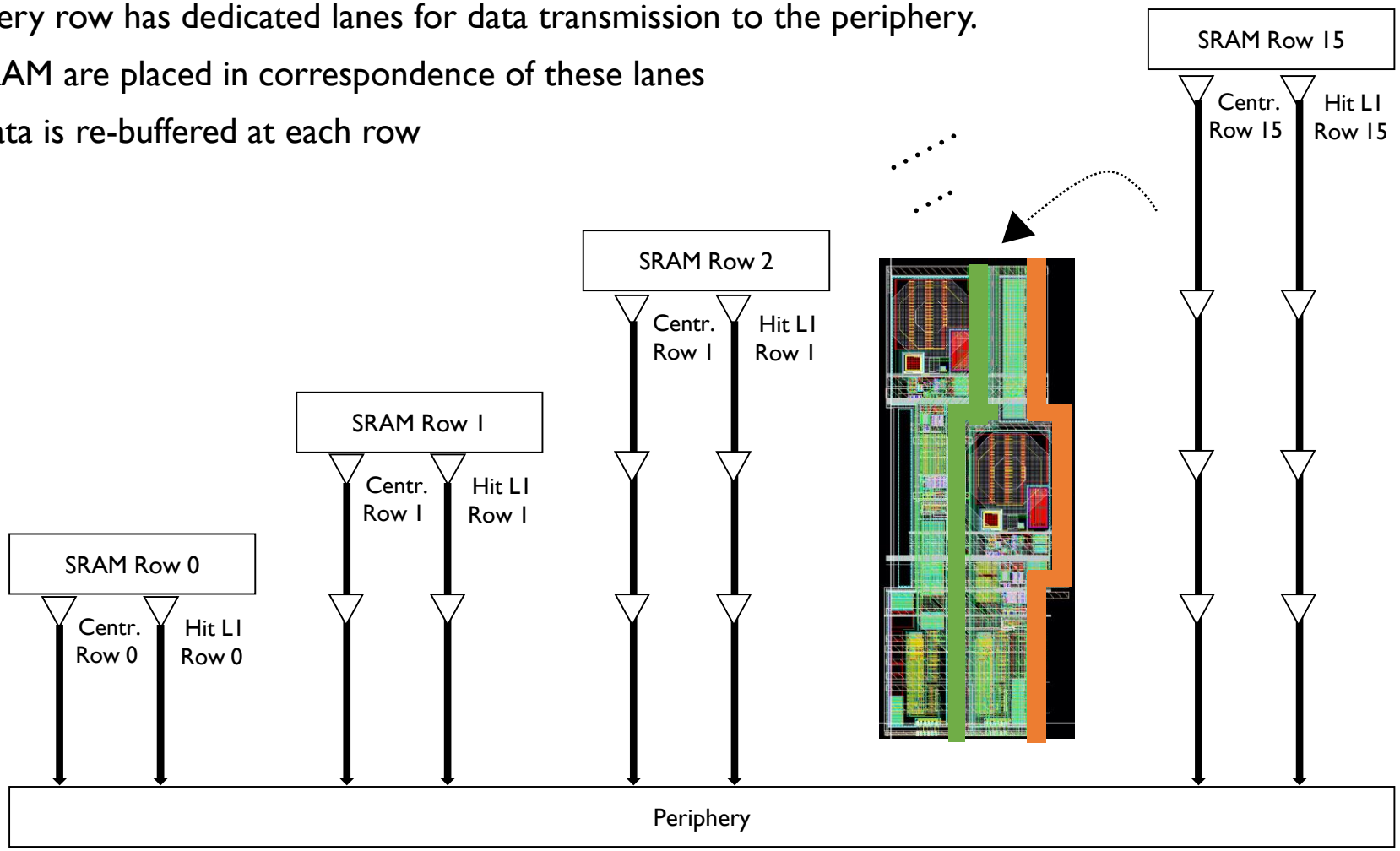
- Synthesized and PnR separately
- Integrated as Macro Block
- Placed and connected to FE manually
- Contains only FE electronics (no configuration)





Pixel Row

- Every row has dedicated lanes for data transmission to the periphery.
- SRAM are placed in correspondence of these lanes
- Data is re-buffered at each row



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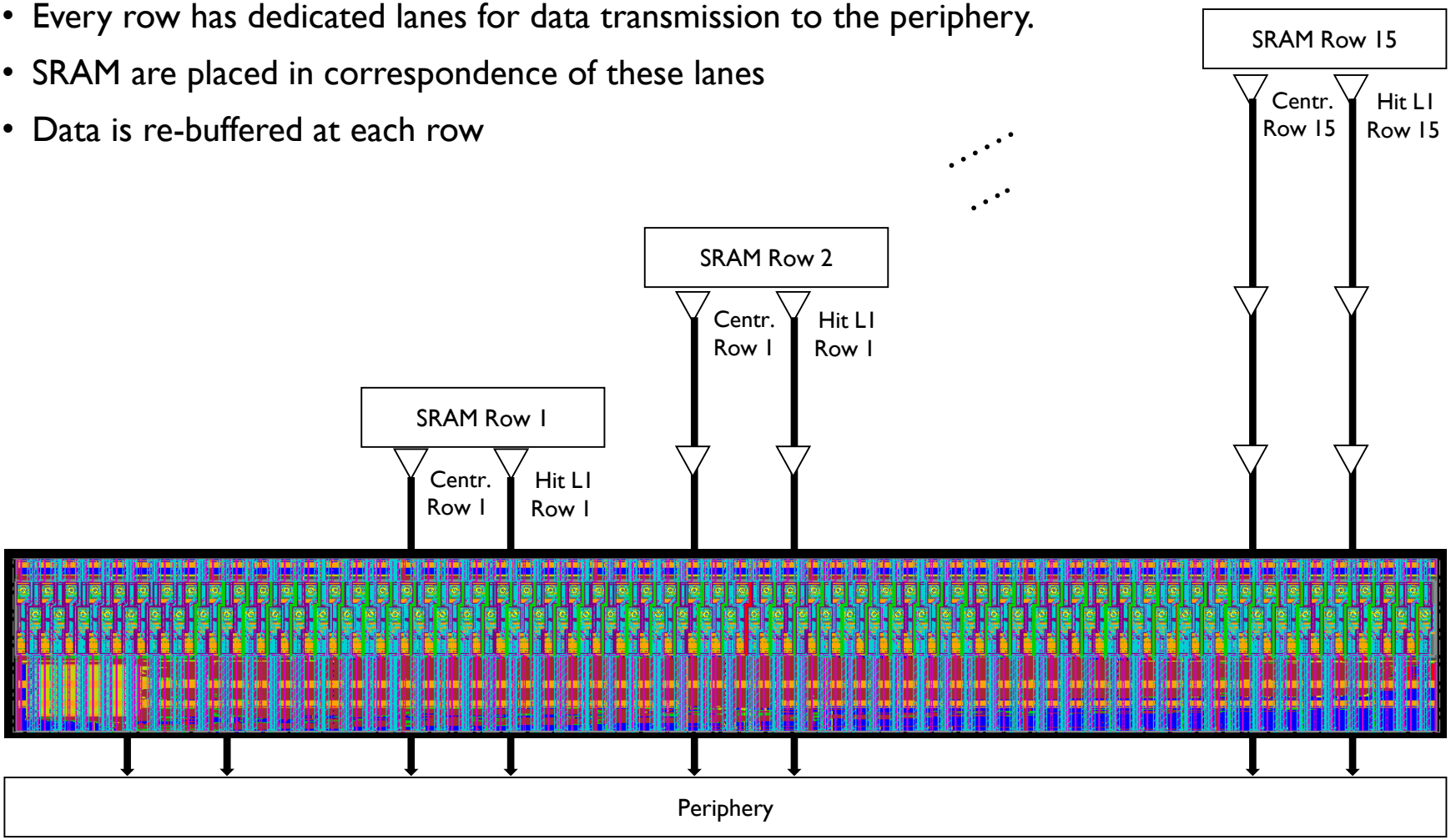

Periphery

Integrates:

- Bias Block
- Clock Buffer and data re-buffering
- DLL
- eFuse
- IO Pad Area
- Digital logic (flat approach)