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Characterization of the MPA prototype, a 65 nm pixel readout ASIC with on-chip quick transverse momentum discrimination capabilities.

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The first prototype of the full-size, full-functionality Macro Pixel ASIC has been prototyped in a 65 nm technology employing radiation tolerant techniques. It is a pixel readout ASIC designed for the Phase-II upgrade of the CMS Outer Tracker detector. It features novel on-chip particle discrimination capabilities allowing performing real-time event-driven readout of high transverse momentum particles at a 40 MHz rate. This data flow is complemented with a triggered and zero suppressed readout data path for the readout of full events at a maximum rate of 1 MHz. This contribution presents the functional and performance evaluation results obtained from silicon prototypes.

Summary

The MPA, Macro Pixel ASIC, is a pixel readout ASIC featuring on-chip particle discrimination capabilities. The first full-size, full functionality prototype employing radiation tolerant design techniques has been produced in an 8-metal 65 nm CMOS technology.

The design fulfills the requirements of the CMS Outer Tracker upgrade for the High Luminosity LHC (HL-LHC). The upgrade foresees to adopt the use of double layer sensors to facilitate the quick, on-detector, identification of high transverse momentum (pT) tracks (> 2 GeV/c) and their transmission to the L1 trigger system at the 40MHz bunch crossing rate. For the first time data coming from the Tracker will be used in the L1 trigger decision of a high luminosity hadron experiment. In parallel, a readout channel will transmit triggered events to the DAQ at a nominal average trigger rate of 750 kHz.

This contribution presents the characterization of the Macro Pixel ASIC prototype. Measurements on bare die and at wafer level show a noise of less than 200 e- and a gain of 75 mV/fC in average. The measured time-walk is less than 15 ns for an input charge ranging between 0.5 fC and 9 fC. The peaking time, which is tunable by the user, varies between 22 ns and 28 ns. The analog circuit power supply current, including the biasing circuits, is around 30 uA per channel. The digital functionalities are verified using an on-chip digital pattern generation circuit embedded in the pixel array and an external FPGA test board. The measured power consumption is in good agreement with the ASIC simulations and complies with the targeted power density of less than 100 mW/cm2.
Test beam measurements and measurements performed with radioactive sources using assemblies of single MPA chips with pixelated sensors confirmed the performance evaluation results obtained from the bare die. Radiation tolerance evaluation test are currently on going and will be presented.

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