Reliability test results of the interconnect structures of the front-end hybrids for the CMS Phase-2 Tracker Upgrade

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Outline:

1. Introduction
2. Test coupon design, test structures, test system
3. Summary of results
4. Problems found
5. Conclusion

CMS: Compact Muon Solenoid
The CMS Tracker Phase-2 Upgrade is required to adapt the CMS Tracker to the 3000 fb\(^{-1}\) total integrated luminosity and 14 TeV centre-of-mass energy of the HL-LHC.

Two main module types are being developed for the upgrade. The readout electronics are based on flexible hybrid circuits assembled on Carbon Fibre (CF) reinforced stiffeners for both modules.

**HL-LHC**: High Luminosity Large Hadron Collider; **2S**: Strip-Strip module; **PS**: Pixel-Strip module;
The Tracker environment where the hybrids will operate:

- Controlled low humidity.
- Coolant temperature at around -35 °C, operation temperature at around -20 °C.
- A few shutdowns of cooling plant per year, a few power cycles per year.
- High radiation dose for PS modules, lower for 2S modules (56 Mrad max [1]).
- Operation in a strong static magnetic field.

The planned lifetime of the electronics is **15 years**. The modules must remain fully operational during this period.

[1]: The Phase-2 Upgrade of the CMS Tracker Technical Design Report CMS-TDR-17-001
The hybrid circuits are:

- High Density Interconnect (HDI) flex circuits reinforced with CF stiffeners.
- Dielectric layers are 25 µm thick with 9 – 15 µm copper.
- **Smallest line width and spacing is 40 µm.**
- Via laser drill is 25 – 50 µm in diameter in a capture pad of 110 µm.
- Vias are filled with copper and staggered to increase reliability.
- Up to 3000 (PS) or 6000 (2S) signal interconnections in one circuit.
- **9 flip-chips are bump bonded on each hybrid ( ~6500 bump bonds on the 2S).**

HDI: High Density Interconnect; MPA: Macro Pixel ASIC; SSA: Short Strip ASIC; CIC: Concentrator ASIC;
Properties of carbon fibre stiffeners:

- Made from high tensile modulus, high thermal conductivity (800 W/m·K) fibers.
- Key thermal and mechanical components of the modules.
- CTE mismatch between the hybrid and the stiffener is a problem source.
- All the test coupon assemblies were affected by the problem.
- Different solutions are currently being investigated to solve the problem.

Delamination of stiffener during reflow due to CTE mismatch between different substrates.

CTE: Thermal Expansion Coefficient
Parts of the circuits where failure might occur:

- Solder connections of surface mount components.
- Via structures.
- Fine traces.

Fine line test structure with 45 µm lines.

Daisy-chain test flip-chip with 254 µm pitch.

Flip-chip test daisy-chain with via-in-pad structure.

Via daisy-chain test structure.
2. Test coupons – Design of the different coupons

Coupon #1 only one manufacturer.

- Impedance test (not used in the test).
- Via daisy-chain structures with 9504 vias staggered.
- Dummy flip-chip for assembly test.

Some were irradiated @ 1MGy.

Test coupons designed by M. Kovacs.

Coupon #3 only one manufacturer.

- Flip-chip daisy-chain structure with 5 x 317 bumps.
- Fine line test structure with two parallel nets and 45µm/50µm linewidth/spacing 1.6m total length.
- Via daisy-chain structures with 3564 vias staggered.
- Flip-chips with SAC305 bumps.
2. Test coupons – Design of the different coupons

- Three different circuit manufacturers and assemblers.
- Flip-chips with eutectic Sn63Pb37 balls.
- 2 sets manufactured with solder-mask defined pads.
- 1 set manufactured with copper defined pads.
- The flip-chip assembly on the #2 V coupons failed.

Coupon #2 from three different manufacturers.

Daisy-chain flip-chip with 317 Sn63Pb37 bumps.

Via daisy-chain structures with 1158 via staggered.

1.4m long fine line test structure is under the probe pads.

#2 Type test coupon instance

Top layer design of all #2 type coupons.

Inner layer design of all #2 type coupons.

Test coupons designed by M. Kovacs.
The Panasonic A35S connector family is planned to be used for the service hybrid to front-end hybrid data connection.

- 10 coupons were irradiated with 1MGy Gamma ray.
- 10 coupons were not irradiated.
- 5 coupons from each group had 5 connect-disconnect cycles before the tests.

Test coupon designed by B. Allongue.
## 2. Test coupons – Summary of test objects

<table>
<thead>
<tr>
<th>Coupon type</th>
<th>Flip-chip DC</th>
<th>Via DC</th>
<th>Fine line</th>
<th>Other</th>
<th>Pieces</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coupon #1</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>Irradiated</td>
<td>3</td>
</tr>
<tr>
<td>Coupon #1</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>-</td>
<td>4</td>
</tr>
<tr>
<td>Coupon #2V</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>SnPb, SM defined</td>
<td>11</td>
</tr>
<tr>
<td>Coupon #2E</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>SnPb, Cu defined</td>
<td>8</td>
</tr>
<tr>
<td>Coupon #2E</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>SnPb, Cu defined</td>
<td>6</td>
</tr>
<tr>
<td>Coupon #2A</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>SnPb, SM defined</td>
<td>14</td>
</tr>
<tr>
<td>Coupon #3</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>SAC305*, SM defined</td>
<td>17</td>
</tr>
<tr>
<td>Coupon #3</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>-</td>
<td>11</td>
</tr>
<tr>
<td>Conn. coup.</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Irradiated, 5 cycles</td>
<td>5</td>
</tr>
<tr>
<td>Conn. coup.</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Irradiated, no cycles</td>
<td>4</td>
</tr>
<tr>
<td>Conn. coup.</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>5 cycles</td>
<td>5</td>
</tr>
<tr>
<td>Conn. coup.</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>no cycles</td>
<td>5</td>
</tr>
</tbody>
</table>

*SnPb solder alloy was applied during assembly for the following coupons: (2005,3005,7007,13007).
The test system has two functional parts. A static resistance measurement and a dynamic resistance measurement system. The dynamic system uses Arduino Due boards to count the duration of resistance transients above 60 Ω. The static system uses Keithley multimeters and a switch to measure the resistance of 80 channels.
In order to be compatible with different test coupon runs, an interconnect board was designed which is compatible with all the test coupons. Shielded 34 pin ribbon cables with IDC connectors interconnect the test chamber’s inner part to the system.

Reference voltage is generated on-board and reference resistors are mounted for each channel. The reference voltage and the coupon voltage drop is measured by the Keithley 2000 multimeters.
The test thermal cycle is chosen to run from -35 °C to 65 °C with 15 minutes dwell time and ~7 °C/min temperature ramp. The thermal chamber used for the tests is a Climats Excal model. Dry air injection was activated to avoid condensation on the test specimens. The test system and the thermal cycle was set up using the guidelines from IPC-SM-785.

Similar climatic chamber to the one used for the tests [2]

Temperature profile of one thermal cycle.
3. Performance of the test system

The test system is equipped with three reference channels with 110 Ω reference resistors. The relative resistance measurement was very precise, less than 0.1% deviation was observed (air-conditioned room).

The resistance transient detection did not indicate failures before they were visible by the static measurement. Some failures were not indicated.

Resistance of reference is recorded for the full test duration.
The test system saves the data in CSV files. It measures the resistance of all 80 channels every 5 minutes. During 1000 thermal cycles it generates ~1 million measurement points. A Matlab script was created to load, sort and plot the data.

As the resistance of the test coupons is changing in function of the temperature, the resistance is averaged based on 144 measurement points. This averaging method relies on the absolute temperature of the cycles and it can drift with the absolute temperature of the chamber.

Resistance fluctuation caused by the temperature change.

Small deviation caused by the absolute temperature change.

Test software design by G. Blanchot.
# 3. Test results summary

<table>
<thead>
<tr>
<th>Via test structures</th>
<th>Failed at start</th>
<th>Failed after 100 cycles</th>
<th>300 cycles</th>
<th>500 cycles</th>
<th>700 cycles</th>
<th>1000 cycles</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coupon #1</td>
<td>0/5</td>
<td>0/5</td>
<td>0/5</td>
<td>0/5</td>
<td>0/5</td>
<td>0/5</td>
<td></td>
</tr>
<tr>
<td>Coupon #1 Irradiated</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td>0/3</td>
<td></td>
</tr>
<tr>
<td>Coupon #2A</td>
<td>1/14</td>
<td>1/14</td>
<td>2/14</td>
<td>2/14</td>
<td>2/14</td>
<td>2/14</td>
<td></td>
</tr>
<tr>
<td>Coupon #2V</td>
<td>0/11</td>
<td>0/11</td>
<td>0/11</td>
<td>0/11</td>
<td>0/11</td>
<td>0/11</td>
<td>15V slight incr. (4%)</td>
</tr>
<tr>
<td>Coupon #2E</td>
<td>0/14</td>
<td>0/14</td>
<td>0/14</td>
<td>1/14</td>
<td>1/14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Coupon #3</td>
<td>1/28</td>
<td>2/28</td>
<td>2/28</td>
<td>2/28</td>
<td>2/28</td>
<td>2/28</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Fine line test structures</th>
<th>Failed at start</th>
<th>Failed after 100 cycles</th>
<th>300 cycles</th>
<th>500 cycles</th>
<th>700 cycles</th>
<th>1000 cycles</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coupon #2A</td>
<td>1/14</td>
<td>1/14</td>
<td>2/14</td>
<td>2/14</td>
<td>2/14</td>
<td>2/14</td>
<td></td>
</tr>
<tr>
<td>Coupon #2V</td>
<td>0/11</td>
<td>0/11</td>
<td>0/11</td>
<td>0/11</td>
<td>0/11</td>
<td>0/11</td>
<td></td>
</tr>
<tr>
<td>Coupon #2E</td>
<td>1/14</td>
<td>1/14</td>
<td>1/14</td>
<td>1/14</td>
<td>1/14</td>
<td>2/14</td>
<td></td>
</tr>
<tr>
<td>Coupon #3</td>
<td>0/28</td>
<td>0/28</td>
<td>0/28</td>
<td>0/28</td>
<td>0/28</td>
<td>0/28</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Flip-chip test structures</th>
<th>Failed at start</th>
<th>Failed after 100 cycles</th>
<th>300 cycles</th>
<th>500 cycles</th>
<th>700 cycles</th>
<th>1000 cycles</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coupon #2A</td>
<td>0/14</td>
<td>0/14</td>
<td>0/14</td>
<td>0/14</td>
<td>0/14</td>
<td>0/14</td>
<td>Sn63Pb37 bumps SM-def.</td>
</tr>
<tr>
<td>Coupon #2E</td>
<td>0/8</td>
<td>0/8</td>
<td>1/8</td>
<td>5/8</td>
<td>5/8</td>
<td>8/8</td>
<td>Sn63Pb37 bumps Cu-def.</td>
</tr>
<tr>
<td>Coupon #2V</td>
<td>14/14</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Assembly failed.</td>
</tr>
<tr>
<td>Coupon #3</td>
<td>2/17</td>
<td>5/17</td>
<td>8/17</td>
<td>10/17</td>
<td>11/17</td>
<td>11/17</td>
<td>SAC305, mixed paste</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Connector test coupons</th>
<th>Failed at start</th>
<th>Failed after 100 cycles</th>
<th>300 cycles</th>
<th>500 cycles</th>
<th>700 cycles</th>
<th>1000 cycles</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conn A35S IRR 5CYC</td>
<td>0/5</td>
<td>0/5</td>
<td>0/5</td>
<td>0/5</td>
<td>0/5</td>
<td>0/5</td>
<td></td>
</tr>
<tr>
<td>Conn A35S IRR No CYC</td>
<td>0/4</td>
<td>0/4</td>
<td>0/4</td>
<td>0/4</td>
<td>0/4</td>
<td>0/4</td>
<td>1 slightly increased</td>
</tr>
<tr>
<td>Conn A35S 5CYC</td>
<td>0/4</td>
<td>0/4</td>
<td>0/4</td>
<td>0/4</td>
<td>0/4</td>
<td>0/4</td>
<td></td>
</tr>
<tr>
<td>Conn A35S No CYC</td>
<td>0/5</td>
<td>0/5</td>
<td>0/5</td>
<td>0/5</td>
<td>0/5</td>
<td>0/5</td>
<td>2 slightly increased</td>
</tr>
</tbody>
</table>
When a test structure is considered as broken/failed, it is important to analyze the failure method. Based on the nature of the failures, they can be grouped in four categories:

- Design problem.
- PCB manufacturing problem.
- Assembly problem.
- Via metallization or solder joint fatigue.

Design, PCB manufacturing and assembly problems can be fixed in the future if they are found during the reliability tests. Fatigue failures are related to the applied technology and materials and they determine the expected product lifetime. For lifetime analysis only fatigue failures can be considered.
4. Types of failures found

Design problem

The fine trace can crack close to the solder pad.

PCB manufacturing problem

Soldermask opening was not tuned to SM thickness.

Solder joints could not form between the PCB and ASIC.

Assembly and design problem

SnPb solder paste was used to assemble ASICs with SAC305 bumps.

Substrate warps due to CTE mismatch during reflow.
## 4. Types of failures found

<table>
<thead>
<tr>
<th>Coupon type</th>
<th>Solder pad fine trace crack</th>
<th>Too small soldermask opening</th>
<th>Warpage issue during assembly</th>
<th>Not yet investigated/unknown</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coupon #2A via daisy-chain</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Coupon #2E via daisy-chain</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Coupon #3 via daisy-chain</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Coupon #2A fine line</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Coupon #2E fine line</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Coupon #2V flip-chip daisy-chain</td>
<td>14</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Coupon #2E flip-chip daisy-chain</td>
<td></td>
<td></td>
<td></td>
<td>8</td>
</tr>
<tr>
<td>Coupon #3 flip-chip daisy-chain</td>
<td></td>
<td></td>
<td></td>
<td>11</td>
</tr>
</tbody>
</table>
• The PCBs tested so far showed good reliability. No via structures failed due to via fatigue, no fine line structures formed shorts or broke.

• The connector test coupons showed good reliability even after irradiation and 5 plug-unplug cycles.

• The test system can be operated reliably for the long duration tests.

• The analysis shows when the failures developed during the test.

• The test system can find the manufacturing/design/assembly failures.

• The resistance transient detection did not indicate some failures.

• Good surface flatness is a key point to achieve a reliable flip-chip assembly. The warpage problems need to be solved. Different solutions are being explored.

• The reliability of the different flip-chip assemblies cannot be compared due to the assembly problems, lifetime analysis is not possible for the flip-chip bonding.
5. Future work

- Continue thermal cycling of the samples which did not show failures.
- Analyze the failure methods of the coupon #2 E flip-chip daisy-chain (ongoing).
- Test coupons will be added to every new design. Thin connection to solder pad need to be improved.
- Solve flex warpage problem due to the CTE mismatch of stiffener and PCB.
- Prepare lifetime analysis when fatigue failures are found.
- Compare the reliability of different assemblies and technologies.
- Estimate expected lifetime in the tracker environment.
I would like to thank for the help of all the colleagues involved in this project:

- B. Allongue – connector test coupon design
- F. Andre – design of the DAQ software
- G. Blanchot – Analysis software design and project supervision
- R. Camus – Interconnection cabling of test coupons
- T. Gadek – useful ideas and design tips
- R. Gajanec – design of the test coupon interconnect board
- M. Sebastien – Preparation of cross section polishes and microscope images
- And many others with small or big favors...
There are many publications related to the reliability of lead-free solder joints, but limited resources are available about the reliability of flip-chips equipped with lead-free solder bumps. No literature is available about the reliability of CF reinforced flexible circuits. Reliability testing is required to control the quality of the circuits.

Conclusions from different publications:

• Under filled flip-chip assemblies should stay functional for 3-10 thousand thermal cycles with 100 °C temperature change.[3]

• Assemblies with lead-free alloy can outperform assemblies with Sn63Pb37 alloy.[3]