VULCAN READOUT CHIP
Test Strategy for Low Failure Rates and Status of a Highly Integrated Readout Chip for PMTs in JUNO

2018-09-18  |  A. ZAMBANINI
Introduction to JUNO

Concept of the **Vulcan** Readout Chip

Lab Verification Status of Vulcan

Test Strategy for Low Failure Rates

Summary and Outlook
THE JUNO EXPERIMENT

- **Jiangmen Underground Neutrino Observatory**
  - Jiangmen, China (near Hong Kong/Macao)
  - Planned start: 2022, duration of **6 years**
  - 2 nuclear reactors, baseline ~53 km

- **Multi-purpose neutrino detector**
  - Main goal: determine neutrino mass hierarchy
  - Energy resolution: 3% at 1 MeV
  - Central detector:
    - 20 000 t liquid scintillator (LAB)
    - **18 000 20” PMTs; ~36 000 3” PMTs**
    - Detector **submerged** in water to support weight
THE VULCAN CHIP DEVELOPED FOR JUNO

~18 000 large PMTs as intelligent PMTs
- Readout electronics submerged with PMT
- Lower bandwidth on the cable
- GCU (global control unit) as central control with ADU (analog to digital unit)

Highly linear, fully integrated circuit – Vulcan
- Sampling ADC with approx. 80 dB linearity
- No external components required
- On-chip clock generation from ref. clock

Precise signal reconstruction
- No analog delay line (reducing noise & distortion)
- Control loop to suppress DC variations
- Optional overshoot compensation

Key Parameter of Vulcan

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>65 nm CMOS</td>
</tr>
<tr>
<td>Active Area</td>
<td>22 mm²</td>
</tr>
<tr>
<td>Power</td>
<td>~ 1.2 W</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>&lt; 10 Ohm</td>
</tr>
<tr>
<td>Input Bandwidth</td>
<td>500 MHz</td>
</tr>
<tr>
<td>Sampling Rate</td>
<td>1 GSample/s</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>80 dB</td>
</tr>
<tr>
<td>ADC Resolution</td>
<td>3× 8 bit</td>
</tr>
<tr>
<td>High Gain</td>
<td>0.06 p.e./bit</td>
</tr>
<tr>
<td>Medium Gain</td>
<td>0.4 p.e./bit</td>
</tr>
<tr>
<td>Low Gain</td>
<td>8 p.e./bit</td>
</tr>
</tbody>
</table>

Vulcan: Son of Juno in ancient Greek mythology
**Signal Modes – Small & Medium Signals**

First two signal chains
- Parallel TIA input
- Programmable gains
- Combined input resistance of ~ 5 Ω
**Signal Modes – Large Signals**

Third signal chain
- Current > 20 mA
- TIA input saturates, ESD diodes open
- Voltage over diodes measured

![Diagram of signal modes and ADCs](image-url)
**Vulcan Design Status**

- Complete design (22 mm²) with
  - 3x receiver chain (TIA, 8 bit ADC)
  - 4 GHz on-chip PLL
  - Digital part with ~ 7 million transistors
  - 20 LVDS outputs

- Second engineering sample: **tapeout in Q3/2017**
  - Return in Q4/2017, lab verification since then
VULCAN LABORATORY SETUP
**Verification Board Concept**

**Verification Board**
- Main board for IC verification
- Best RF/Impedance performance
- Optimized for verification measurements

**Socket Board**
- Non-destructive measurement
- Limited performance measurements
- Functional tests

**PMT Board**
- For direct usage with PMT
- Protection circuit
- All 3 ADCs connected

**Main Board**
- Logic analyser connection
- Power supply connection
- JTAG interface
- DC measurements
- Samtec board to board connectors

**System Board**
- All 3 ADCs connected
- Protection circuit
- Reference design for system implementation
VERIFICATION BOARD IN ACTION

Main Board

Daughter Board
**ADC CHARACTERIZATION**

- Precise current source as input to Vulcan
- Equivalent DC input voltage
  - Measure ADC value
  - Mean, min, max
- Result:
  - Linear over all 4 sub-ADCs
  - Little spread per voltage
ADC Characterization

- Signal generator as input to Vulcan
- Sine wave with $f = 100\, \text{kHz}$
  - Also used for SNR & ENOB calculation (next slide)
- Output shows proper digitization in the full range
**Signal to Noise Measurement**

- **SNR w/o distortion**
  \[ \text{SNR} = 45.92 \, \text{dB} \]

- **ENOB w/o distortion**
  \[ \text{ENOB} = 7.48 \]
  (req.: 7.33 ENOB)

\[ \text{ENOB} = \frac{\text{SNR} - 1.76 + 20 \times \log_{10} \left( \frac{\text{Full\_scale}}{\text{Used\_scale}} \right)}{6.02} \]

SNR: signal to noise ratio
ENOB: effective number of bits
SINGLE PULSE MEASUREMENT

- Signal generator producing short rectangular pulse
  - Pulse shape different due to limited bandwidth
  - Amplitude and length equiv. to one photoelectron

Vulcan can detect realistic pulses
Reliability of Integrated Circuits

- Generally: product failures in different phases:
  - Infant mortality due to manufacturing defects
  - Normal life (covered by e.m. aware design)
  - Wear-out (covered by e.m. aware design)

- Manufacturing defects due to process variations
  - Varying between wafers and with position on wafer
  - Strong defects: not operational transistors or wires
    \[\rightarrow\] immediate impact on functionality
  - Weak defects: weakened wire that can wear out with time
    \[\rightarrow\] fails with stress on circuit

- Goal: filter out all unreliable ICs so that only stable ones survive
  - Foundry: test devices on wafer next to each IC (PCM); rigid visual inspection
**Electromigration-Aware Design**

- Material transport by gradual movement due to electron collisions
  - Dependent on current density in the conductor
  - Degradation of the metal over time
  - Leads to connection faults in the design

- Prevent by design methods
  - Use wider/multiple conducting wires
  - Use multiple vias instead of single vias

- Perform electromigration studies to estimate degradation prior tapeout
  - Based on IR drop simulation
  - Detailed current consumption analysis
  - Critical areas get easily visible
**Structural Scan Test**

- Digital part composed of combinatorial and sequential logic
  - Goal: test the *connectivity and functionality of digital gates*
  - Method: include scan chain(s) to determine faulty gates/connections

- Flip flops (FFs) exchanged by **scan FF**
  - Two modes of operation: reg. & scan
    - 1) Scan data loaded in scan chain; representing certain logic state
    - 2) Data is processed for 1 clock cycle
    - 3) Data shifted out to scan output

- **Scan patterns generated** by ATPG tool

- Detects single stuck-at-fault gates and delay faults
IDDQ TESTING

- Testing supply current ($I_{DD}$) in the quiescent state ($\rightarrow I_{DDQ}$)
  - Or: measuring the leakage current without digital activity
  - CMOS logic circuit draws current only during switching phase
  - Many production faults increase the current by orders of magnitude

- Easy and fast test
  - Filter devices with $I_{DDQ} < I_{DDQ\_thr}$ (> 95% coverage)
**Voltage Stress Testing**

- Induce artificial stress to extract weak devices

- **Very low voltage (VLV) test**
  - Operation with lower than normal voltage
  - Identify resistive shorts and thin oxide layers
  - Performance of weak devices affected more

- **Short voltage elevation (SHOVE) test**
  - Short bursts with higher than normal voltage (10% - 20% increase)
  - Brief moments of higher current
  - Critical areas (thin oxide regions) will wear out fast
  - IDDQ test results are affected in weak devices (> 95% coverage)
**Performance Testing**

- Quantify the overall performance with **key parameters**
  - PLL frequency and oscillator voltage
  - DAC: INL / DNL
  - ADC: Offset and gain errors
  - … and more

- Pick **best samples**, targeted ratio: 1 out of 3
  - Samples surviving all tests are strongest
    - Suppressing infant failures
    - Confirmed with manufacturer
  - Similar procedure as in automotive industry for reliability assurance

*Effectively, device faults are completely suppressed!*
SUMMARY AND OUTLOOK

- **Vulcan 2nd engineering sample produced**
  - Readout solution developed for PMTs in JUNO
  - 3 receivers with programmable gain (1 GSample/s, 7.48 ENOB)
  - Ongoing verification in the lab

- **Verification concept for low failure rates**
  - Production test developed based on industry standards
  - Extensive selection procedure ensures high reliability
    → **No Vulcan faults expected** for JUNO runtime

- Next step: finish lab verification

- No further iteration planned at this moment
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EXTERNAL SOURCES

• Slides 3-4: Conceptual Design Report, JUNO Collaboration (v2, 2015) & JUNO Collaboration Default Slides
  https://arxiv.org/abs/1508.07166

• Slides 8-14: Measurement results mainly achieved by Christian Roth

• Slide 15: Bathtub curve, Wikipedia (version from 02.08.2009)
  https://commons.wikimedia.org/wiki/File:Bathtub_curve.svg

  http://jes.ecsd.org/content/152/1/G45.full (DOI: 10.1149/1.1828419)

• Slide 17: Scan chain visualization, AnySilicon website (accessed Feb. 2017)
  https://anysilicon.com/overview-and-dynamics-of-scan-testing/
3 types of neutrinos with squared masses $m_1^2$, $m_2^2$, and $m_3^2$
Absolute masses of neutrinos unknown
Mass differences are known: $\Delta m_{12}^2 = m_2^2 - m_1^2$ and $|\Delta m_{13}^2| = |m_3^2 - m_1^2|$
$|\Delta m_{13}^2|$, no sign known $\rightarrow$ 2 possible mass hierarchies (MH)
Measurement of neutrino mass hierarchy:
$\rightarrow$ confirm normal hierarchy (NH) or inverted hierarchy (IH)
PHYSICS MOTIVATION

Measurement of Neutrino Mass Hierarchy

- Phase of oscillation different for NH and IH
- Discrimination of NH and IH by $\Delta \chi^2_{\nu_{MH}}$ by measurement:
  - $\Delta \chi^2_{\nu_{MH}}$ improves i.a. with energy resolution (design: 3%/sqrt(E/MeV))
  - → good energy and waveform reconstruction needed
OVERSHOOT COMPENSATION

- Signal distortion by AC coupling
  - Inter-symbol interferences
  - Reduced signal to noise ratio

- Optional compensation in Vulcan
  - Additional coupling cap. at the bias resistor
  - Sensing voltage over bias resistor ($R_{bias}$)
  - Compensation current generated by a copy of the bias resistor ($R_{bias2}$)
ADC PERFORMANCE REQUIREMENTS

• Noise requirements
  – From Conceptual Design Report:
    “Noise level should be below 0.1 p.e. for single photoelectron detection”
  – Vulcan: 8 bit for first range (0-16 p.e.)

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<th>ENOB</th>
<th>Range [p.e.]</th>
<th>Resolution [1/p.e.]</th>
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<tbody>
<tr>
<td>8</td>
<td>16</td>
<td>0.0625</td>
</tr>
<tr>
<td>7.33</td>
<td>16</td>
<td>0.1</td>
</tr>
<tr>
<td>7</td>
<td>16</td>
<td>0.125</td>
</tr>
<tr>
<td>7</td>
<td>14</td>
<td>0.109</td>
</tr>
</tbody>
</table>
## ADC Performance Requirements

- **Noise requirements**
  - From Conceptual Design Report:
    - Noise level should be below 0.1 p.e. for single photoelectron detection
  - Vulcan: 8 bit for first range (0-16 p.e.)

- **Time requirements**
  - From Conceptual Design Report:
    - Waveform sampling should be available over the whole energy range with a sampling rate of 1 GS/s.
  - Vulcan: 500 MHz sampling, both edges

- **Configurable: sampling or integrating ADC**

### ENOB | Range [p.e.] | Resolution [1/p.e.]
---|---|---
8 | 16 | 0.0625
7.33 | 16 | 0.1
7 | 16 | 0.125
7 | 14 | 0.109
VERIFICATION BOARD CONCEPT

Main Board

Verification Board or Socket Board or PMT Board or System Board
VERIFICATION BOARD

Samtec Supply Connector

Samtec LVDS Digital Connector
**Socket Board Setup**

- Yamaichi Socket for functional testing
VERIFICATION RESULTS OF VULCAN ES2

- LVDS Data Lines
TRANSIMPEDANCE AMPLIFIER INPUT IMPEDANCE
Full Range ADC DNL (low Gain)
Full Range ADC INL (low Gain)

Vulcan 2.0 RX1 ADC + TIA INL (Integral nonlinearity) Measurement ($TIA_{\text{Input}}$ to $ADC_{\text{Output}}$)
STRESS TESTING FOR LAYOUT VERIFICATION

- Classical temperature stress test (*burn-in*)
  - High temperature during operation favors electromigration
  - Faster aging, but still long measurement time until first failures (few years)
    → not feasible for JUNO schedule

- Alternative approach: *burn-in light*
  - A few samples O(100) operated in high temperature
    - Samples won’t be used in JUNO
  - Goal: verify layout regarding electromigration
  - Also possible: verify the selection procedure
Insert additional grid layers
IR DROP ANALYSIS – CURRENT LIMITS