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Test strategy for low failure rates and status of a highly integrated readout chip for PMTs in JUNO

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The Jiangmen Underground Neutrino Observatory (JUNO) is a multi-purpose underground experiment to determine the neutrino mass hierarchy as the main objective. The signal detection is performed by photomultipliers with readout electronics close to them. Therefore, a highly integrated analog-to-digital conversion unit with low power and large dynamic range is developed for PMT integration. To achieve the resulting need for a low failure rate a new test strategy is proposed. Various methods to increase the test coverage, which are implemented in the chip are presented. Also, appended features and measurement results from the second generation of the readout chip are presented.

Summary

The Jiangmen Underground Neutrino Observatory (JUNO) is an upcoming neutrino detection experiment located in China that aims to determine the neutrino mass hierarchy by detecting reactor antineutrinos from two nearby nuclear power plants. The central detector is a liquid scintillator with a mass of 20,000 ton and is situated with 700 meters rock overburden. It is surrounded by 18,000 20-inch photomultipliers (PMTs) that are designed to detect the produced light with high timing and energy resolutions while being submerged in water. For the discussed readout chip, the electronics is aimed to be integrated into the PMT housing to preserve signal quality and reduce the number of cables in the detector.

The readout chip called Vulcan is a highly integrated analog-to-digital conversion unit that is developed in 65 nm TSMC CMOS technology with three parallel 1 GSample/s 8-bit ADCs that include programmable gain pre-amplifier inputs. Combining the three ADCs, a linear voltage input range of more than 80 dB is achieved. After digitization and signal processing, the signal is forwarded above water.

The detector volume is submerged in a water tank which prevents the replacement of system components during the run time of the experiment. This in turn sets the requirement of the electronics connected to the PMTs to have extremely low failure in time value. The specification for the electronic readout in JUNO is set to maximum of 95 devices in the first six years of operation. For the capability to meet the demand for highly reliable devices, a special test strategy for the 18,000 readout chips is proposed.

Production tests majorly test for strong defects in the silicon, which causes functional errors or critical performance reduction on the chip. While the defects introduced during the manufacturing process of the digital logic can be spotted using scan chains, test structures like built in self-test can be used to verify the chip's functionality.

Usually, only critical performance that cannot be guaranteed by design is tested during production. The proposed test strategy looks at the performance of the circuitry so that weak defect causing early failures are spotted. The design for testability includes structures such as: scan chain, programmable waveform generators and programmable digital to analog converters. These elements were specially introduced into the Vulcan chip.

The design for test structures introduced in the Vulcan chip and the possibilities of measurement offered by test structures will be presented. This includes also different digital assisted alignment loops, which are used to find optimal settings before the tests can be performed. Alongside, measurement results of the digital part of the second chip version will be presented and compared to the system requirements.

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