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Upgrade of the CMS Barrel Muon Track Finder for HL-LHC featuring a Kalman Filter algorithm and an ATCA Host Processor with Ultrascale+ FPGAs

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The CMS Barrel Muon Track finder is a component of the Level-1 Trigger which performs track reconstruction and momentum measurement in the central region of the CMS experiment.
The current algorithm uses precalculated look-up tables to estimate the track parameters. A new approach will be presented deploying a Kalman filter algorithm that
exploits DSP resources in modern FPGAs, is prototyped in C using High Level Synthesis tools, and is implemented and tested in the current running CMS trigger.
A versatile ATCA platform featuring Ultrascale+ FPGAs and high speed fly-over optics proposed to host this algorithm in HL-LHC will be discussed.

Summary

The CMS Barrel Muon Track Finder (BMTF) is a component of the Level-1 Trigger which performs the identification and selection of muons and the determination of their transverse momenta and location in the central (Barrel) region of the CMS experiment. The Track Finder uses track segment information of candidate muons, delivered by the local trigger electronics of the Drift Tube and RPC chambers in the barrel region of CMS. The legacy track finding algorithm is using precalculated extrapolation and assignment look-up tables (LUTs) and η-patterns, estimating the muon trajectories by extrapolating from the innermost to the outermost muon detector stations while applying vertex constraints. A new approximate Kalman Filter algorithm has been proposed for the Phase II CMS upgrade that improves the L1 muon reconstruction performance and enables triggers of displaced particles. The algorithm is implemented in C with High Level Synthesis tools and exploits the DSP resources to perform multiplications needed
by the Kalman filter with high speed and low resource utilization. After the first implementation of the algorithm in Ultrascale+ FPGAs it was realized that an implementation in the FPGAs used in the current trigger (Virtex 7 690T-2) is feasible. This implementation was pursued and it was found that it is possible to implement both the legacy and the Kalman algorithm in the current system running in parallel and reading-out the output of both track finders in the DAQ. This parallel running is used to evaluate the physics and firmware performance of the algorithm towards a replacement of the legacy track finder in future LHC runs and in HL-LHC. The firmware implementation of the algorithm will be discussed along with its performance on resource utilization and latency in different FPGAs targeted for HL-LHC. In addition, the algorithm performance and the validation of the High level synthesis firmware in the current LHC run will be presented.
Given the performance on muon reconstruction algorithms in FPGAs and the low resource utilization achieved by exploiting efficiently all resources (including DSPs) a versatile ATCA processor will be presented that will form a platform to study
algorithms for the muon reconstruction in HL-LHC. The processor design utilizes cost-optimized Ultrascale+ FPGAs of high speed grades ideal for high latency sequential algorithms (e.g Kalman filter)
and high speed optical links up to 28 Gbps featuring the Samtec firefly technology.

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