Improved Time-to-Digital Converter (TDC) for a new generation of Resistive Plate Chamber (RPC) detectors

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Outlook

- Proposed RPC for CMS muon upgrade at high eta
- TDC specifications
- Development of FPGA TDC
- Conclusion and perspectives
Introduction

CMS muon upgrade at high eta

72 chambers to equip area with $1.8 < |\eta| < 2.4$

- Add track hits in muon reconstruction
- Search for Heavy Stable Charge Particle

[C. Combaret, RPC2018]
Introduction

Proposed double gap RPC

Top RPC

Bottom RPC

PCB with pick-up strips readout on both sides

Readout board

Principle of the readout electronics

On-detector Strip

Off-detector Strip

Y-position determination

\[ Y = f(t_{ext} - t_{int}). \]
Introduction

Small size prototype + readout board

- 32 strips of 3 mm width (4 mm pitch)
- 2 TDC board of Tsinghua University
- 2 32-ch petiroc
- Off-detector Strip

30.8ps@tdc1-td0=>30,8/√2=22 ps

TDC mezzanine based on Cyclone II with 18ps RMS (wave union A)

large size prototype + readout board

In-beam Work in progress

48 strips

1 32-ch petiroc + 1Tsinghua TDC board

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Specifications and FPGA choice

Requirement for FPGA-based TDC solution

- Multi-channel (65, 33 or 49) TDC
- Time-over-threshold (ToT): improvement of time resolution and charge measurement
- Leading and tailing edge resolution (RMS) : < 40ps
- Dead time : < 10 ns
- Minimum pulse width : a few ns

Solution based on Cyclone V

28-nm Cyclone V-GT FPGA:
- Support GBT protocol,
- Low cost,
- Low consumption
Tapped-delay-line TDC

Typical architecture

- Measured signal
- Calibration signal
- Carry chain based delay line
- Encoder
- Synchronisation from fast to slow clock domains
- Look up table
- Coarse time counter
- Fine time
- Coarse time

TDC clock domain

Slow clock domain
Delay-line implementation

Issue of implementation of tapped delay line due to low cost and low consumption

- More than one thousand of transition bits (3 cycles) when measured signal enters directly delay line

**Cause** (due to its characteristics)

1. $T_t >> T_e$: Increasing of the transition time after passing through each logic element or interconnect network AND Relative long transition time
2. Loop back noise (DL-DFFs change state) via LAB interconnect network (not local interconnect network)

**Observation**

E.g. input signal to FPGA

E.g. input signal to delay line

$T_t$ : transition time

$T_e$ : effective delay element

Expected output vs. Real output

TDC clock

ADDER

Adaptive Logic Module (ALM)
Proposed solutions

- Signal reshaping and loop-back noise blocking by using D-type Flip Flop

![Diagram of Delay-line implementation]

Original signal

Reshaped signal

**Dedicated route**

- A(0)
- Cin(0)='0'
- B(0)='1'
- Cout(0)
- Sum(0)

**Half ALM**
Delay-line implementation

Proposed solutions

- Using dedicated route to transfer signal from output of DFF to the input of delay line

![Circuit Diagram]

Location: FF_X*_Y*_N2

Reshaping DFF
Delay-line implementation

Achievement

- Reducing the transition bits to ~ 23bit by **reshaping** the input signal as well as **blocking** the loop-back noise
- Improving resolution from **32ps** to **10ps** for the leading edge due to **reshaping** signal
# Encoder implementation

<table>
<thead>
<tr>
<th>Issues</th>
<th>Solutions</th>
</tr>
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<tbody>
<tr>
<td><strong>23 bit noise after signal transitions</strong> =&gt; impossible to use the converter from thermo-code to one-hot code</td>
<td>Detection of the first signal edge in short time windows (64 bits) around the signal transitions</td>
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<tr>
<td>Minimize the consumption of FPGA resources</td>
<td>Separate encoder for leading and falling edges</td>
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<tr>
<td>Minimize pulse-width limit (a few ns)</td>
<td></td>
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## TDC clock domain

- 64bit
- Leading edge encoder
- Trailing edge encoder
- Slow clock domain

## Down sampling

- (N+1)*32-1
- N*32-1
- (N-1)*32-1

## Leading edge (OR 4bit)

- ‘0’
- ‘1’
- ‘1’
- ‘1’
- ‘1’
- ‘1’
- ‘0’

## Trailing edge (AND 4bit)

- ‘0’
- ‘0’
- ‘1’
- ‘1’
- ‘1’
- ‘0’
- ‘0’

**ATTENTION**: special treatment for the beginning
**Setup**

- **Pulse generator** (Keysight 81150A)
- **Clock input**
- **FPGA**
  - TDC 0
  - TDC 1
  - FIFO
  - RS232
- **Pc (Python)**
- **Cyclone V GT FPGA development board**

TDC provides time of leading edge and trailing edge.
Measurement

Result obtained

Leading edge (TDC0 - TDC1)

Measured RMS : 14,5 ps
RMS of TDC0 or TDC1 : 14,5/√2 = 10,35 ps

Trailing edge (TDC0 - TDC1)

Measured RMS : 20,5 ps
RMS of TDC0 or TDC1 : 18/√2 = 14,6 ps

TOT of TDC0 for the 8ns pulse width

Measured RMS with source jitter : 18,1 ps
Theoretical value: √(14,6^2 + 10,35^2) = 17,9 ps

Result:
- Time resolution of the leading edge is about 30% better than the one of the trailing edge
- Improvement foreseen on the trailing edge

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Measurement

Result obtained

Need for better source to measure TOT for pulse widths lower than 2ns
Conclusion and perspectives

Conclusion

Successful development of the ToT measurement on Cyclone V by using

- signal reshaping of the measured signal
- Use of a dedicated route for the input signal of the delay line,
- edge-detection and encoding in time windows around signal transitions

perspectives

- Finalization of the TDC calibration with a better source
- Integration TDC to the DAQ firmware
- In-beam test

Thanks for your attention
Back up
Issues on implementing delay line for Cyclone VI

### Noise
- At the beginning of the delay line with ~3 bin width (limit by 60nm technology)
- Due to the input signal pass through LAB interconnect network,
- No more thank to the dedicated carry-chain as well as relative large input load

### Bubble
- Max 1 bin width
- E.g. sig on delay line
- Transition zone