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Improved tapped-delay-line Time-to-Digital Converter (TDC) with time-over-threshold (TOT) measurement for a new generation of Resistive Plate Chamber (RPC) detectors

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For developing a new generation of Resistive Plate Chamber detectors, we present here an improved tapped-delay-line Time-to-Digital Converter (TDC) for time-over-threshold (TOT) measurement, which has been implemented on a low-end, 28nm cyclone V-GT FPGA. Our proposed approaches include signal reshaping and optimized routing, as well as edge-detecting and encoding only a small segment of signal around edge. The latter saves at least 50% of the FPGA's hardware resource (for each channel). Preliminary tests on the FPGA have shown 12-ps time resolution for leading and trailing edges and 20-ps resolution for TOT measurements with 2-ns pulse duration, and 5-ns dead time.

Summary

For CMS RPC (Resistive Plate Chamber) upgrade that is a part of the CERN CMS (Compact Muon Solenoid) muon upgrade project, it has been suggested to equip the high η muon stations for HL-LHC with a new generation of detectors. For this purpose, a new generation of RPC with high-rate capability and improved spatial and timing resolution has been proposed. Recent developments include two prototypes with associated readout electronics (including Cyclone II FPGAs to implement Time-to-Digital Converter (TDC) to fully exploit the RPC fast timing capability). Although the operation of both systems has successfully been tested with beam at CERN, their integrated TDC does not meet the requirements for 64-channel/module and a capability of measuring detected signal's pulse width (PW) down to a few ns. For the latter requirement, it is also known as time-over-threshold (TOT) measurement and is about the capability of measuring the signal charge if PW resolution is sufficient. Knowing the signal charge will improve accuracy of time-of-arrival time measurement.

We propose here an improved TDC with implementation of TOT measurement using one single tapped-delay-line TDC channel (mainly delay line, fine-time encoder and look-up table memory). The proposed TDC was designed to have a time resolution less than 45ps for leading and trailing edges for PW determination, with a dead time of less than 10ns.

Our proposed TDC is based on a low-power, low-cost, 28-nm Cyclone V-GT FPGA, which supports GBT protocol for our application. The main issue of this type of low-end FPGA for TDC implementation is its relative long transition time when the signal pulse is propagated to the TDC input. The transition segment of delay line can be as large as several hundred bits. This is because the transition time after passing through each logic element or unit (matrix switch etc) is increased. Our proposed solution to this issue is to reshape the signal pulse to be measured by using an edge-detecting logic followed by a flip-flop, whose output is routed directly to the delay line input (without passing through any logic element). This improves the time resolution from 32-ps to 12-ps and minimizes the transition segment to two dozens of bits. In order to minimize the consumption of FPGA resources per TDC channel, our approach consists in detecting signal edges and then retaining only a small portion of the signal around the detected edge in only two TDC-clock cycles. The retained segment is then encoded in one slow-clock cycle. This approach can save at least 50% of the FPGA's

hardware resource (for each channel).
Preliminary tests on the FPGA have confirmed the following improvements: 12-ps time resolution for leading and trailing edges and 20-ps resolution for TOT measurements for a 2-ns pulse duration, with a 5-ns dead time. A board incorporating the FPGA has been designed. Its fabrication and testing have been scheduled. We expect to undertake first beam test on the whole RPC system before the end of 2018.

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