A Multi-Layer SEU Mitigation Strategy to Improve FPGA Radiation Robustness for ATLAS Upgrade

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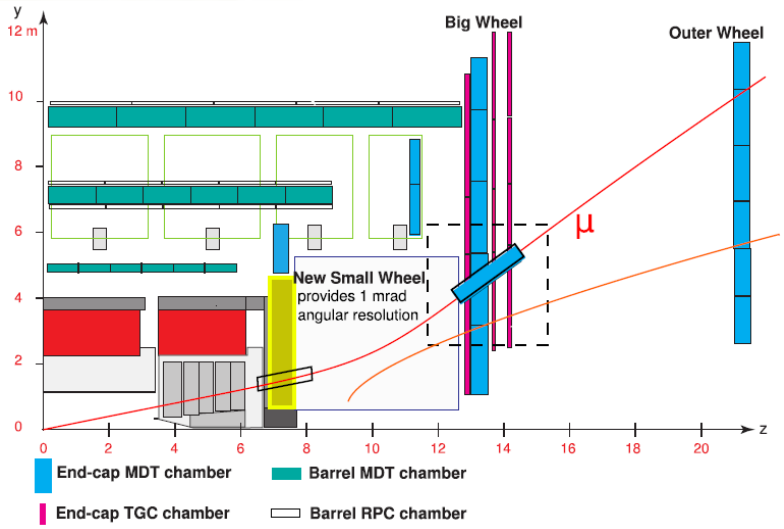
Outline

- Introduction
  - sTGC Router @ NSW
  - Radiation Environment @ sTGC Router
- Multi-Layer SEU Mitigation Scheme
  - Logic level
  - Device level
  - Board Level
- Artix-7 SEU Test System
  - Hardware
  - Firmware
  - Software
- Artix-7 Experimental Test Result
- Summary

sTGC Router @ New Small Wheel

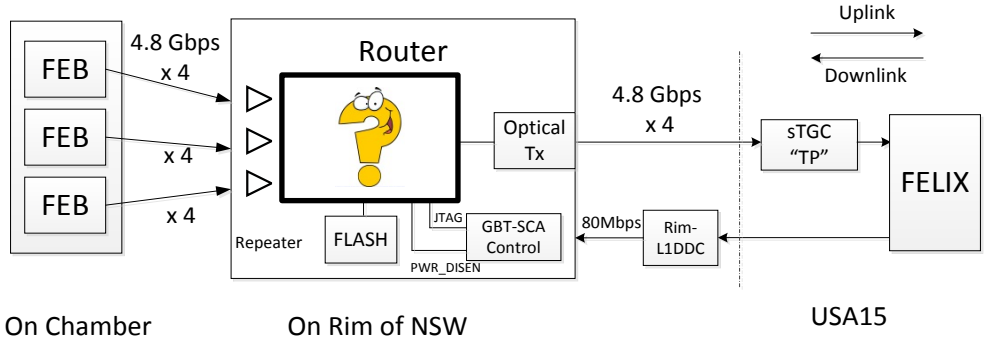
❑ ATLAS NSW Phase I Upgrade

- Filter out fake tracks
  - Reconstructing track vectors in NSW
  - Match to vectors in the BW
- Provide a segment measurement at NSW with 1mrad angular resolution



❑ sTGC Signal Packet Router

- Functionality:
  - Route active strip signals from FEB strip TDS to trigger processor at USA15 and drop NULL packets
- Central Processing Unit:
  - Fixed latency: trigger chain
  - 12-to-4 fast switching: limited bandwidth
  - Gita-bit transceivers: 4.8Gbps data flow



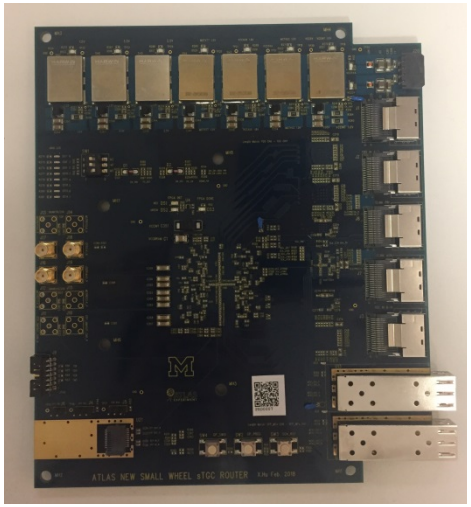
sTGC Router @ New Small Wheel

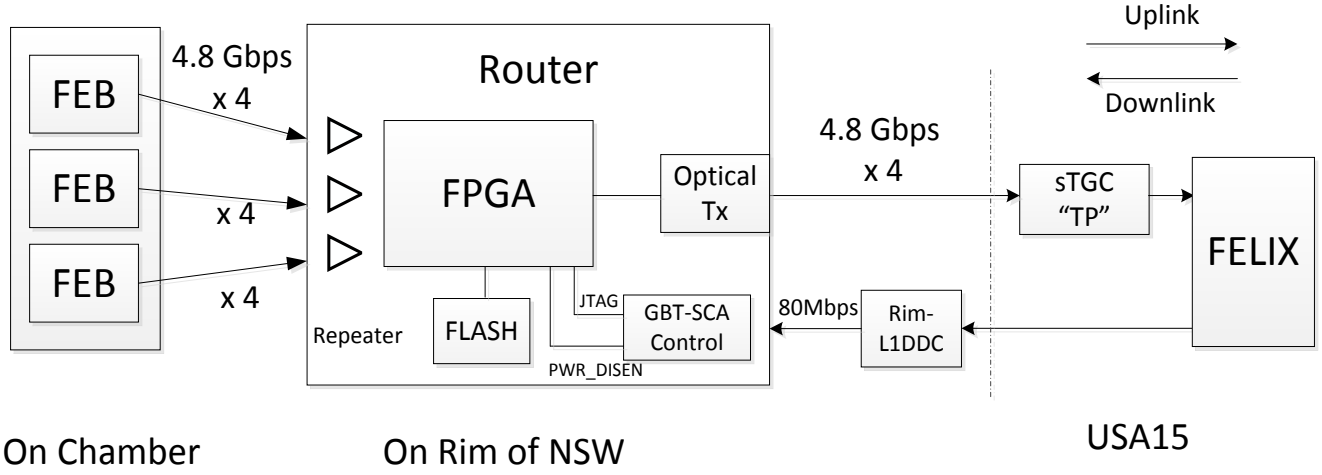
❑ sTGC Signal Packet Router

➢ FPGA or ASIC?

FPGA-based design: Reduce cost, short development cycle, flexibility of updating application in field

Sensitive to radiation effects: TID, SEE…





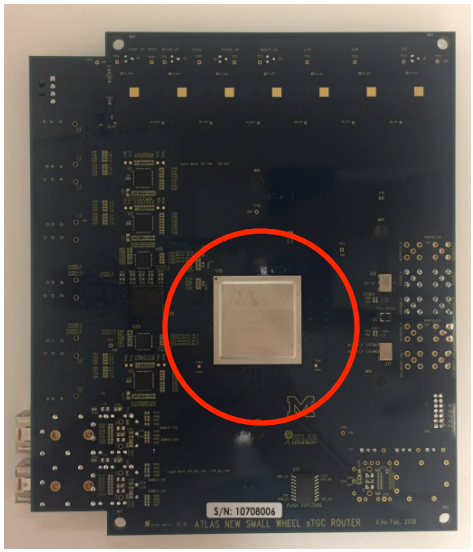


Illustration of serial signal streams through one router in the NSW

Radiation Environment @ sTGC Router

❑ ATLAS Radiation Tolerance Criteria @ NSW OUTER RIM

- NSW Simulated Radiation level

New Small Wheel Simulated Radiation Loads and Magnetic Fields

		Inner Rim ($R = 1\,\mathrm{m}$)	Outer Rim ($R = 5\,\mathrm{m}$)
TID	(γ)	$460\,\mathrm{Gy}$	$16\,\mathrm{Gy}$
NIEL	(fast neutrons)	$2.3 \times 10^{13}\,\mathrm{n/cm^2}$	$7.3 \times 10^{11}\,\mathrm{n/cm^2}$
SEE[1]	(protons)	$4.2 \times 10^{12}\,\mathrm{p/cm^2}$	$1.3 \times 10^{11}\,\mathrm{p/cm^2}$
B field		$\leq 1\,\mathrm{kG}$	$5\,\mathrm{kG}$

Ref: "New Small Wheel Radiation and Magnetic Field Environment", Ryan Edgar, etc

- TID: Total Ionizing Dose
- NIEL: Non-Ionizing Energy Loss
- SEE: Single Event Effect

- Safety factors
  - SF**(TID)** = 1.5*5*4=30.0
  - SF**(NIEL)** = 2.0*1*4=8.0
  - SF**(SEE)** = 2.0*1*4=8.0
- RTC @ NSW OUTER RIM
  - *TID: ~48kRad*
  - *SEE: 1.04*10^12 p/cm^2*
  - NIEL: 5.8*10^12 n/cm^2

Radiation safety factors for New Small Wheel electronics.

Safety Factor	Type	Value	Notes
SF_{sim}	TID	1.5	Updated from [1] as per [2]
	NIEL	2.0	Updated from [1] as per [2]
	SEE	2.0	Updated from [1] as per [2]
SF_{ldr}	TID	5.0	COTS, no control for low-dose-rate effects.
	TID	1.5	ASIC, no control for low-dose-rate effects.
	TID	1.0	COTS/ASIC, accelerated aging or low-rate tests.
	NIEL	1.0	
	SEE	1.0	
SF_{lot}	all	4.0	Unknown COTS batches.
	all	2.0	Preselection; homogenous COTS or ASIC batches.
	all	1.0	Qualification; homogenous COTS or ASIC batches.

RTC = SRL * Sfsim * SFldr * SFbatch

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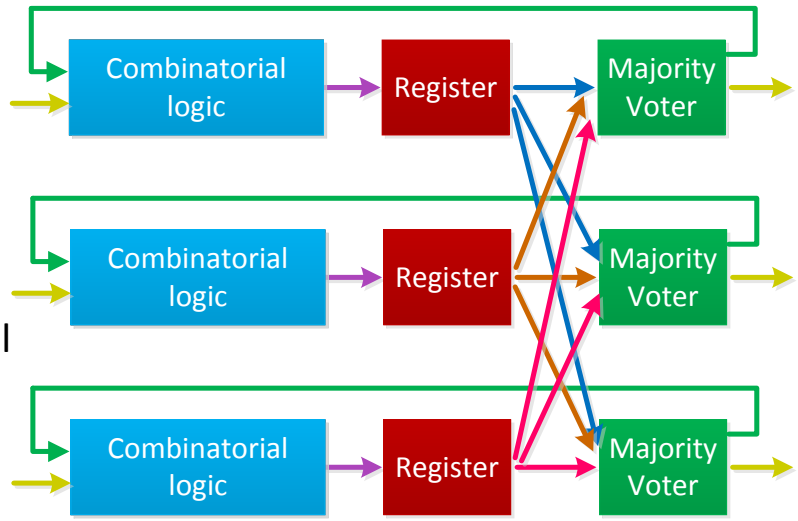
Multi-Layers SEU Mitigation Scheme

❑ Improve FPGA SEU Robustness

Multi-Layers Mitigation	Strategy	Protection
Layer I: Logic Level	TMR	Fabric USER logic
	SEM	Configuration memory
Layer II: Device Level	Flash Scrubbing	multi-boot with 6 copies
	Remote JTAG	Scrubbing FPGA or flash
Layer III: Board Level	Remote Power cycling	Power on/off Router from a "controller" board

❑ Layer I:TMR & SEM

- Triple Modular Redundancy
  - Triplication with 3 voters in fabric design
  - Defeated by MBU
- Soft Error Mitigation Controller
  - Essential bits in CRAM will lead a functional failure
  - Enhanced repair mode: correct single-bit error or double-bit adjacent errors

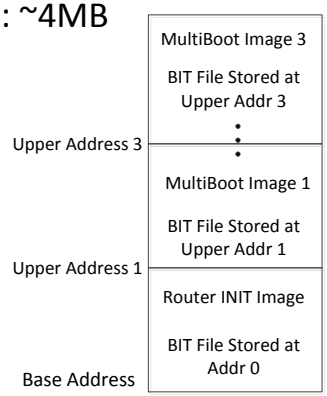


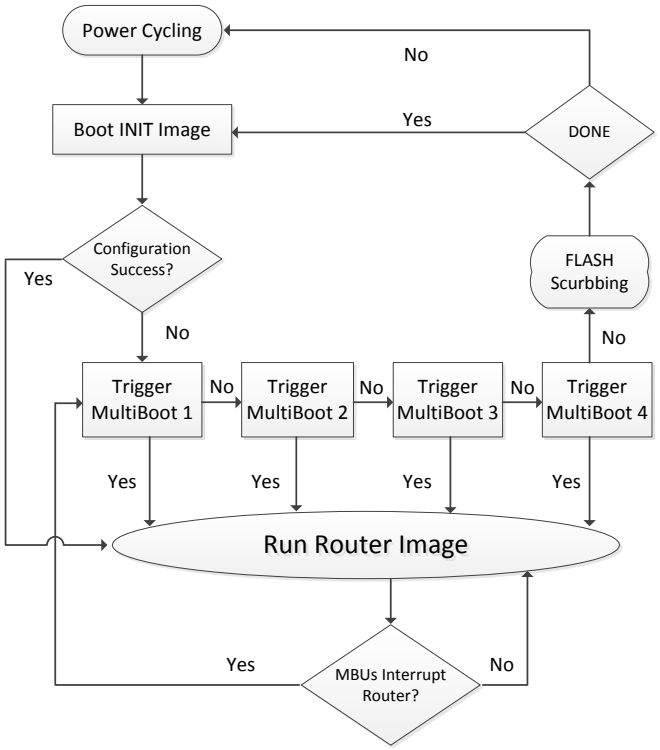
Ref: "Redundancy methods in ASICs", Sandro Bonacini

Multi-Layers SEU Mitigation Scheme

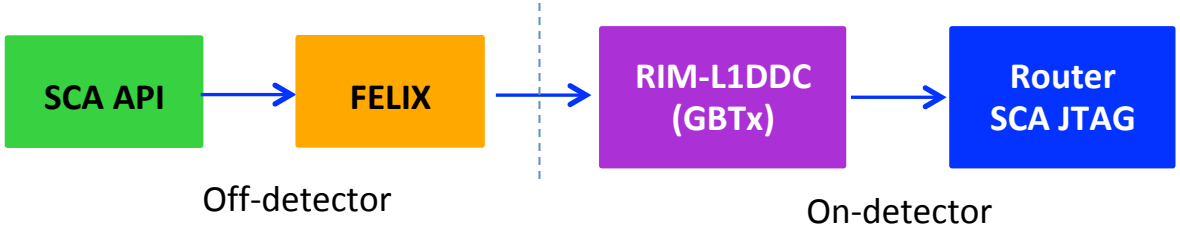
❑ Layer II: Scrubbing @ Device

- Flash Multi-boot Auto Reconfiguration
  - Multiple firmware copies
    - Artix-7 bit stream compress mode: ~4MB
    - 6 copies
  - SPI *4 mode: 4 seconds
- Remote JTAG Reconfiguration
  - Already exist in NSW Trigger Chain
  - CERN GBT link + slow control SCA
  - 9 Seconds: fully scrubbing FPGA
  - Also be able to do FLASH scrubbing





Router Multi-Boot Auto Scrubbing Flow diagram



Remote JTAG Scrubbing @ NSW Trigger Chain

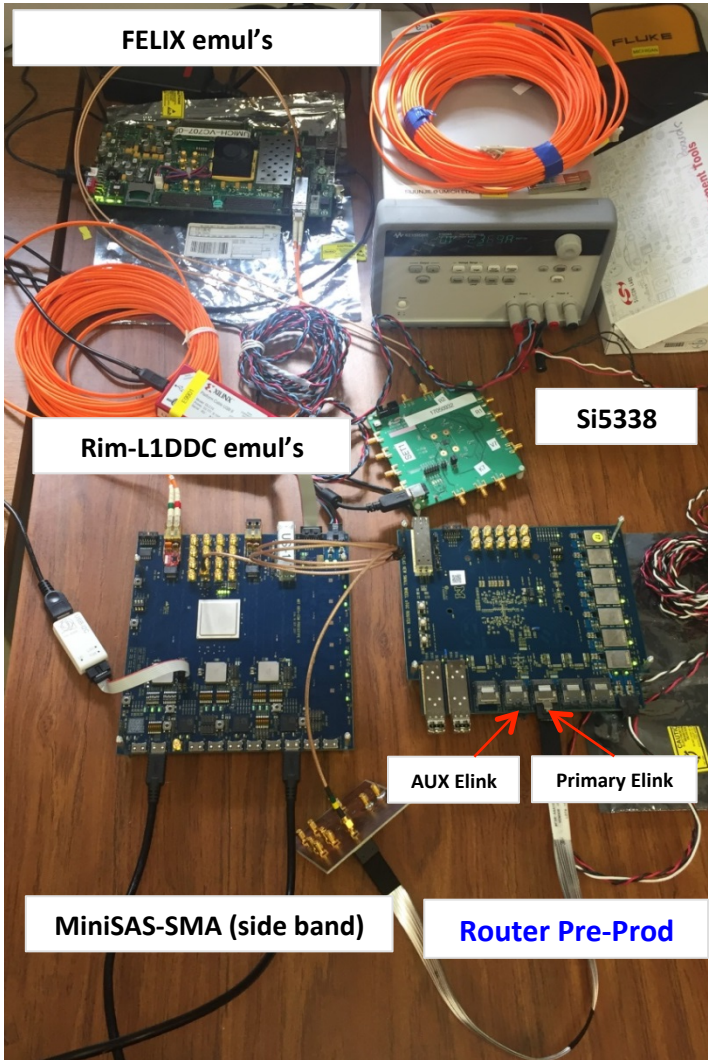
Multi-Layers SEU Mitigation Scheme

❑ Layer III: Remote Power cycling

- Hard Failures (SEFI)
  - PLL / MMCM Fail 1
  - SEM Fatal Error -- Lock FPGA configuration related primitive (ICAPE2…) out 2
  - Xilinx claims

An extremely small number of additional memory bits exist as internal device control registers and state elements. Soft errors occurring in these areas can result in regional or device-wide interference that is referred to as a single-event functional interrupt (SEFI) 3

- Remote Power cycling
  - Control the enable signal of power chip (FEAST)
  - Cooperate with proper power-on sequence of FPGA → Only control the first stage
  - Test platform
    - VC707: simulate partial FELIX fun.
    - GBTx-CSM: simulate Rim-L1DDC
      - VTRx -> GBTx -> GBT-SCA GPIO -> SMA
    - MiniSAS-SMA: sideband A10 connected
      - SMA-> Router Elink Interface B10
    - Router v-pre: DUT



Router Remote power cycling evaluation platform

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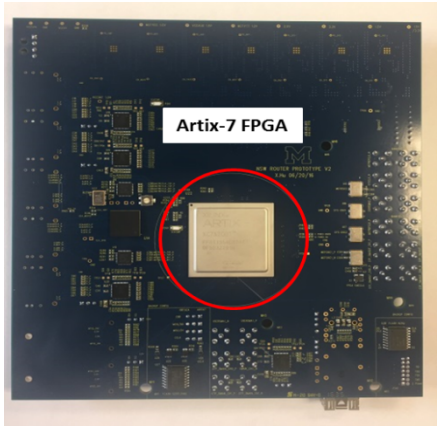
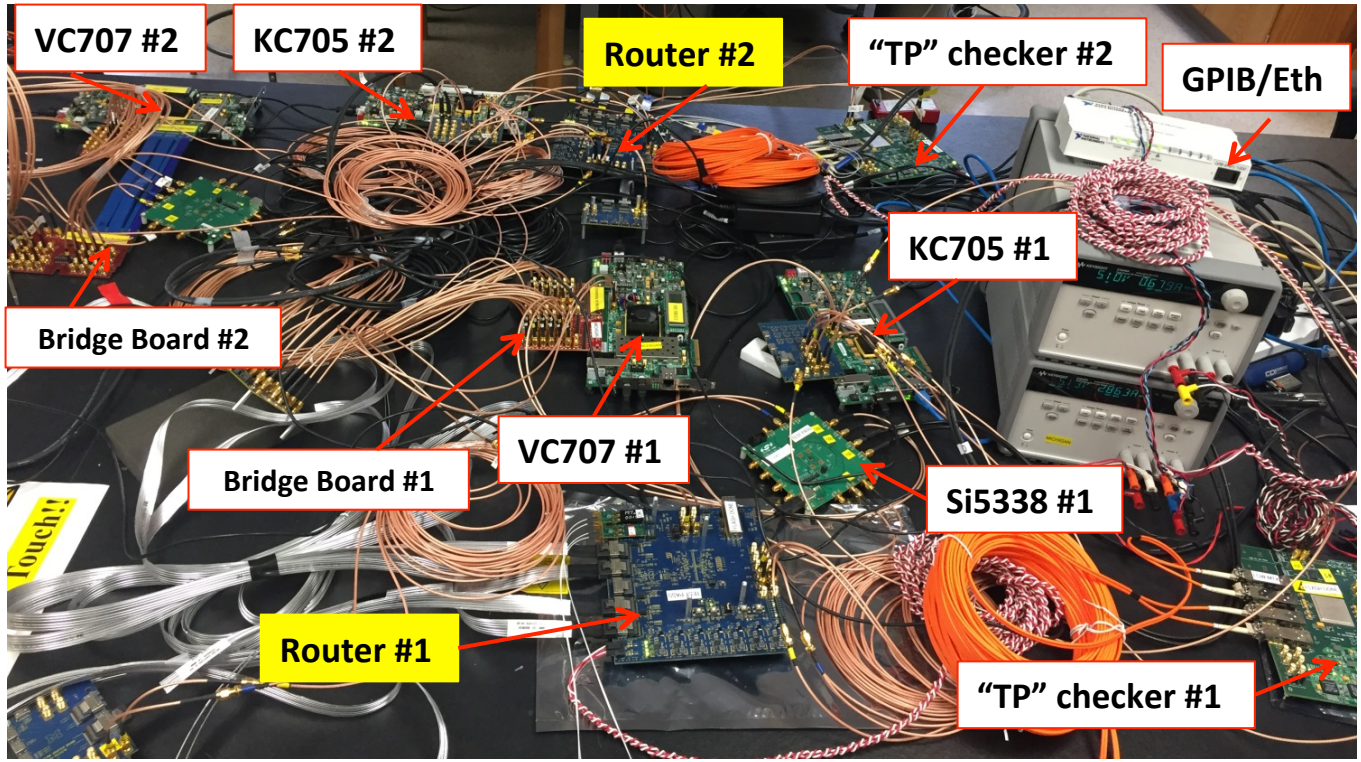
Artix-7 SEU Test System

❑ Hardware System

- Mocking Router running @ NSW
  - VC707: 12 CHs fake “TDS signal Generator”
  - **Router**: Artix-7 DUT FPGA
  - Router v1: 4 CHs fake “Trigger Processor Checker”
  - KC705: Rim-L1DDC emul’s + Ethernet



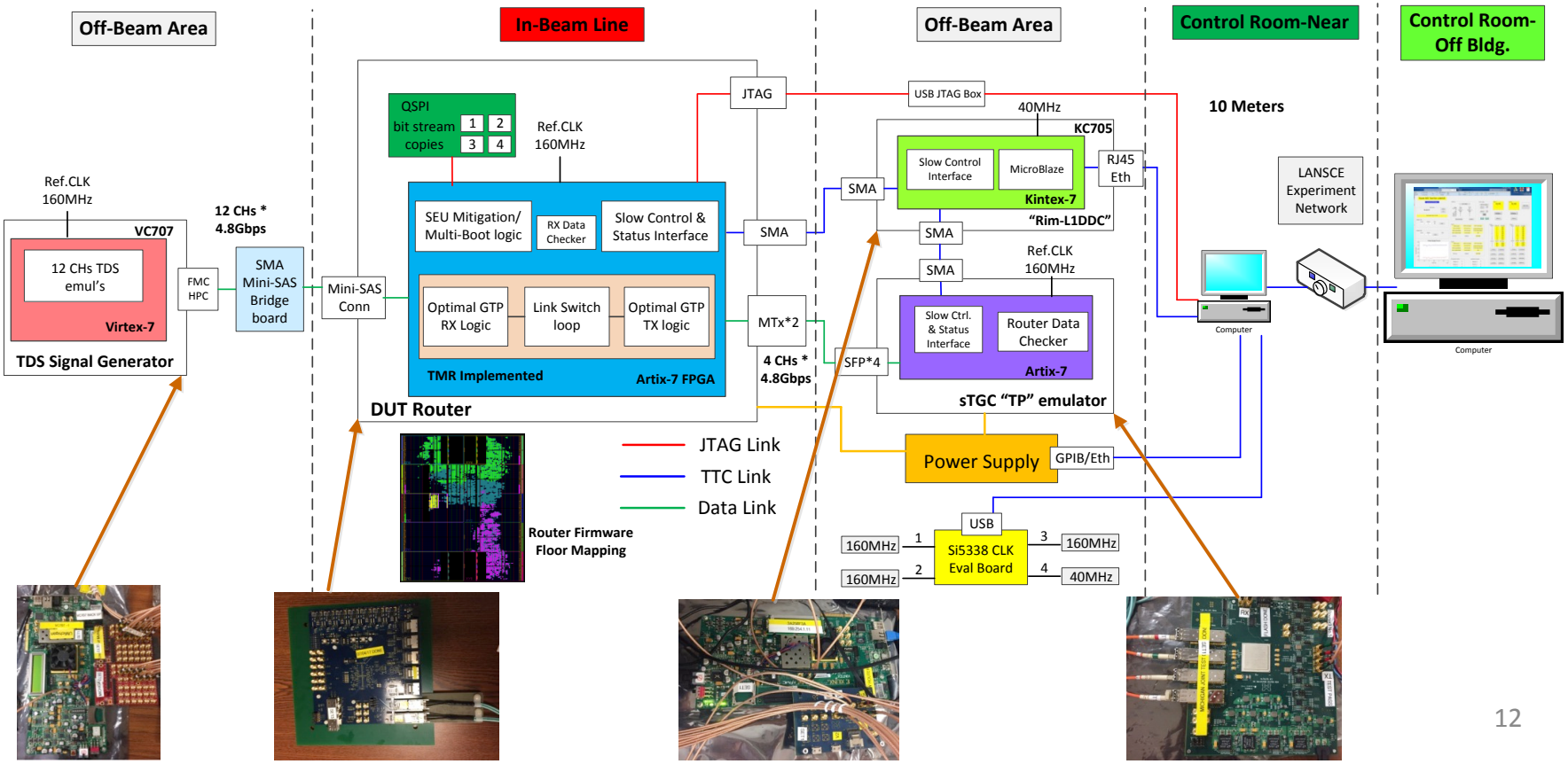
Router Top View



Artix-7 SEU Test System

❑ Firmware @ Artix-7 FPGA

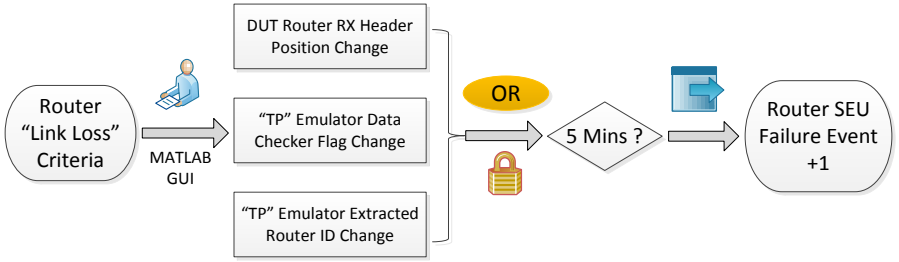
- Router DUT Firmware
  - Deserialization (GTP RX) + Flexible Router (12-to-4) + Serialization (GTP TX)
  - SEM+ Multi-boot trigger
- Auxiliary Firmware

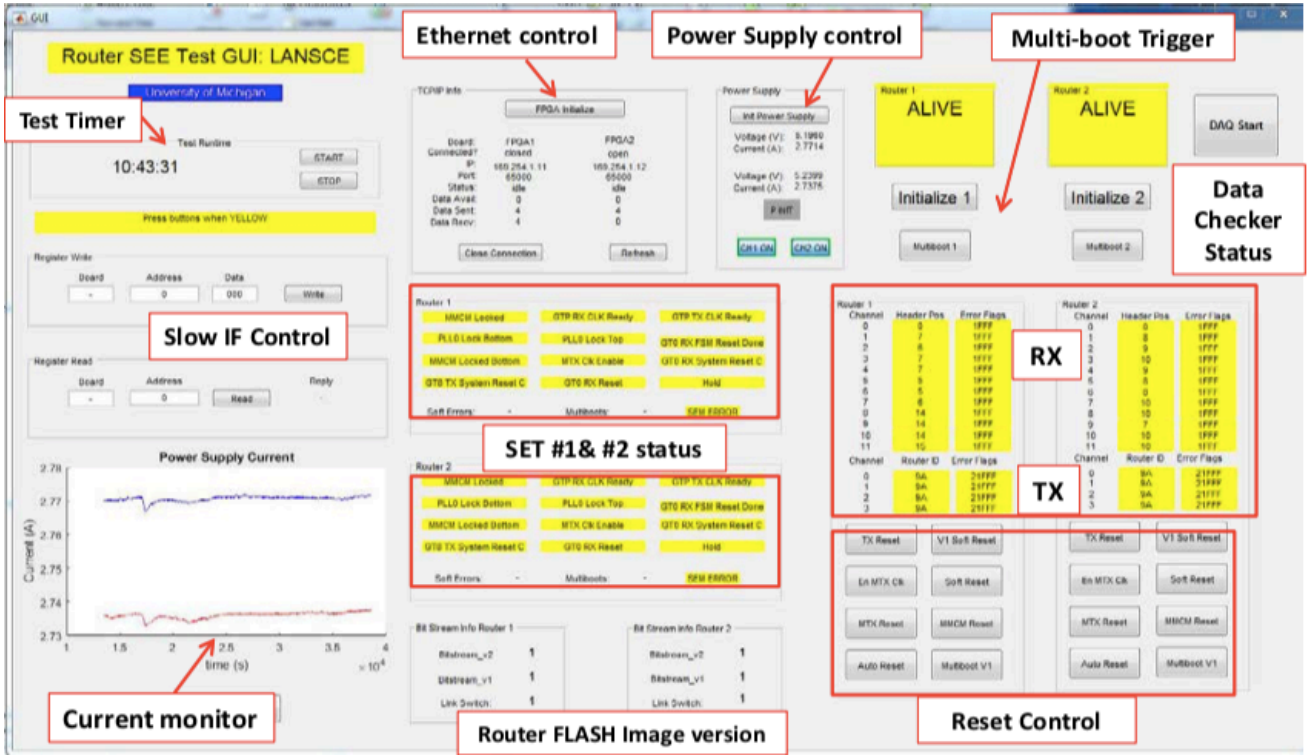


Artix-7 SEU Test System

❑ Software

- MATLAB GUI
  - Control (configuration + multi-boot + power cycling)
  - Set link failure criteria
  - Monitoring “key” status information
  - Automatic recording test results: offline analysis





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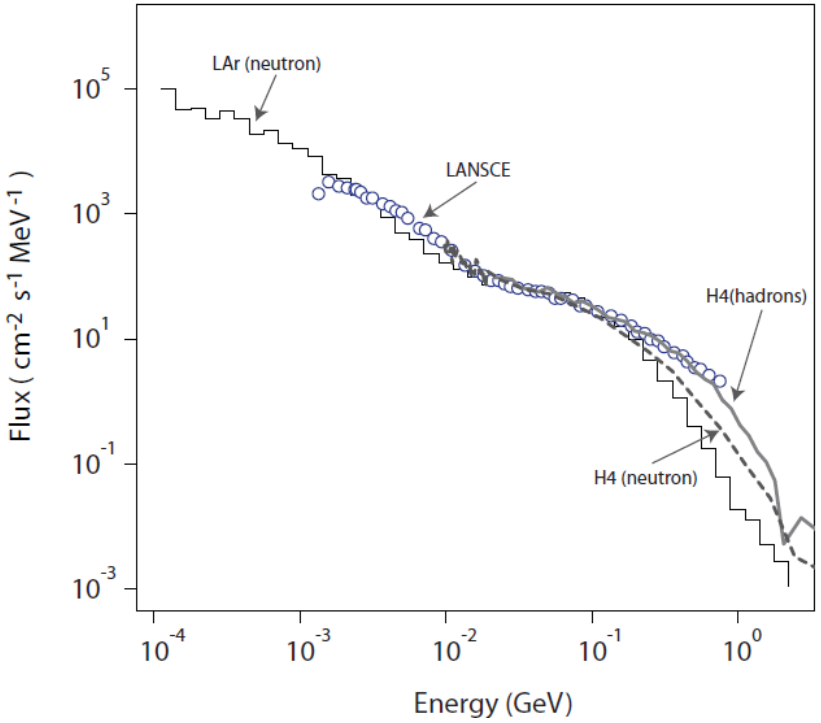
Artix-7 Experimental Test Result

❑ Radiation Tests

- Artix-7 FPGA SEE Test @ 2017
  - Two Facilities: Studying effect of energy on SEEs with same flux
  - 2 setups/Run : Same hardware, firmware, software (cross-check)
- Failure Definition
  - Data cell flips won't cause any failure (just record)
  - Failure: Any router link (12 RX, 4 TX) loss
  - Soft failure: can be fixed by multi-boot, no power cycle needed (< 1min)
  - Hard failure: power cycling operation needed

Artix-7 SEE @2017	Demokritos	LANSCE
Beam Energy (MeV)	20MeV	upto 800MeV
	24MeV	
Beam Size	4π	Collimated 2''
Beam Specturm	Not Clear	Matched well with ATLAS LAr
Flux (n/cm^2/s)	3.41e4, ~4e5	1.39E+06
	1.36E+06	
Total Fluence (n/cm^2)	3.07E+11	5.13e11 * Degraded Factors



LANSCE Beam spectrum matched well with ATLAS LAr

Beam Degraded Factors
Router Set #1: 0.868
Router Set #2: 0.844

Artix-7 Experimental Test Result

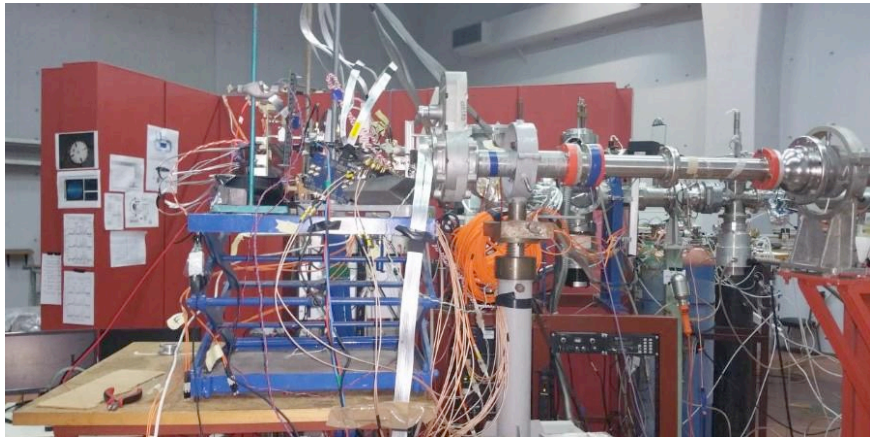
❑ Artix-7 SEE Test @ Demokritos 2017

Day	Energy (MeV)	Flux 1 (n/cm2/s)	Fluence 1 (n/cm2)	Flux 2 (n/cm2/s)	Fluence 2 (n/cm2)	Soft failure	Hard failure	Notes
1	20.1	-	-	1.46e4	1.52e8	0	0	1 Router
2	20.1	3.41e4	1.46e9	1.46e4	6.25e8	0 + 0	0	
3	20.1	3.92e5	1.55e10	5.74e4	2.27e9	3 + 1	0	
4	20.1	4.98e5	1.80e10	5.37e4	1.94e9	4 + 0	0	No TX on #2
5a	24 .0+ parasitic	2.72e7 + 3e8	2.43e11 + 2.5e12	4.04e5	3.61e9	Unstable	0	No TX on #2
5b	**20.1**	**1.36e6**	**2.83e10**	**2.02e4**	**4.21e8**	**9 + 0**	**0**	No TX on #2

Router #1 Total Fluence: 3.07e11 n/cm^2

Router #2 Total Fluence: 9.02e9 n/cm^2

- **Summary**
  - In total, 17 soft failures observed
  - Beam energy 24MeV with 10* parasitic rates makes router links unstable (This Rate is not expected at NSW Rim)
  - 9 soft failures accumulated in 5 hours 30 mins at comparable flux for comparison with Los Alamos Test (~800MeV)

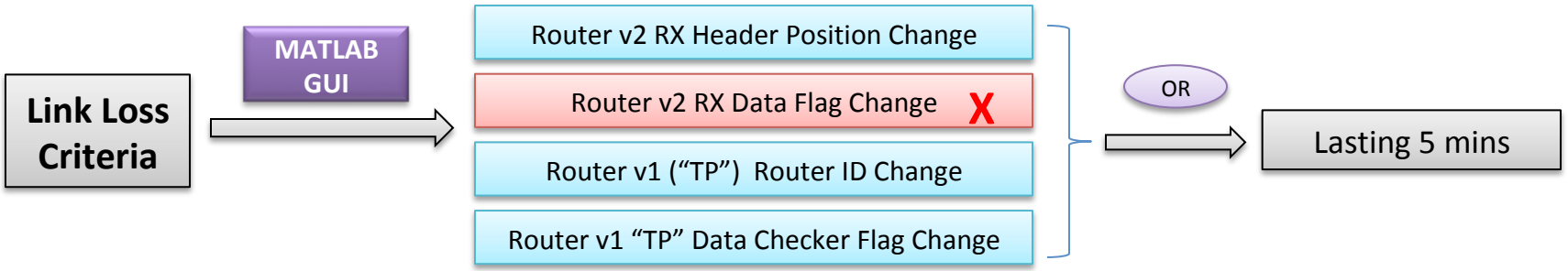


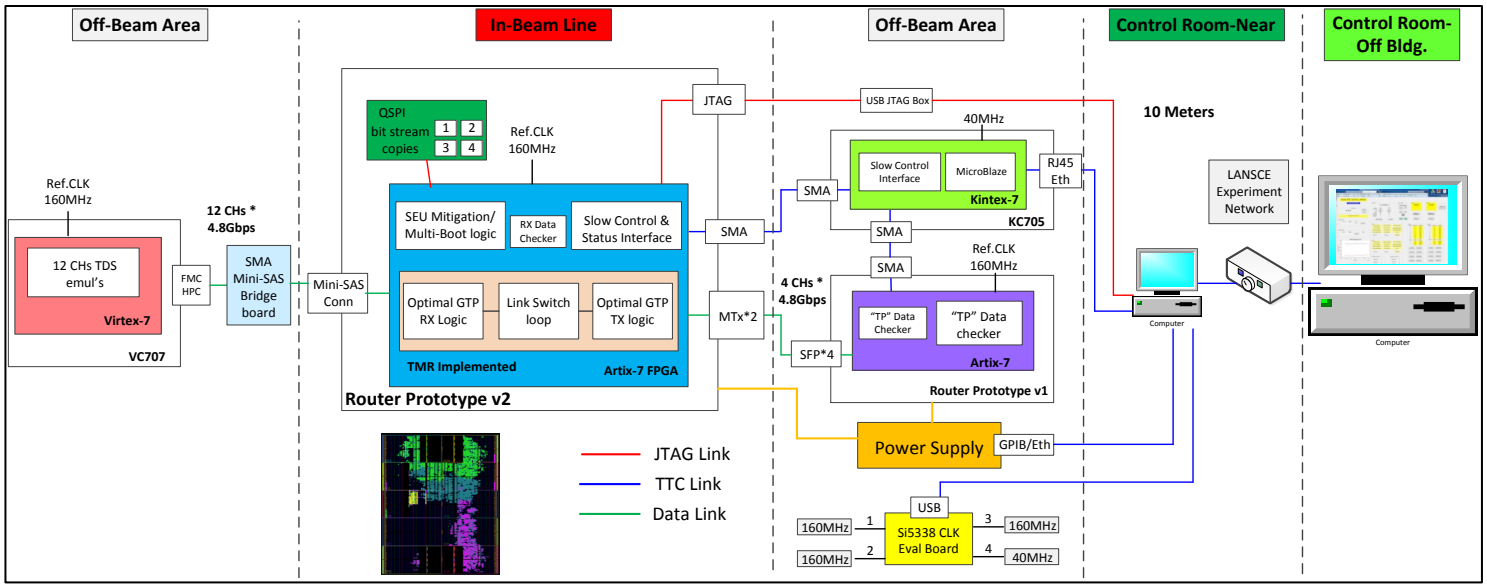
Artix-7 Experimental Test Result

❑ Artix-7 SEE Test @ LANSCE 2017

- Pre-Run (08/29 -08/30 ~12:30pm): LANSCE Beam shut down
- Run I (08/30-08/31 ~9:00 pm): Same system as Demokritos
- Run II (Till beam end @ 09/03 ~6:30am): Update link loss criteria in GUI

Router v2 RX Checking logic is mainly for VS integration test, no TMR and in Beam. And data will be check at "TP" finally

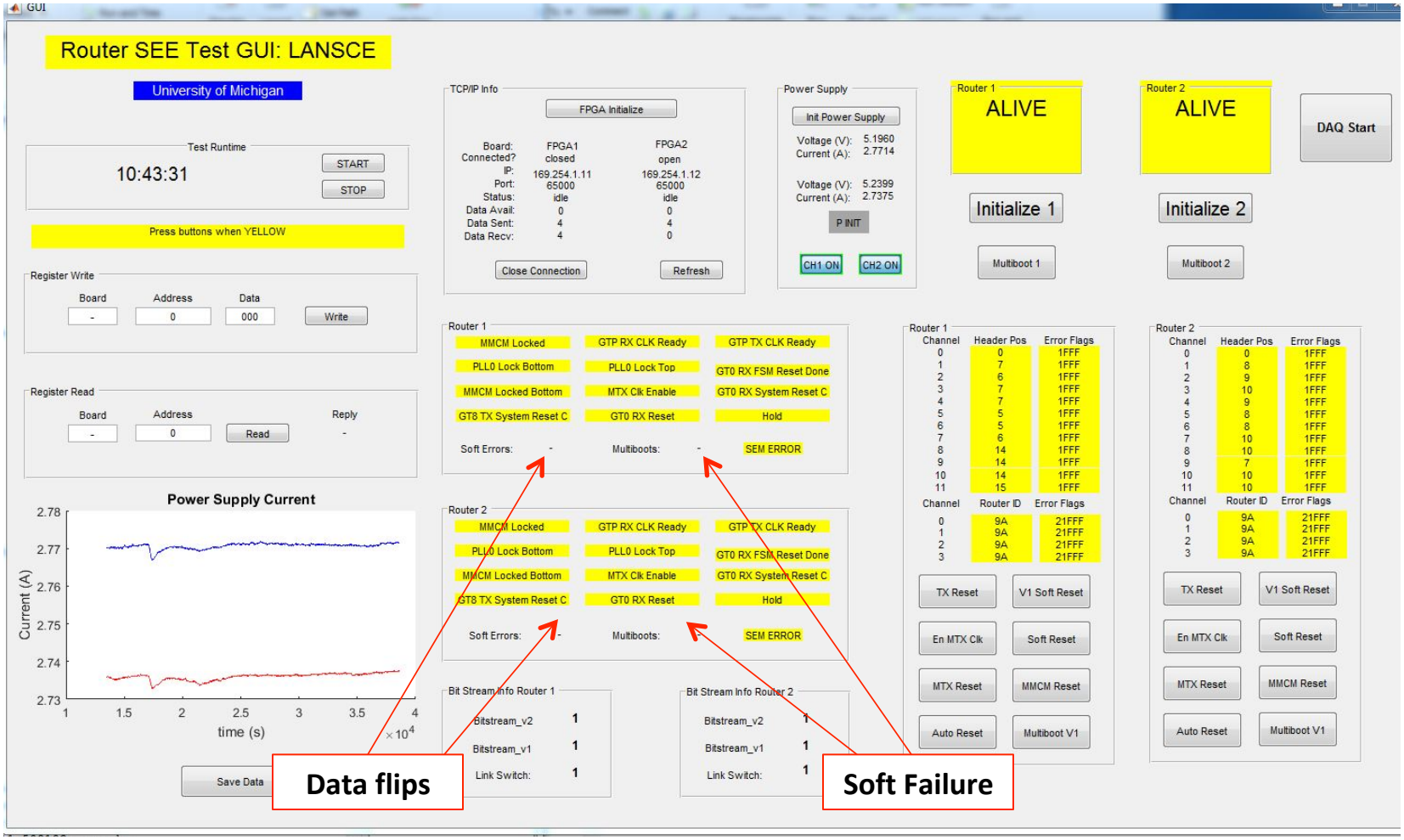




Artix-7 Experimental Test Result

❑ Artix-7 SEE Test @ LANSCE 2017

Pre-Run Result Example: ~11 hours
No data error, no soft failure, no hard failure

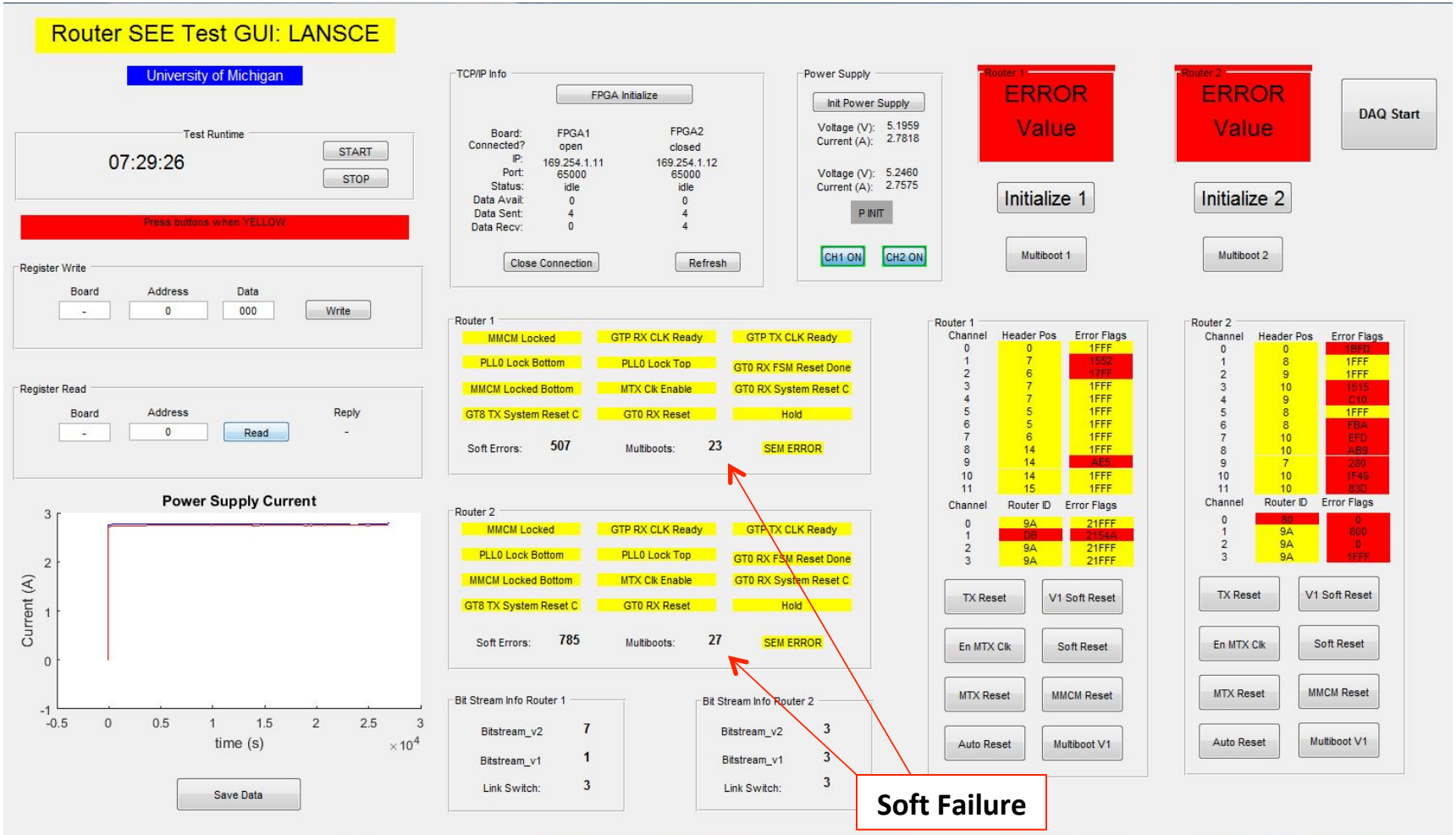


Run at 08/29-08/30 8:30AM No beam at LANSCE

Artix-7 Experimental Test Result

❑ Artix-7 SEE Test @ LANSCE 2017

Run I Result Example: ~7.5 Hours
Set 1: 23 soft failure + 0 hard failure
Set 2: 27 soft failure + 0 hard failure

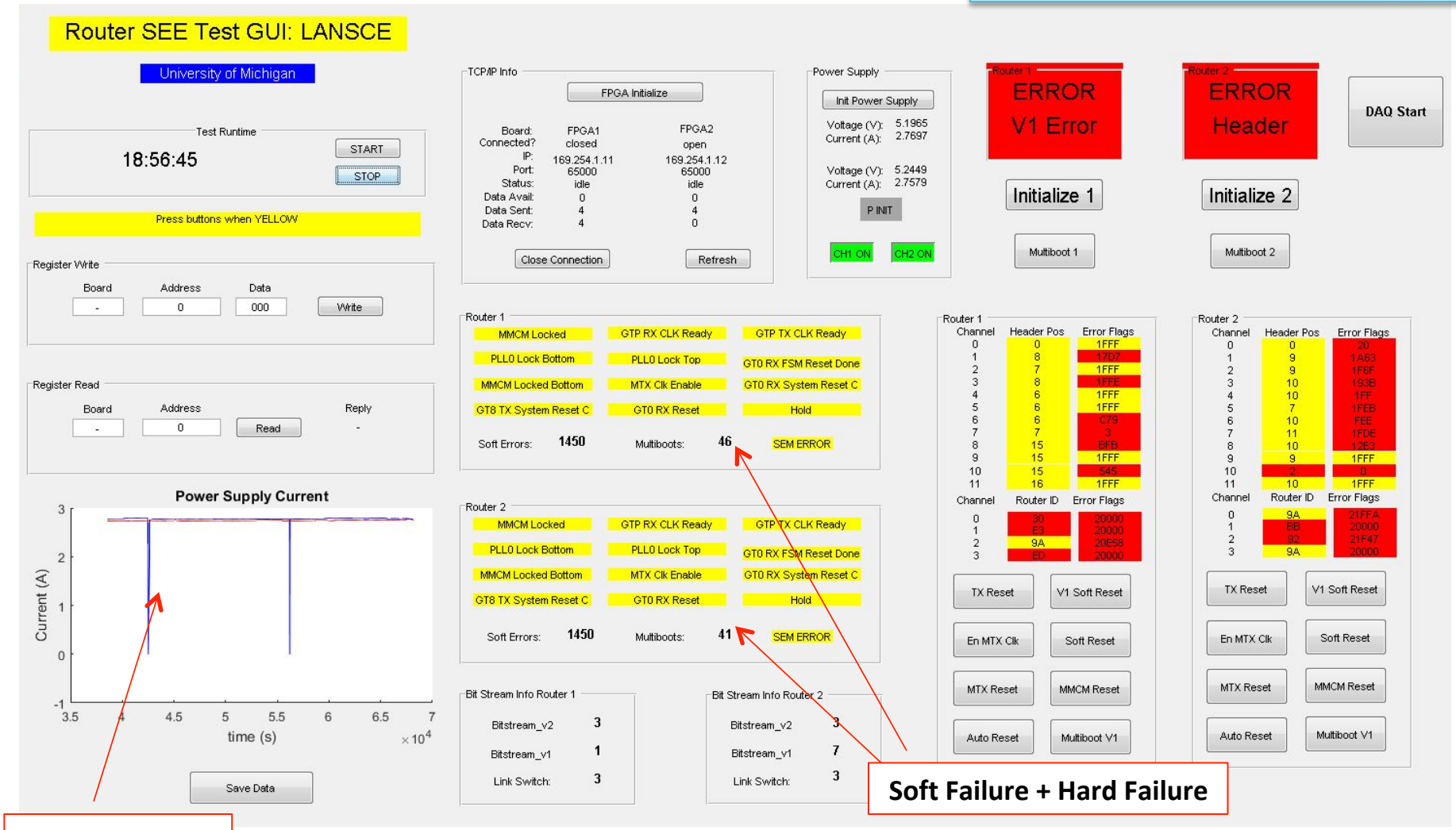


Run I same setup as Demokritos @ 08/31 8:12pm

Artix-7 Experimental Test Result

- **Artix-7 SEE Test @ LANSCE 2017**

Run II Result Example: ~19 hours
Set 1: 43 soft failures + 3 hard failures
Set 2: 40 soft failures + 1 hard failures



Soft Failure + Hard Failure

Hard Failure

Run II from 09/02 11:20am to 09/03 6:00am

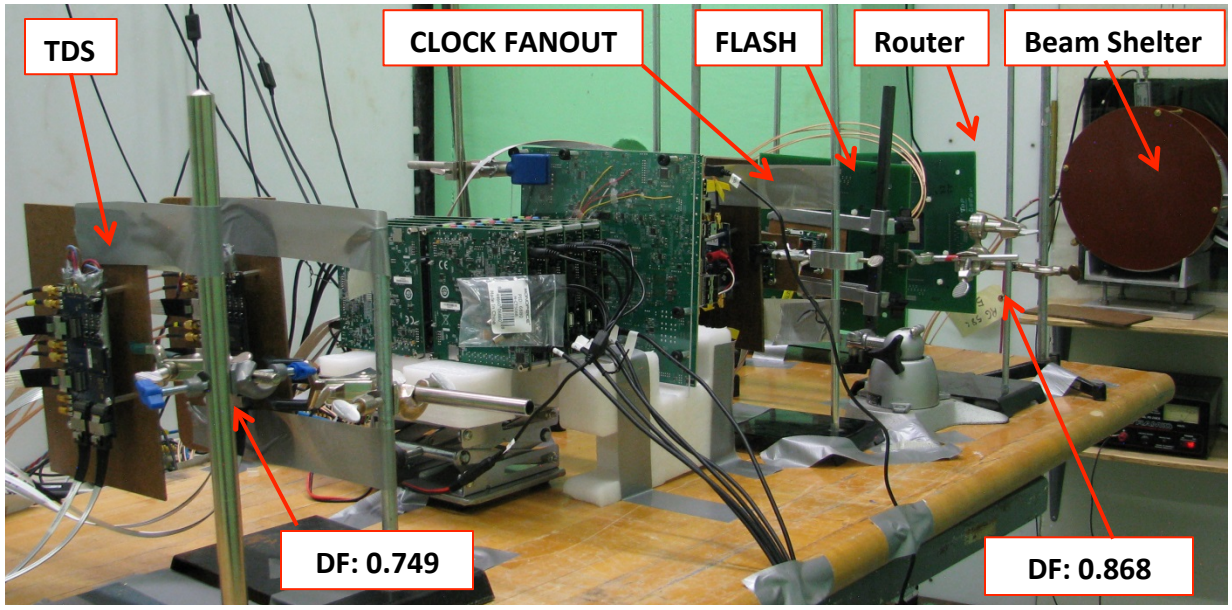
Artix-7 Experimental Test Result

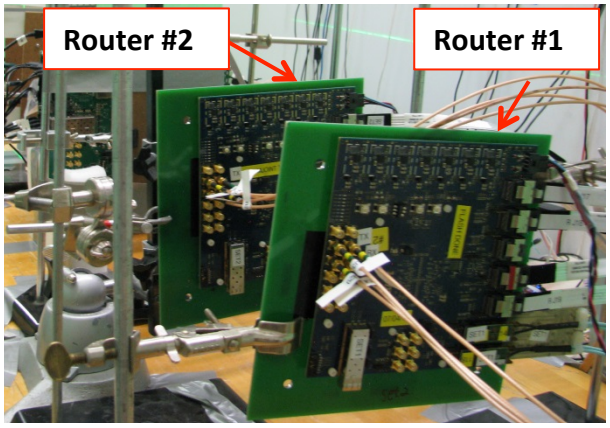
❑ Artix-7 SEE Test @ LANSCE 2017

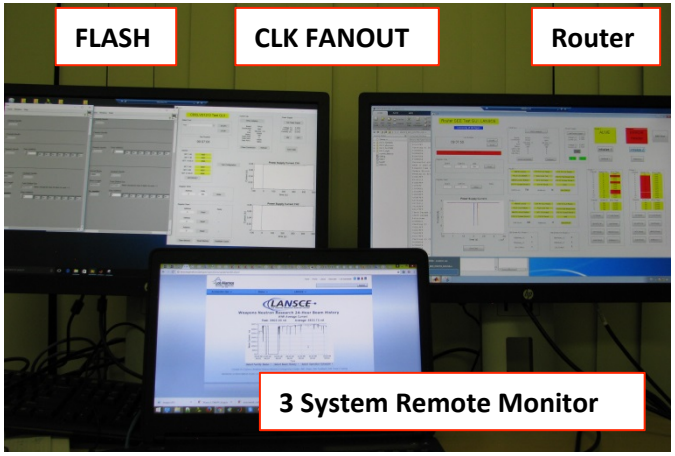
LANSCE @ 2017 RUN	Setup	Accumulated Fluence (n/cm^2)	Soft Failures	Hard Failures	Fully Beam Time	Note
Pre-Run	#1	0	0	0	Beam Down	Matched with Lab stress test
	#2	0	0	0		
RUN I	#1	1.5e11 * 0.868	94	3	~26 hours	Goal: Compare with Demokritos
	#2	1.5e11 * 0.844	88	2		
RUN II	#1	3.63e11 * 0.868	116	7	~63 hours	Goal: Final estimation
	#2	3.63e11 * 0.844	105	6		

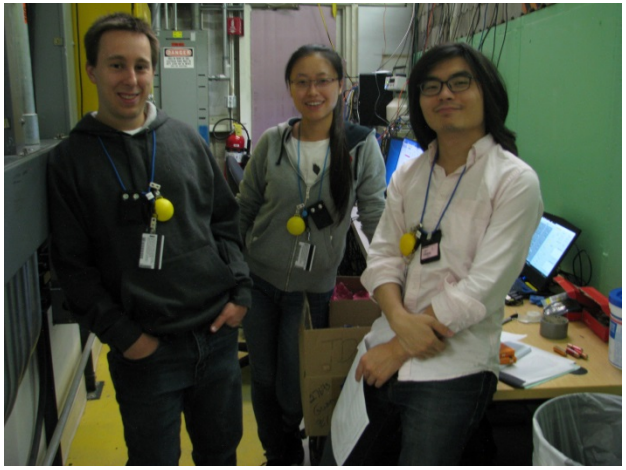
Artix-7 FPGA Test Result Summary @ LANSCE 2017

Artix-7 Experimental Test Result









UM (Tom, Junjie)
& BYU (Mike)
Team Collaboration @
LANSCE

Artix-7 Experimental Test Result

❑ Artix-7 SEE Test @ LANSCE 2017

- **Discussion**
  - Compare Run I result with Demokritos result: **Beam energy matters with ROUTER SEU Rate (Multi-Bit Upsets)**
    - Recoil process naturally related with energy

Soft failures: factors ~2 higher
Hard failures: Yes

Energy transfer to the recoil silicon for incident neutron energy Tn is obtained from classical scattering theory by

$$Tsi = \frac{2MsiMn}{(Msi + Mn)^2}(1 - \cos\theta) \times T_n$$

Max ($\theta=\pi$)
$0.133\times T_n$

Ref: [http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7482701]

- "Fragmentation or Spallation" possibly happened when energy > ~13MeV

Ref: Book "Principles of Radiation Interaction in Matter and Detection" by Claude Leroy, Pier-Giorgio Rancoita

Table 11.7 A few examples of proton, neutron and photon reactions with silicon (from [Leroy and Rancoita (2007)]). The probability of these reactions to occur depends on their energy thresholds.

Reaction	Energy threshold (MeV)	Comment
$n+^{28}Si \rightarrow n+^{28}Si$	0.00	elastic scattering
$n+^{28}Si \rightarrow p+^{28}Al$	4.00	
$n+^{28}Si \rightarrow \alpha+^{25}Mg$	2.75	
$n+^{28}Si \rightarrow \alpha+\alpha+^{21}Ne$	12.99	
$n+^{28}Si \rightarrow p+p+^{27}Mg$	13.90	
$n+^{28}Si \rightarrow p+\alpha+^{24}Na$	15.25	
$n+^{28}Si \rightarrow n+^{12}C+^{16}O$	16.70	
$p+^{28}Si \rightarrow p+^{28}Si$	0.00	elastic scattering

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Summary

- **A Multi-layer SEU Mitigation Scheme**
  - Implemented in Artix-7 FPGA on NSW Router
  - Functionality evaluated at lab
  - Design reliability verified at different Neutron beam facilities
    - System link failure rate within experiment acceptable level
  - Easy portable to other FPGA application
- **More and more FPGA application @ Radiation Environment**
  - CFE experiment in satellites
  - ALICE TPC with Virtex-II FPGA
  - MDT CSM with Virtex-II FPGA
  - NSW Pad Trigger with Kintex-7 FPGA
  - ◦ ◦ ◦

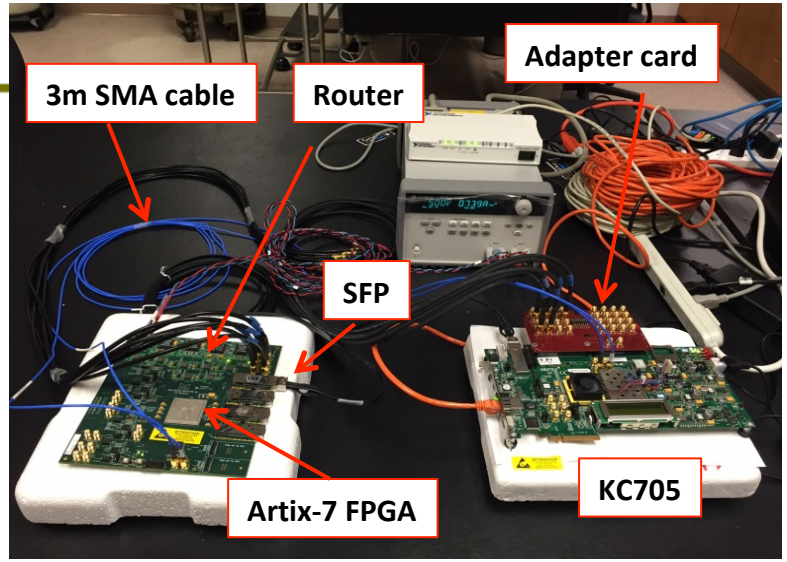
Deeply thanks to:
Michael Wirthlin from Brigham Young University (BYU)
Helio Takai, **James Kierstead** from the Brookhaven National Lab (BNL)
Stephen Wender from Los Alamos Neutron Science Center (LANSCE) for their guide and help!

Backup

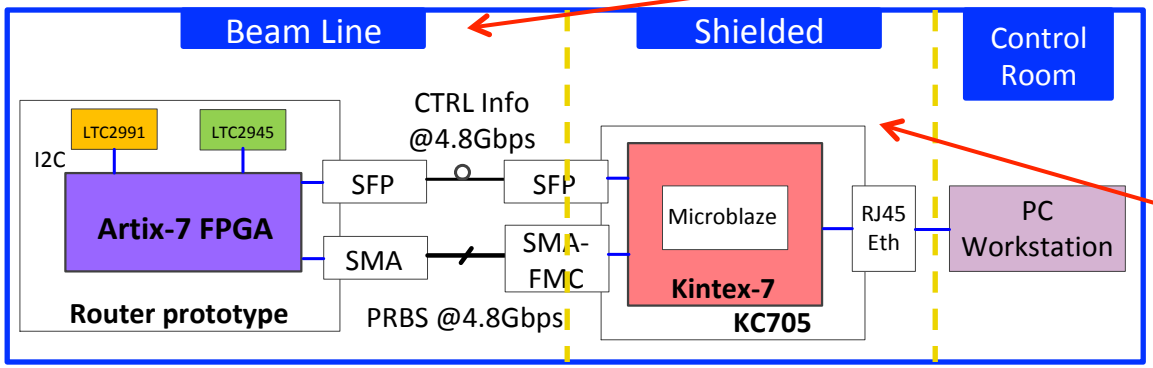
Testing & Validation

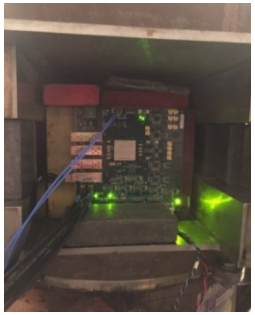
❑ Artix-7 FPGA Radiation Tests

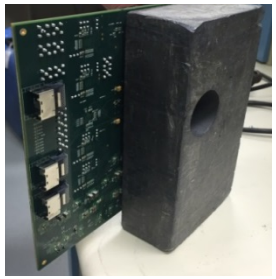
- Artix-7 FPGA TID test
  - Test Two prototypes
  - Test 3 data channels @ 4.8Gbps with PRBS-31, measure BER
  - Monitor current/voltage/die temperature information via SFP (8b/10b)
- Firmware Implementation
  - DUT firmware: PRBS-31 Gen+ GTPs+ 8b/10b coding scheme
  - DAQ firmware: MicroBlaze (MB) soft processor + Ethernet+ + PRBS-31 Checker + GTXs



FPGA TID Test system @ UM
Lab Stress test @ 40 hours NO ERROR



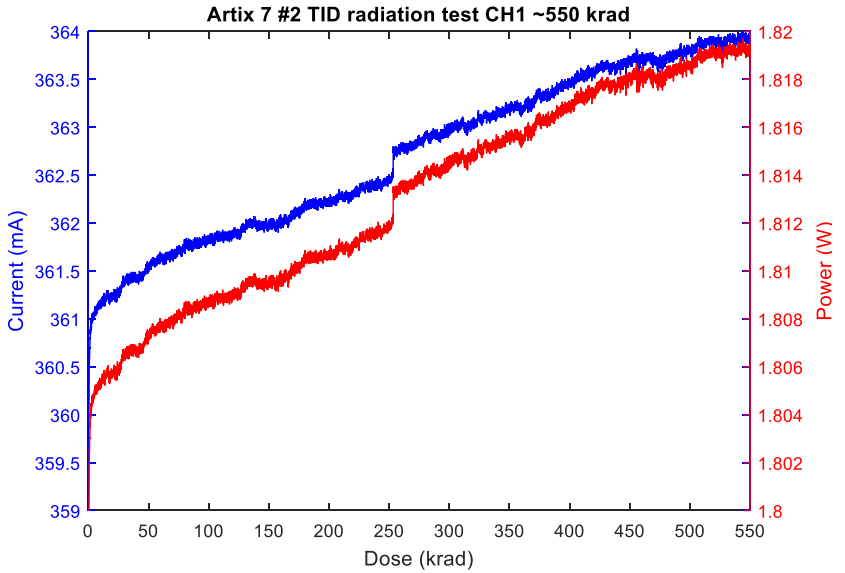


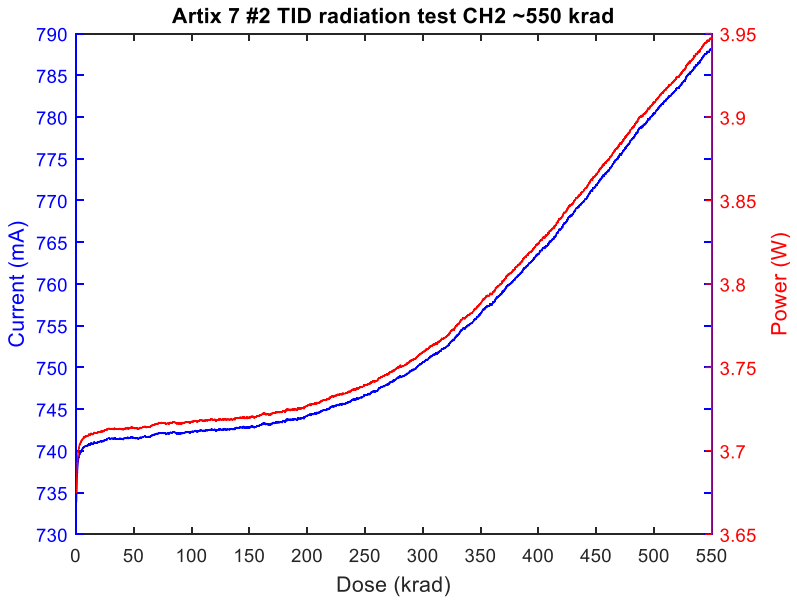


Testing & Validation

❑ Artix-7 FPGA TID Test Results

Current & Power consumption of router #2 5V Input CH 1 (Digital) ~550k*Rad*





Current & Power consumption of router #2 5V Input CH 1 (Analog) ~550k*Rad*

Artix-7 FPGA	#1	#2
Test Time/hour	~30	~55
Test Dose Rate/hour	~10 *kRad(Si)*	~10 *kRad(Si)*
Total Dose/*kRad(Si)*	**~300**	**~550**
Chip states	functional	functional
Current /Power/Temp	normal	normal
4.8Gbps data link	No error	No error

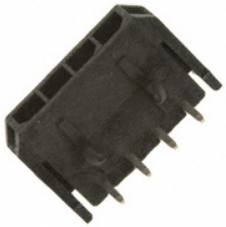
Both Boards test well beyond the 48kRad max at Rim

Design & Implementation

Power Consideration

- Connector: Micro-Fit 3.0 43650
- Input Voltage: 10~12V max
- Power Consumption: 13W (Xilinx XPE tool), 9W max (tested on router prototype v2)
- FEAST: 1 CH. , current max 4A
- Power-on SEQ: Xilinx Requirement
- 7 FEAST/Router

Voltage level	Device	Number of FEAST
1.0V	Artix 7 Vccint, Vccbram	1
1.0V	Artix 7 MGTVcc	1
1.2V	Artix 7 MGTVtt	1
1.5V	GBT-SCA, Artix 7 I/O bank	1
1.8V	Artix 7 Vccaux	1
2.5V	Repeater, OSC, MTx	1
3.3V	MTx	1



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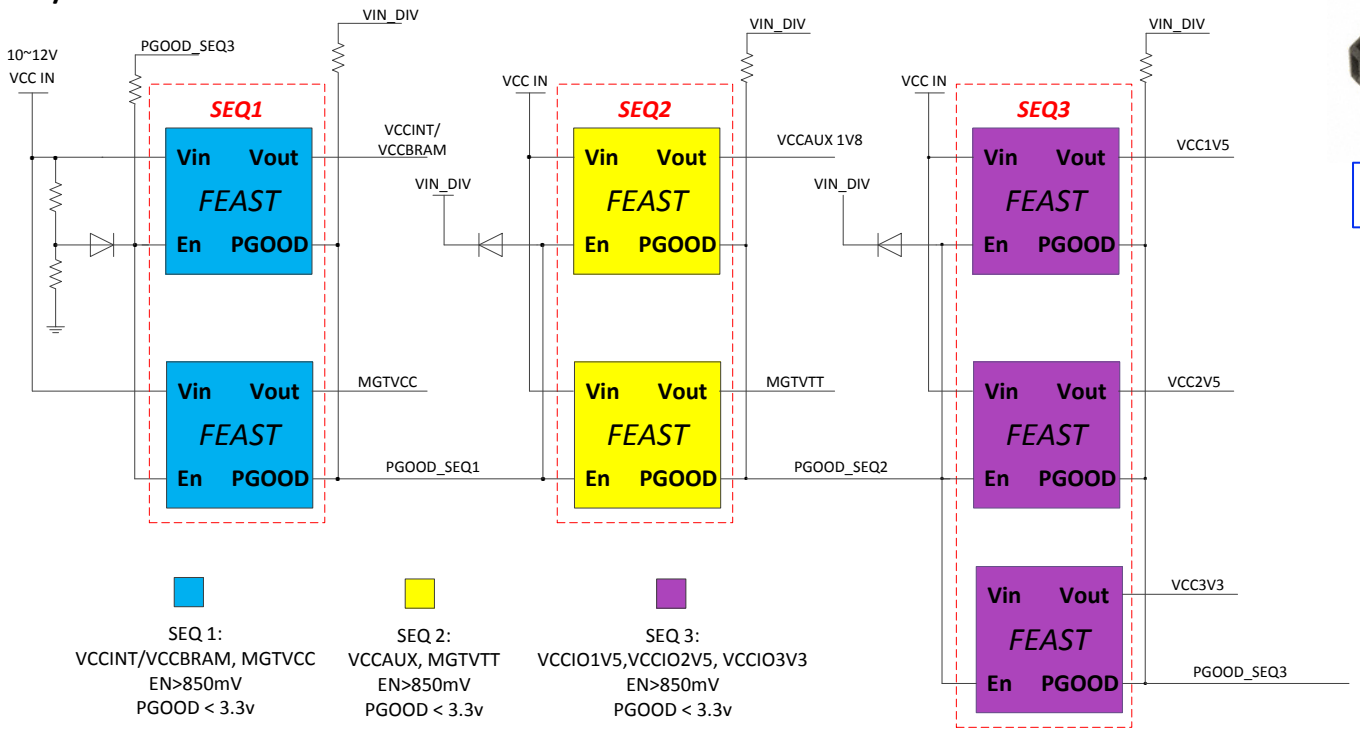
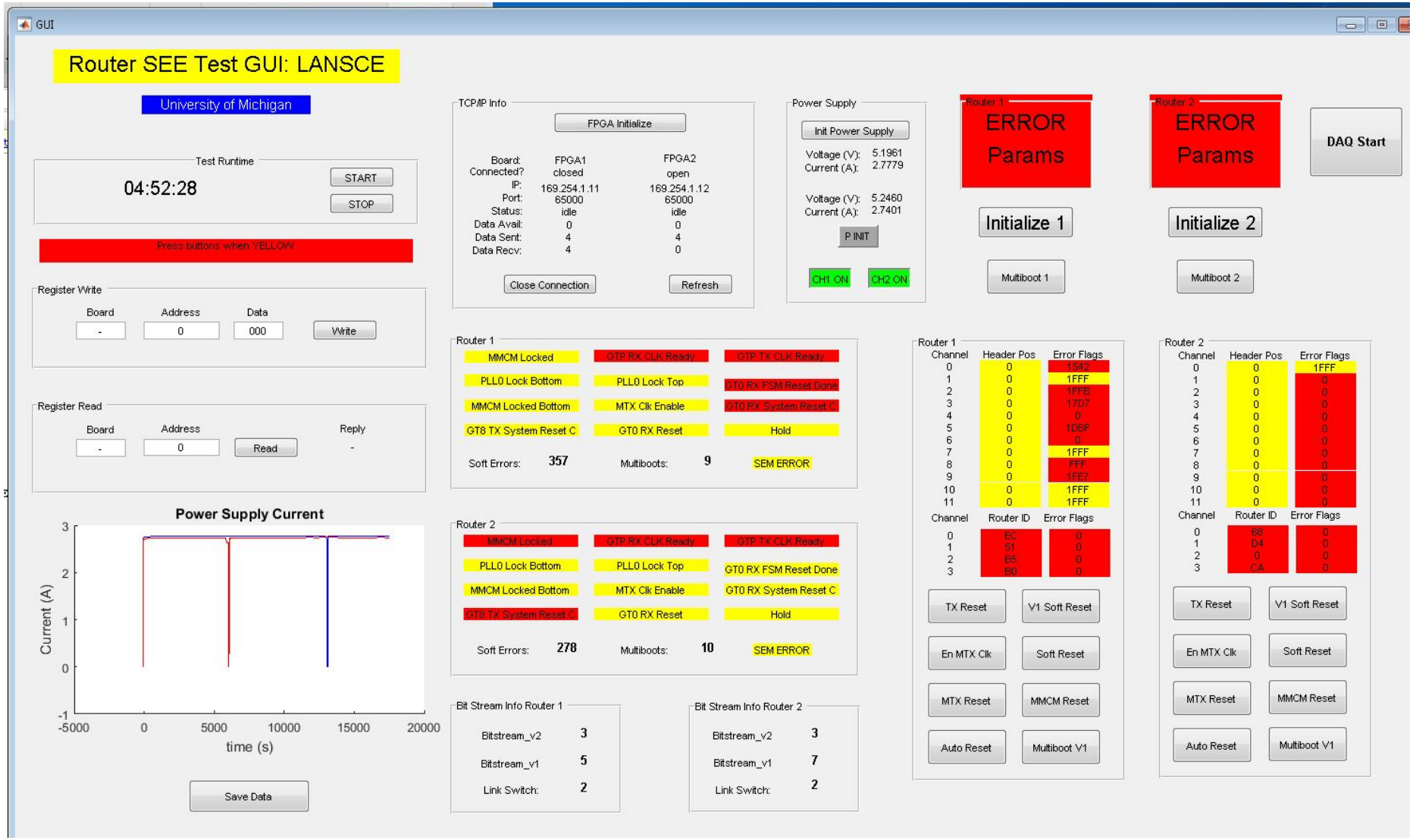


Testing & Validation

- **PLL/MMCM Fail Case**



Testing & Validation

❑ SEM Controller Fail Case