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Investigation of Proton Induced Radiation Effects in 0.15 µm Antifuse FPGA

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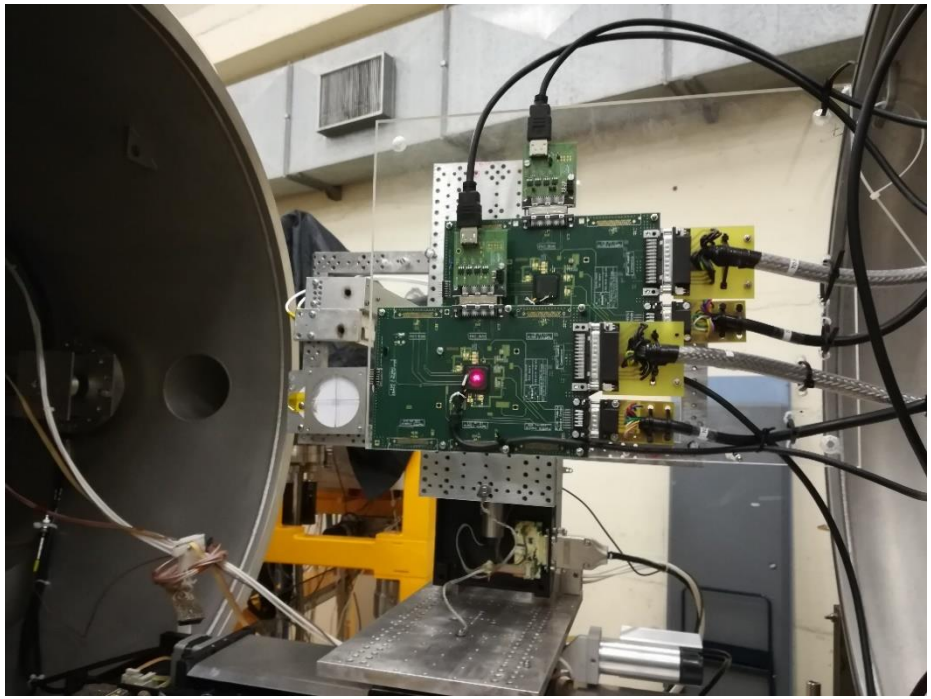
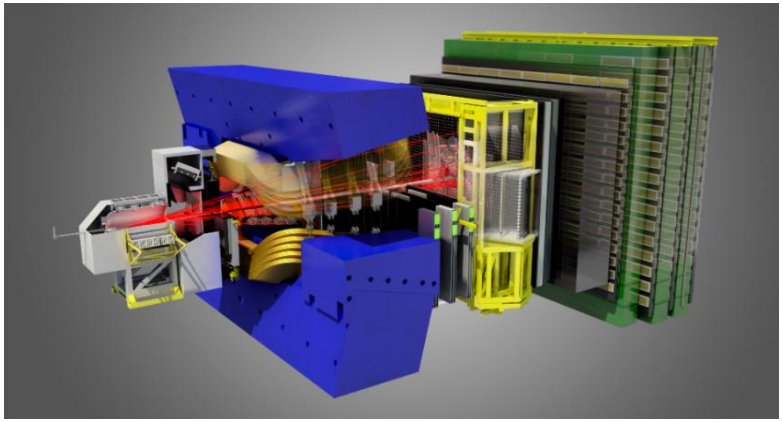
Outline

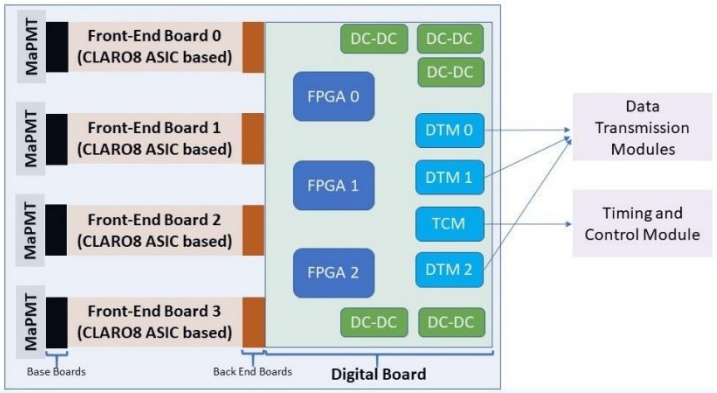
- Introduction
- Radiation environment
- Device Under Test
- Setup
- Irradiation Results
- Summary & Conclusions



Introduction-LHCb Upgrade



LHCb detector
https://lhcb-public.web.cern.ch/lhcb-public/

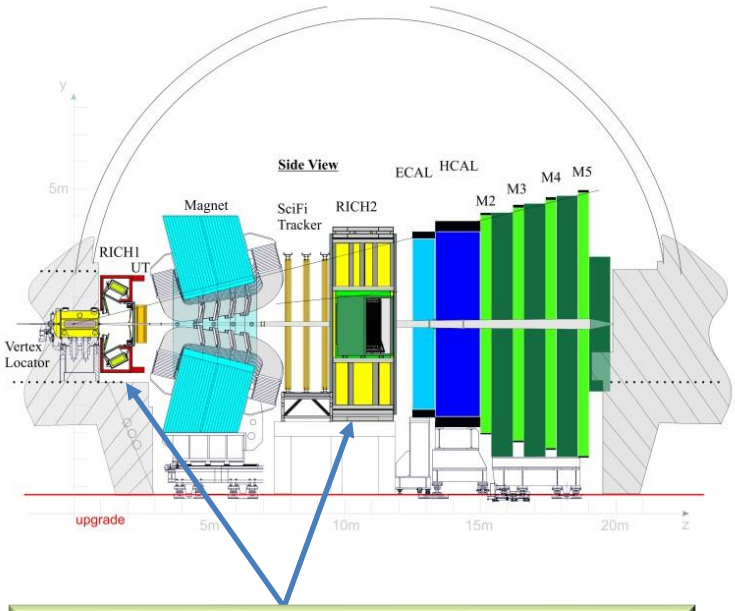


Elementary Cell (simplified architecture)
512 readout channels

- During the second LHC long shutdown (2019-2020) the entire LHCb detector will be upgraded to operate at higher luminosity;
- The LHCb RICH sub-detectors will be upgraded with a 40 times increased readout rate;
- For the Digital Boards an SRAM based FPGA from Kintex-7 family has been proposed as a main solution;
- An antifuse FPGA from Microsemi's Axcelerator family has been proposed as a back-up solution;
- Device under test: **AX250-FG484**.

The LHCb Collaboration, *LHCb Particle Identification Upgrade Technical Design Report*, available at: link.

Radiation Environment



RICH 1 and RICH 2 sub-detectors

- FLUKA simulation --> Total Ionizing Dose (TID) and neutron equivalent for 50 fb^{-1};
- Worse case scenario values are expected in RICH 1 sub-detector, because of its position with respect to primary collision point;
- FPGA exposed to a maximum of 200 krad (2 kGy) over the Upgrade Phase I.

Framework TDR for the LHCb Upgrade: Technical Design Report

Region	TID [krad]	Hadrons: >20 MeV [cm^{-2}]	Neutrons: 1 MeV n_{eq} [cm^{-2}]	Dose rate [rad/s]
RICH 1	200	1.2×10^{12}	3×10^{12}	0.008**

** => assuming 7000 h of LHC operation over the entire Phase I.

LHCb Upgraded RICH 1 Engineering Design Review Report

Device Under Test

- **AX250-FG484:**
  - not a flip-chip device;
  - manufactured in 0.15 µm CMOS antifuse process technology;
  - 1408 R-Cells => dedicated Flip-Flops;
  - 2816 C-Cells => combinational cells;
  - 55.296 kb of embedded SRAM;
  - 248 user I/O pins organized in 8 I/O banks;
  - 4 hardwired clocks and 4 routed clocks;

Axcelerator Family Datasheet

- **Antifuse process:**
  - non-volatile => immune to configuration SEUs;
  - one time programmable;

- **Immune to SEL:**
  - no SEL up to LET = 120 MeV cm^2/mg;
  - J. J. Wang et al, “Single Event Effects of a 0.15 µm Antifuse FPGA” (2002).

Setup

AX250 Test Board Features:

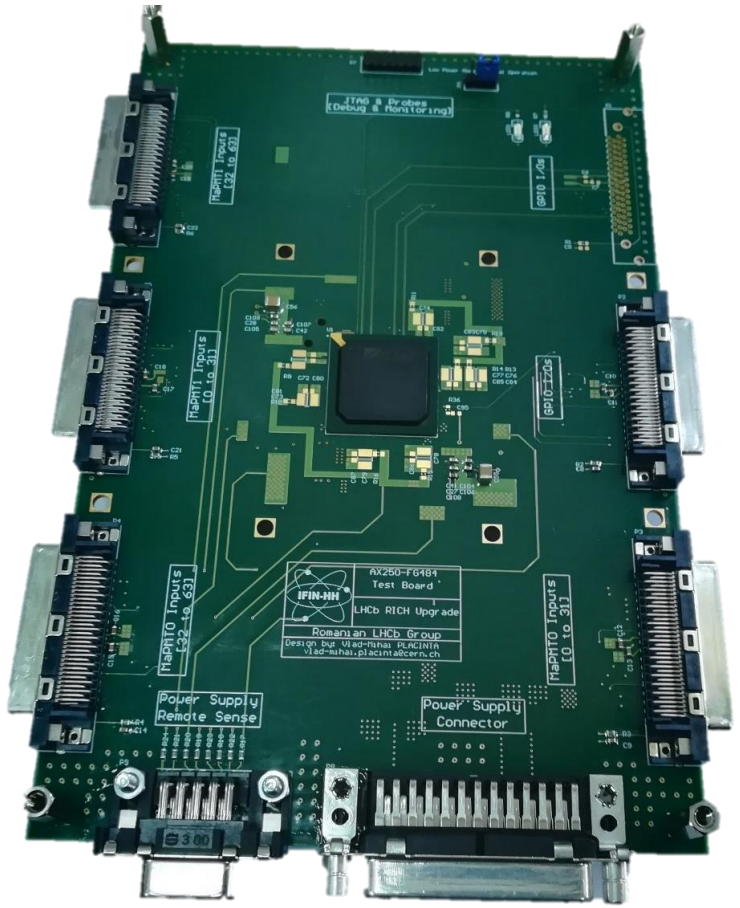
- **Designed on 8 layers with 180 x 120 mm;**
  - **Mostly because of the VHDCI connectors;**

- **128 I/O pins corresponding to 2 MaPMTs are used for testing the I/O blocks with simulated trigger signals;**
  - **The signals are hardware generated by pulling up or down each I/O pin using a passive switch;**

- **2 types of clock network resources are routed out and only one was tested;**
  - **HCLK=> hardwired clocks;**

- **Data is shifted in/out serialized;**

- **Optionally, the JTAG TAP controller and the device's checksum number can be monitored.**



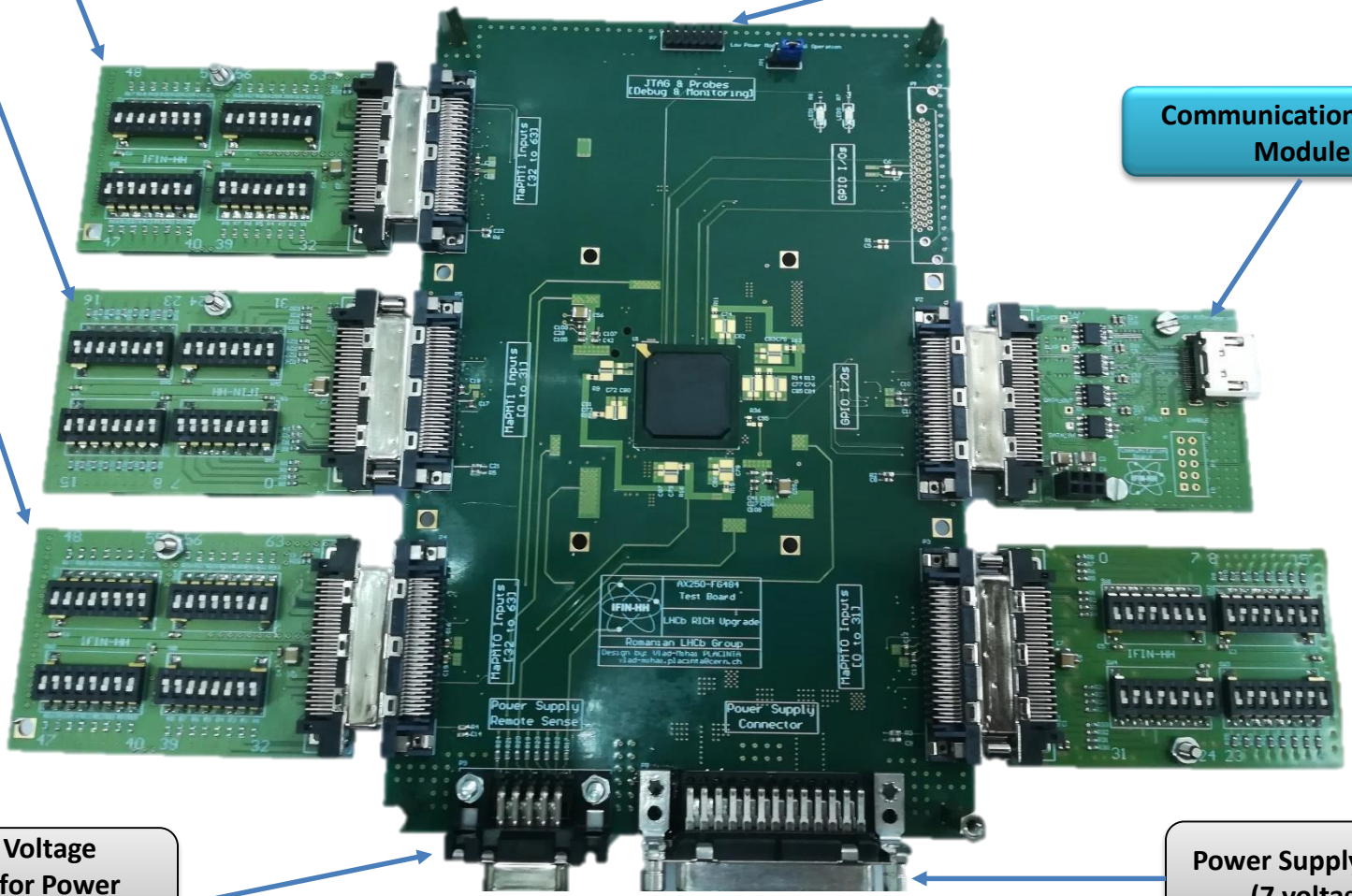
AX250-FG484 Test Board

Setup

Plugins: to simulate MaPMT triggers (passive)

JTAG & Checksum Monitor

Communication Plugin Module



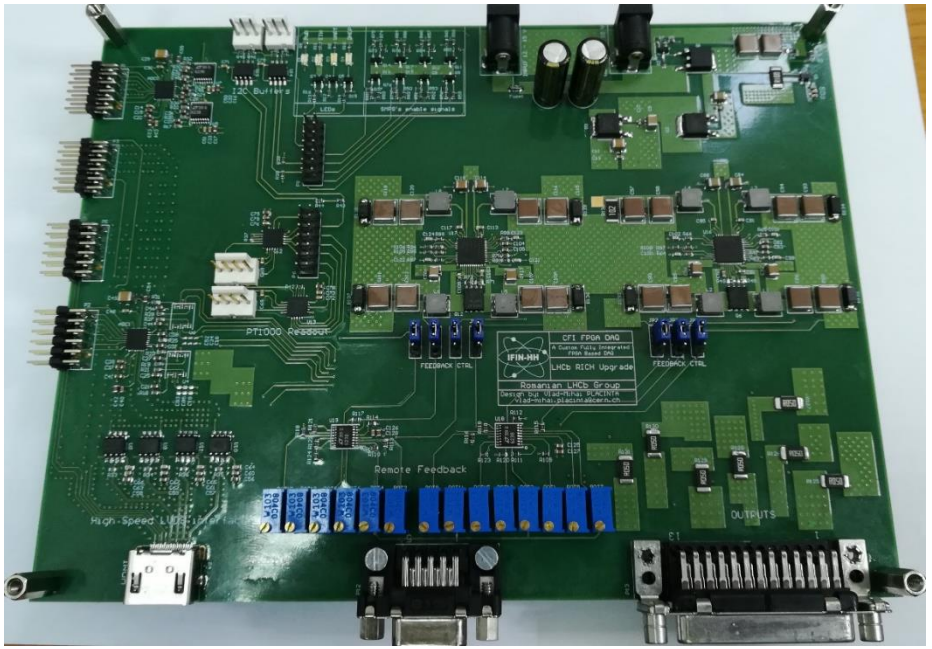
Remote Voltage Feedback for Power Supplies

Power Supply Connector (7 voltage rails)

AX250-FG484 Test Board and its modules

Setup

- A custom DAQ system, FPGA based, has been designed to power, control and monitor the FPGA and its firmware activity over 5 meters of screened cables;
- 7 voltage rails were used to power up the FPGA;
  - Remote feedback was added on the each voltage rail;
- Two PT1000 sensors were used for DUT's dice and environmental temperature monitoring;
- The DAQ system can be connected either via UART or TCP/IP Ethernet to a PC where a LabVIEW GUI controls and reads the DAQ;
  - Data is saved in ASCII files (40 Hz rate).



DAQ System

62.5 µV and 62.5 µA sensitivity for each power rail

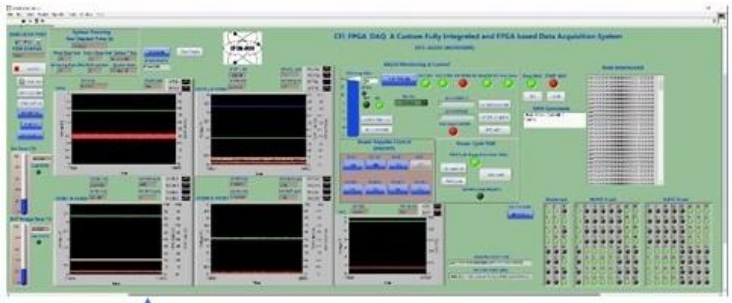
Setup

- The AX250 user logic has been running at 40 MHz, provided from the DAQ;
  - Hardwired clock was used;
- Hardware Flip-Flips (R-Cells) configured as a TMR architecture;
  - Optionally, a minority voter has been embedded to monitor and to detect single lane changes;
- "LHCb RICH like" firmware:
  - 128 inputs were read, packed and sent to the DAQ;
- Embedded SRAM readout firmware;
  - 38.76 kb of SRAM were read, packed and sent to the DAQ.

Firmware	R-Cells	C-Cells	Embed. RAM	Clocks	IOs
TMR	846 (60 %)	2	0	HCLK (40 MHz)	5
LHCb RICH-like	326 (23 %)	124 (4 %)	0	HCLK (40 MHz)	135
SRAM	418 (30 %)	846 (30%)	38.76 kb (70 %)	HCLK (40 MHz)	7

Setup

For SIRAD facility from Legnaro National Laboratories (Italy)



CONTROL ROOM

IRRADIATION AREA (inside the vacuum chamber)

TCP/IP

USER DAQ SYSTEM

EXPERIMENTAL AREA (outside the vacuum chamber)

PT 1000 readout (screened cable)

Power rails (screened cable)

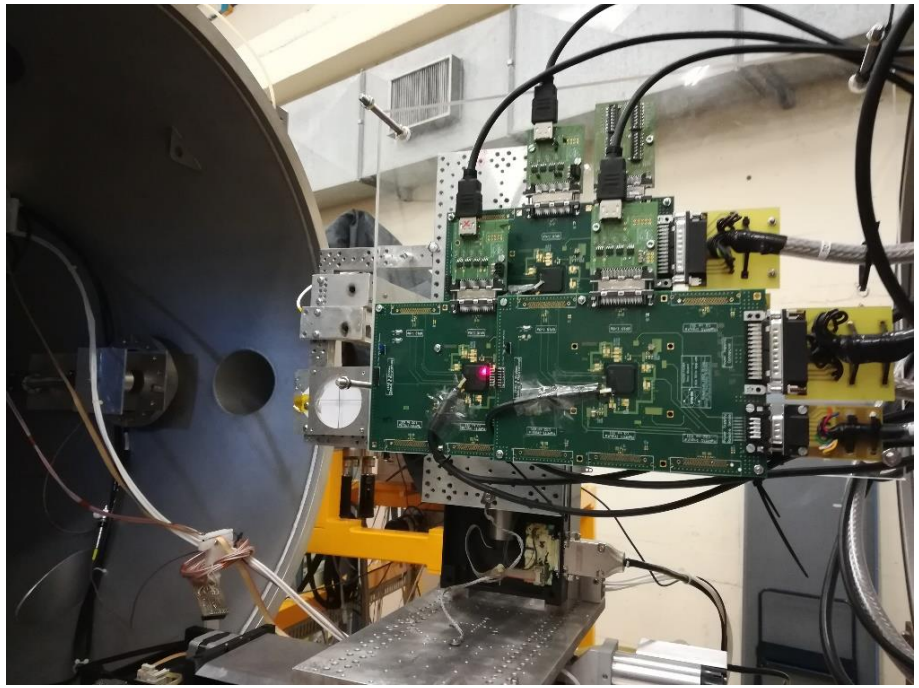
Remote Feedback for each voltage rail (screened cable)

Communication & Controls (HDMI cable)

5 m long

Irradiation Results

- We used 24 MeV protons from the SIRAD facility at INFN - Legnaro, Italy; (May, 2018)
- Average fluence per FPGA's active layers: 10^{13} to 2.5 x 10^{13} protons/cm^2;
- Flux values between 0.5 x 10^8 and 5 x 10^9 protons/cm^2/s:
- TID delivered:
  - 3.2 Mrad (Si) for 3 samples;
  - 8 Mrad (Si) for one sample;
  - 1.6 Mrad (Si) for one sample.
- 5 samples were irradiated in 2 days;
  - 2 samples during 1st day;
  - 3 samples during 2nd day;
  - Annealing for 6 days + 1;
- Proton runs dose rate:
  - between 130 rads/s and 360 rads/s;
  - one run with 1 krad/s for one sample.



Irradiation Results

- No SEUs or SETs have been seen in the TMR logic;
  - 3 samples were tested for a fluence of 10^{13} particles/cm^2;
  - the TMR architecture had 100 % efficiency;

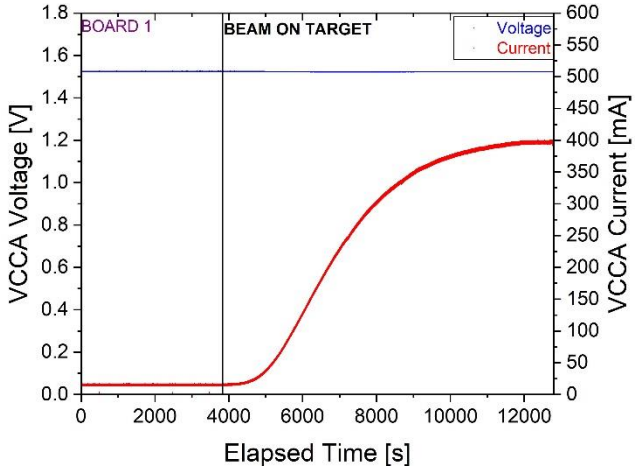
- 1 SEU and 2 SET events in the "LHCb RICH – like" firmware due to high dose rate (~ 1 krad/s) and high TID 8 Mrad (Si):
  - one sample was tested for a fluence of 2.5 x 10^{13} protons/cm^2;
  - upper limit for SETs: 0.18 x 10^{-9} cm^2/device;

- The embedded SRAM prove to be sensible to proton induced SEUs:
  - one sample was tested for a fluence of 5 x 10^{12} protons/cm^2;
  - 3.6 x 10^{-14} cm^2/bit (26 % error);
  - 1.39 x 10^{-9} cm^2/device (26 % error);
  - Compared with the Kintex-7: ~ 0.7 x 10^{-14} cm^2 /bit (40 % error);
    - Caveat, for antifuse we can apply TMR with 100 % efficiency, if we use non-volatile resources;

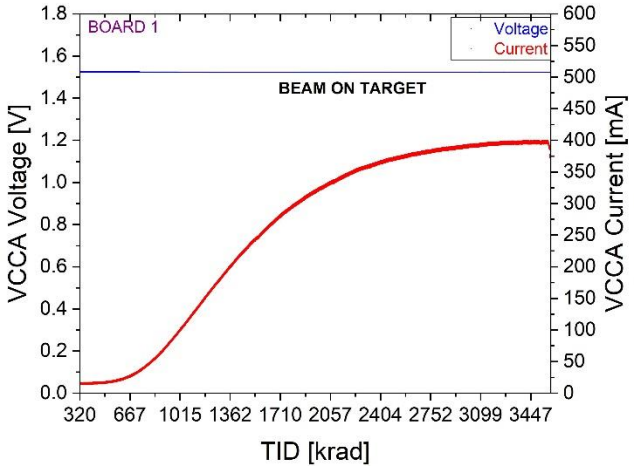
Irradiation Results

- Up to 320 (±80) krad (Si) with a average dose rate of 154 rad/s we didn't see any major current increase in the DUT's power rails;

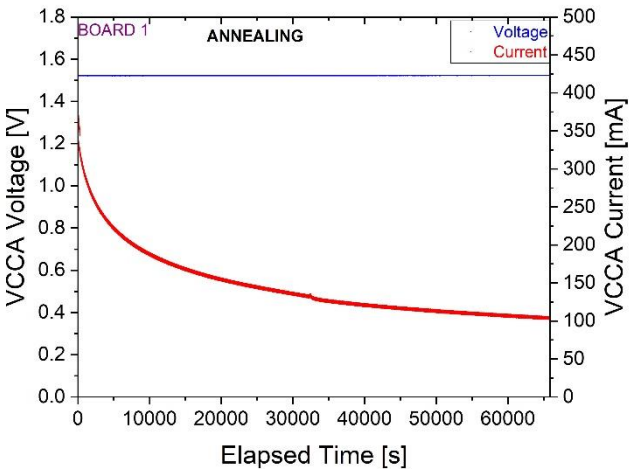
- However, when we moved to higher TID with or without higher dose rate, the current increasings start to appear in all 7 power rails of the DUT:
  - the TID effects are more persistent in the main core power rail;
  - around 300 krad (Si) TID seems to be the threshold for the current increasings.



Core current increasing for 363 rad/s dose rate up to 3.2 Mrad (Si) TID



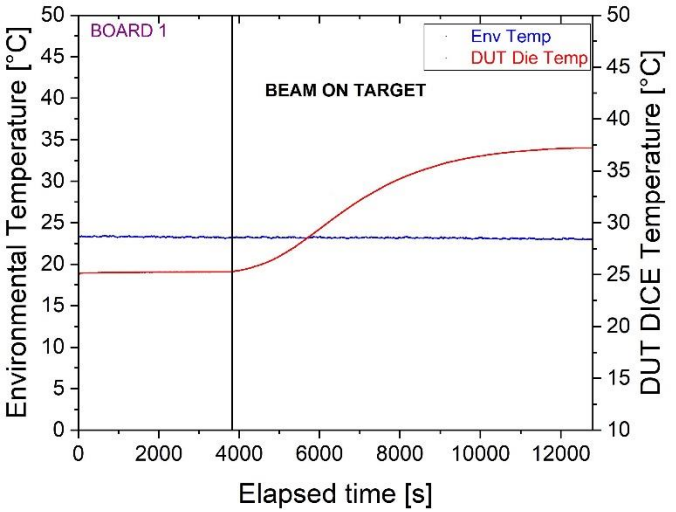
Core current vs TID for 363 rad/s dose rate up to 3.2 Mrad (Si) TID



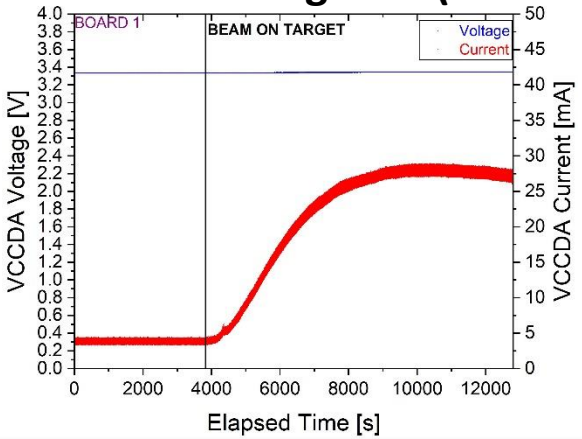
Annealing of the core voltage after 3.2 Mrad (Si) TID

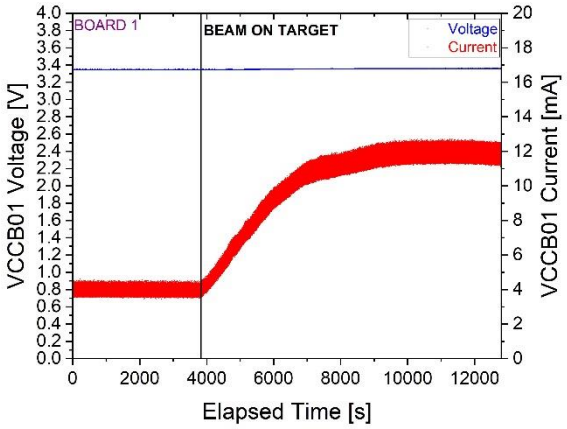
Irradiation Results

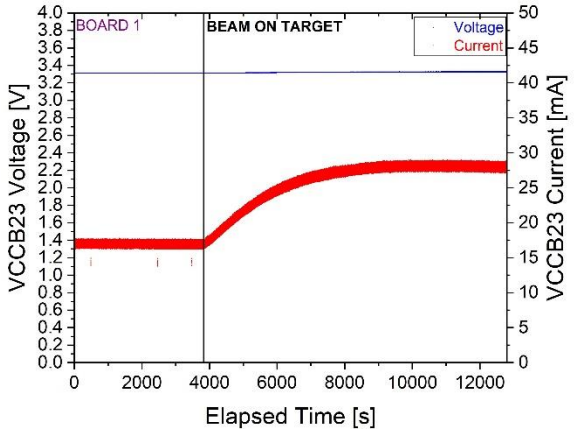
- The other power rails were also affected by the same TID effects:
  - VCCDA => voltage rail for JTAG, I/O differential amplifiers and probes;
  - VCCB01 => voltage rail for I/O Bank 0 & 1;
  - VCCB23 => voltage rail for I/O Bank 2 & 3;



- While the dissipated power increased due to TID effects, the DUT's DICE temperature increased with almost 12 degrees. (363 rad/s)



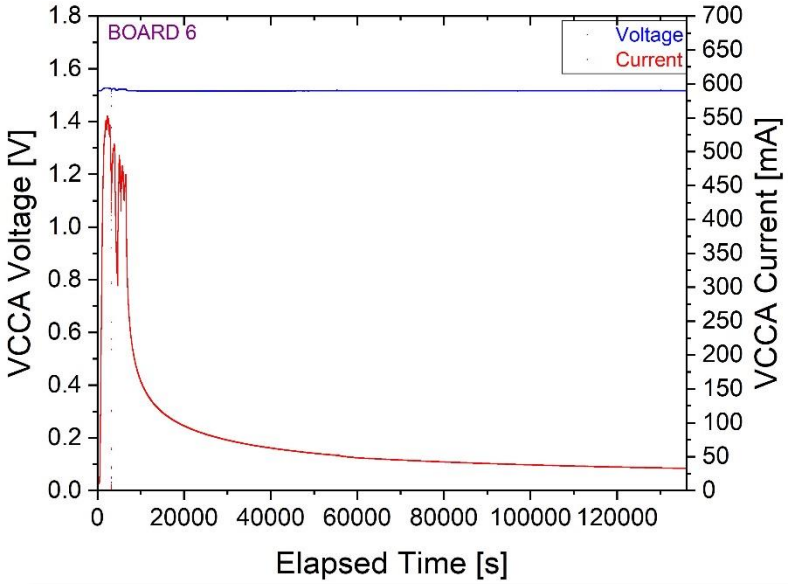


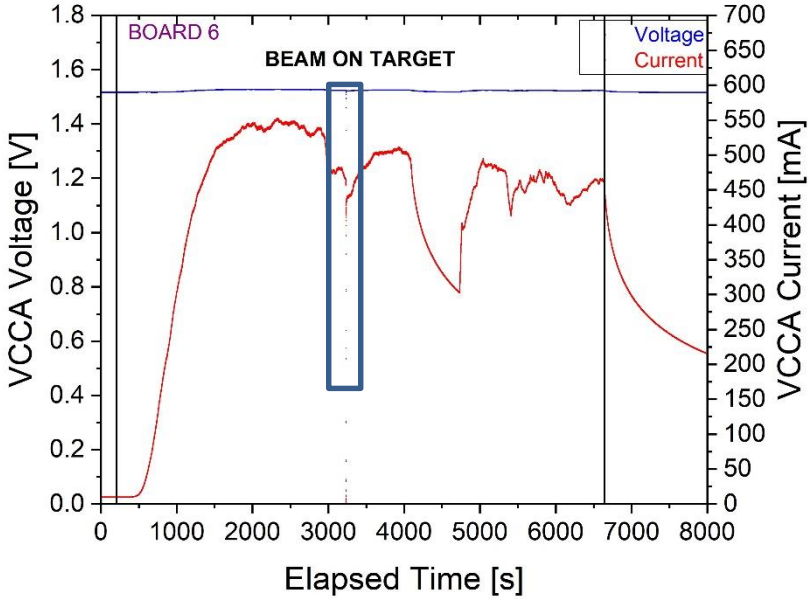


Current increasings in multiple power rails for 363 rad/s dose rate up to 3.2 Mrad (Si) TID

Irradiation Results

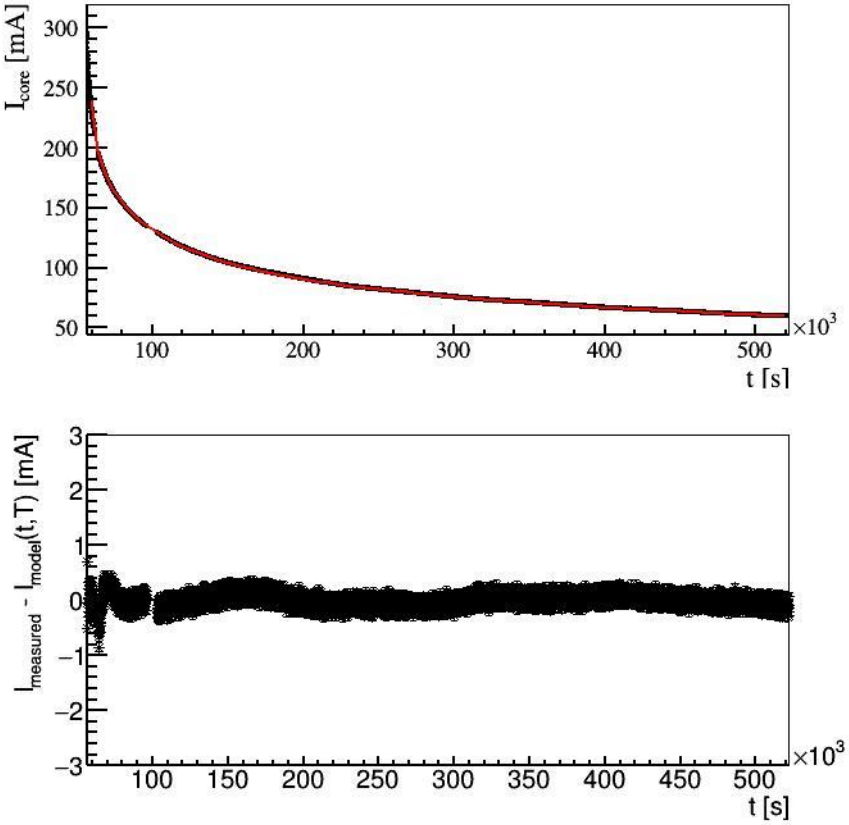
- One sample was irradiated with 1 krad/s up to 8 Mrad (Si) TID;
- We saw one SEU which froze the entire logic;
  - recovered with a power cycle;
- The current variations are corelated with the beam fluctuations;
- Very strong room-temperature annealing.





Irradiation Results

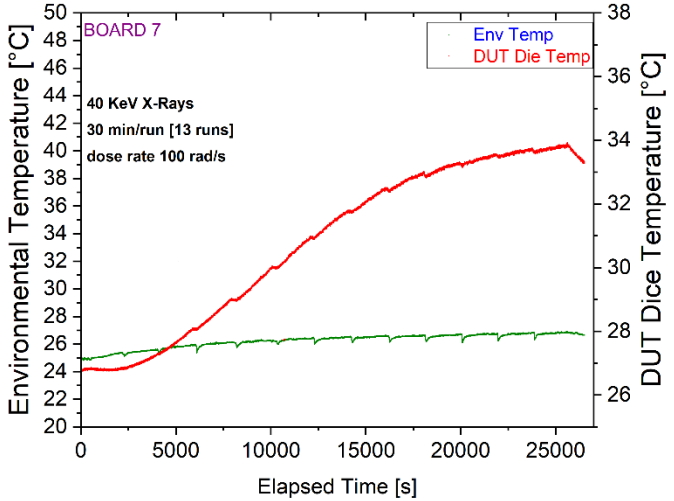
- Based on the measurements done with protons we are trying to parametrize the annealing curve of the device;
- After 10^{13} protons/cm^2 at more than 20 MeV energy we have in 7-8 weeks complete annealing of the TID component;
- These fits are preliminary and still ongoing.

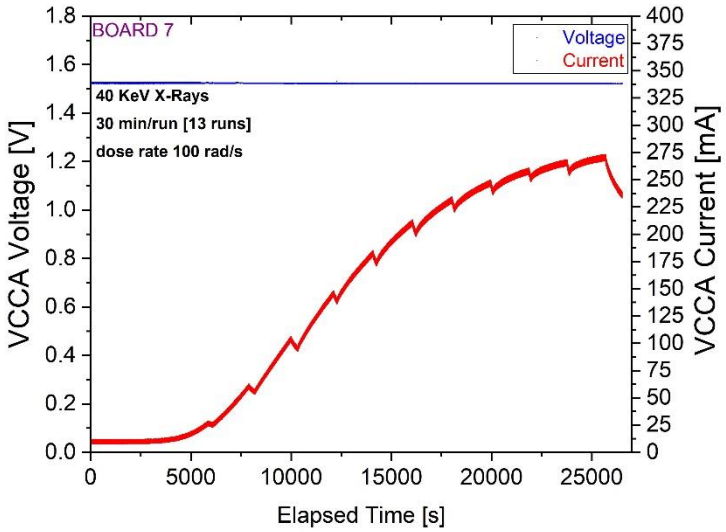


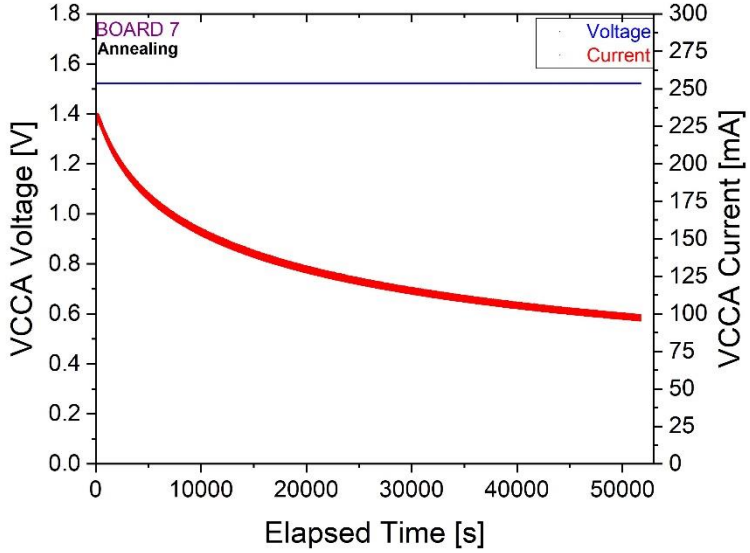
X-RAYS

Irradiation Results

- We used 10 - 40 keV X-Rays from SIRAD X-Ray facility:
  - 2 samples were irradiated;
  - one with 13 runs of 30 minutes each at 100 rads/s => 180 krad/run;
  - TID => 2.3 Mrad (Si);
  - The TID proton induced effects were confirmed by the X-Ray runs;







Summary & Conclusions

- 7 boards with different firmware architectures were tested with protons and X-Rays;
  - 3 with TMR firmware, 1 with "LHCb RICH-like" firmware, and 1 with SRAM readout firmware with protons;
  - 1 with TMR firmware and 1 with "LHCb RICH-like" firmware with X-Rays;
- 1 board was tested up to 8 Mrad TID with protons:
  - For HL-LHC extrapolations, Upgrade Phase II (2 Mrad TID);
- The FPGA proved to be resilient to high dose rates and high TID up to 8 Mrad (Si);
  - Caveat, provided we show with our fit model that in realistic conditions the threshold is never reached;
- Very low error rates:
  - Except for 1 SEU, most of the logic SEUs were masked by the TMR architecture;
- High leakage current was seen in the DUT's core power rail at high TID with very high dose rate, over 0.3 Mrad (Si);

Summary & Conclusions

- The current variations are correlated with the high dose rate and other environmental parameters;
  - most fast changes are due to beam fluctuations and annealing;
- Annealing tests have been carried out after TID tests;
  - very strong room-temperature annealing of the device;
- Due to small dose rate expected in LHCb sub-detectors, we expect this effect to be removed or to be orders of magnitude smaller;
- We will parametrize the rise and annealing curves and propagate/extrapolate the results to LHCb-RICH environment;
- Draw-backs:
  - Small number of resources compared with SRAM-based FPGAs;
  - Not a reconfigurable device => one time programming device.