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Investigation of Proton Induced Radiation Effects in 0.15 μm CMOS Antifuse FPGA

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Considered as a back-up solution of the upgraded LHCb RICH sub-detectors, the antifuse FPGAs have been seen as a viable solution to be used in the harsh radiation environment of high energy physics and space experiments. This study is a summary of test beam results performed on a 0.15 μm CMOS antifuse device with a proton beam. We are characterizing the FPGA behavior under large TID and high dose rate conditions, and we are using the obtained results to extrapolate to HL-LHC conditions.

Summary

The Axcelerator family are antifuse FPGAs from Microsemi designed in the 0.15 μm CMOS antifuse technology. They are considered the backup solution in the digital boards of the upgraded LHCb RICH detectors. A proton irradiation campaign is ongoing, in view of testing and qualifying radiation tolerance under radiation environment equivalent to 50 fb-1 integrated LHC luminosity and beyond to HL-LHC, by analyzing the device response for Total Ionising Dose (TID) effects, Displacement Damage (DD) and Single Event Effects (SEEs). A sizeable FPGA sample is to be used with a TID in excess of 200 krads at the Legnaro National Laboratories in Italy scheduled for the middle of May.

For this purpose, a custom FPGA-based data acquisition system (DAQ) has been designed to monitor the activity of the device under test (DUT) during and after irradiation. The DAQ is able to monitor the power consumption on all important voltage rails and also to monitor and control the DUT internal logic status. The hardware logic inside DUT will be running at 40 MHz or higher, and with a firmware architecture which is based mostly on Flip-Flops (FF), R-Cells, and a few combinational cells, C-Cells, used to implement gate based operations like a Triple Modular Redundancy (TMR) voter and an additional minority voter. Another firmware architecture implies I/O trigger readout, and will be used to test the I/O blocks vulnerability with a firmware which is closest to the target HL-LHC application. The test bench includes a precise temperature monitoring and dose rate which will allow to obtain good estimates for fit parameters on current increasing with TID and annealing. All the electrical and logical parameters are sampled at a user configurable rate,100 Hz maximum, and are sent through ethernet to an LabVIEW based graphical user interface. The acquired data is displayed and saved in ASCII files for later analyses.

Using 20 - 26 MeV proton beam, the FPGA will be tested for TID effects, DD and SEE. We will measure the SEE occurrence in dedicated hardware resources like: R-Cells, C-Cells, Embedded RAM and I/O blocks. Furthermore, the possibility of using this device family in the next upgrade of the LHC, HL-LHC, and space experiments is also investigated and the results are extrapolated.

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