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28 nm high-k bulk digital circuit performance (SEU) after Heavy Ion exposure

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This paper presents the results of a Single Event Upset (SEU) test with heavy ions on a shift register manufactured in a 28nm commercial CMOS technology, interesting for future upgrades for HL-LHC. Results will show the cross section curve in a Linear Energy Transfer (LET) range between 3-60 MeV·cmˆ2/mg for different patterns.

Summary

The HL-LHC upgrade at CERN will increase of a factor 10 the collision rate. Silicon Vertex Trackers will require to read out large area sensor matrices of highly pixellated detectors with low power consumption, high level of processing and rad-hard. In order to comply with such challenging requirements, designers are considering to move to higher density CMOS technology nodes for the pixel readout channels. However, it is well known that shrinking technology feature size, increasing operating frequencies and lower power voltages have caused single event soft errors to be one of the key reliability issues in advanced Integrated Circuits.

Within the INFN Scaltech28 project, we have designed a flip-flop based shift register, composed of 1024 cells, to establish the radiation sensitivity to Single Event Upsets (SEU) of a commercial 28 nm high-k technology. The Shift Register single cell is based on a master-slave positive edge-triggered D Flip-Flop, composed by two gated D latches with inverted enable signal (the clock signal (CLK), in this case) between the two cells. The CLK signal is buffered after each Flip-Flop cell in order to maintain 50% duty cycle. Each D-latch is based on a SR-NAND latch scheme. A fully custom layout design ensures the single cell dimensions to be kept the minimum allowed by the 28 nm CMOS technology DRC rules. The single Flip Flop cell dimensions are 6×1.025 µm2 for an overall area occupancy of 116.7×80.7 µm2 for the entire shift register. No particular layout techniques were exploited in this design in order to increase the shift register radiation hardness performances.

The chip has been exposed to heavy ion irradiation at the SIRAD irradiation facility of the INFN Legnaro Laboratories. We reconstructed the SEU cross section as a function of the Linear Energy Transfer (LET) of the particles impinging on the chips (the Weibull curve); LET values were chosen in order to cover as much as possible the cross section curve: they ranged from the threshold through the "knee", up to the plateau region (> 40 MeV·cm2/mg).

During irradiation, a known binary path was given as input and the same pattern was checked at the output; whenever a difference was detected between the input and the output pattern, then a Single-Event occurred. Different patterns were written into the register in order to establish different sensitivities. Results show that the different patterns exhibit different slightly different LET threshold values (< 3 MeV·cm2/mg) and saturation cross sections (in the order of 10-8 cm2 per bit).

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