Radiation hard Depleted Monolithic Active Pixel Sensors with high-resistivity substrate

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Outline

• The ATLAS Inner Tracker (ITk) upgrade for HL-LHC
• The H35 large area demonstrator chip
  • Monolithic matrix readout and tuning
  • Beam test measurements
• The new LF2 chip
• Conclusions and outlook
ATLAS upgrade for HL-LHC

- LHC
  - 19 Pile-up events

- HL-LHC
  - 140-200 Pile-up events
    - High particle multiplicity
    - Critical radiation damage

Insertable B-Layer (IBL): forth pixel layer at 3.2 cm from the beam line

“Phase II”: full inner detector replacement (5 pixel layers)
Replace the whole ATLAS Inner Detector with a new full-silicon Inner Tracker (ITk)

- New pixel detector layout with 5 barrel layers

Sensor technologies under investigation:
  - Outer pixel layers (large area to cover)
    - HR/HV-CMOS monolithic pixel detectors $\Rightarrow$ $\sim 1e15 \times n_{eq} \text{cm}^{-2}$
    - Hybrid detectors with n-in-p planar silicon sensors (150 µm thick)
  - Inner pixel layers (Radiation hardness)
    - Hybrid detectors with thin n-in-p planar silicon sensors (100 µm thick)
    - Hybrid detectors with 3D silicon sensors (baseline for innermost layer)

* safety factors not included
Hybrid vs. Monolithic

Hybrid detector

- Sensor + chip

**PRO:**
- Sensor and chip can be optimized separately
  - radiation hardness
  - high rate capability (MHz/mm\(^2\))
- Complex signal processing already in the pixel cell

**CON:**
- Relatively large material budget
  - multiple scattering
- Complex production and assembly
  - expensive!!

Monolithic detector

- All in one piece

**PRO:**
- Commercial technology
- No interconnection costs
  - cost effective!!
- Low material budget
  - low multiple scattering

**CON:**
- Functionalities limited by the size of pixel and dead area at the periphery
- Signal obtained by diffusion
  - slow!!
  - not radiation hard!!
Hybrid vs. Monolithic

Monolithic detector
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  - PRO:
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Hybrid detector
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How to overcome these limitations in the present CMOS technology?
- Smaller and more radiation hard electronics
  - CMOS process can go down to 150 nm and less
  - Depleted Monolithic Active Pixels Sensors (DMAPS)
    - High voltage
    - High resistivity
    \[ d \propto \sqrt[\rho]{V} \]
Two different philosophies:

- **Electronics inside the n-well**
  - Large fill factor: isolation of p-well inside a deep n-well
  - Large sensor capacitance (~100 fF)
  - More uniform electric field
  - Shorter drift distance
  - Radiation hardness*

- **Electronics outside the n-well**
  - Small fill factor
    - Very small sensor capacitance (~5 fF)
  - Low electric field regions
  - Longer drift distance
  - Radiation hard??

*already proven on CCPDs: M.Benoit et al., JINST 13 (2018) no.02, P02011

See: Bojan Hiti talk on Friday
Two different philosophies:

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Design characterized in this presentation

*See: Bojan Hiti talk on Friday*
The H35 large area demonstrator chip
The H35 Demonstrator

AMS 350 nm High Voltage CMOS: different $\rho$: 20–80–200–1000 $\Omega$cm

- Monolithic nMOS matrix:
  - Digital pixels with in-pixel nMOS comparator
  - Two flavors: with and without Time Walk compensation

- Analog matrices (2 arrays):
  - To be Capacitive Coupled (CC) to FE-I4 readout chips (pitch 50x250 $\mu$m²)
    
    \[ M. \ Benoit \ et \ al., \ arXiv:1712.08338 \]

- Monolithic CMOS matrix:
  - Analog pixels with off-pixel CMOS comparator
    - One comparator in the left sub-matrix
    - Two comparators in the right sub-matrix

+ test structures without electronics for Transient Current Technique (TCT) studies

\[ E. \ Cavallaro \ et \ al., \ JINST \ 12 \ (2017) \ no.01, \ C01074 \]
The H35 Demonstrator

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EMS 350 nm High Voltage CMOS: different $\rho$: 20–80–200–1000 $\Omega$cm

Designed by KIT, IFAE and Univ. of Liverpool

Large collaboration

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The H35 pixel structure

- **Pixel size:** 50x250 μm²

- **Large fill factor:**
  - nMOS and pMOS transistors embedded in the same deep n-wells acting as collecting electrodes
  - p-substrate + 3 separate deep n-wells* to reduce the capacitance
    - reduce the noise, improve timing - power consumption
  - Short charge drift
    - reduced trapping after irradiation
  - More uniform electric field

- **Bias voltage applied from the top:**
  - Single side processing
  - Bias voltage > 100 V

*all matrices but monolithic nMOS
The monolithic CMOS matrix

- Analog electronics in pixel
  - CSA, shaper and a second stage amplifier

- Digital electronics in the periphery
  - ReadOutCell (ROC)
  - End Of Column (EOC)
  - Control Unit (CU)

- Off-pixel discriminators in the ROC:
  - 1 in the Left part (left sub-matrix)
  - 2 in the Right part (right sub-matrix)
    - Additional time-stamp for better timing

- Column drain readout architecture with priority encoding
  - Trigger-less readout
  - No zero-suppression

Both implemented in the FPGA firmware
**IV characteristics**

- **IV curves before irradiation show a breakdown between 160 and 185 V**
  - Strange behavior of the 1 kOhm sample which shows a Rise And Fall (RAF) effect

- **H35Demo chips have been irradiated:**
  - At JSI, Ljubljana with reactor neutrons up to $2 \times 10^{15}$ $n_{eq}/cm^2$ (~2 Mrad)
  - At the KIT cyclotron with 23 MeV protons up to $1 \times 10^{15}$ $n_{eq}/cm^2$ (~150 Mrad)

- **After irradiation devices exhibit breakdowns around 140-160 V**
  - The current rises consistently with the irradiation fluence

- **Charge collection studies before and after irradiation were carried out on TCT structures:** *E. Cavallaro et al., JINST 12 (2017) no.01, C01074*
Monolithic matrix readout and tuning
Monolithic matrix readout at IFAE

Trigger board
- Trigger in
- Busy out
- RJ45

H35demo chip
- Both CMOS and nMOS matrices wire-bonded

H35demo PCB
- Voltage regulators
- Sensor bias input
- Injection pulse input
- Analog signal output

FPGA board
- Xilinx ZC706

Adapter PCBs
- 1x H35 PCB
- 1x test signals
- 1x trigger board

External
- Pulse generator
- Power supplies

S. Terzo et al., JINST 12 (2017) no.6, C06009
Monolithic CMOS matrix tuning

- **CMOS matrix tuning (not irradiated):**
  - Injection capacitance: 0.84 fF from simulation (confirmed by x-ray fluorescence)
  - Min. achieved threshold: 1300 ± 130 e
  - Threshold noise = 180 ± 26 e
Threshold tuning after irradiation

- After irradiation the minimum achievable threshold is around 1800 e

- The threshold noise is higher than before irradiation (230 – 300 e), but mostly confined within 400 e

- Tuning optimized for the left sub-matrix to reach lower thresholds
  - Beam test analysis after irradiation focused on the left part only
Beam test measurements
Efficiency before irradiation

- **Fermilab beam test**
  - 120 GeV protons
  - IFAE in collaboration with UniGe & Argonne Lab
  - UniGe FE-I4 telescope* + IFAE readout
  - Not irradiated chips of 20,80,200 Ωcm

*M. Benoit et al., JINST 11 (2016) no.7, P07003

- **Hit efficiency results:**
  - Better performance with resistivity ≥ 80 Ωcm:
    - Full efficiency with just 50-80 V
    - 20 Ωcm needs 160 V
Efficiency after irradiation

- **Beam test at CERN SPS and DESY**
  - 180 GeV pions at CERN SPS and 4 GeV electrons at DESY
  - IFAE readout + UniGe FE-I4 (@SPS) or EUDET (@DESY) telescopes
  - 200 Ωcm neutron (@JSI) and proton (@KIT) irradiated up to 2e15 \( n_{eq}\) cm\(^{-2}\)

- **Hit efficiency results:**
  - > 98% efficiency measured after both proton and neutron irradiations up to 1e15 \( n_{eq}\) cm\(^{-2}\) with ≥ 130 V
Efficiency vs. Threshold

- **Sample irradiated in JSI with neutron to $1e15$ n$_{eq}$cm$^{-2}$**
  - Efficiency measured at the DESY beam test
  - Operated at 150 V with different thresholds

- **99% efficiency with 1800 electrons threshold:**
  - The efficiency starts dropping with higher thresholds
  - Inefficiency due to charge sharing is localized in the cell boundary and in particular in the four corners of the pixel
Noise occupancy

- **Noise occupancy measured at stable temperature in a climate chamber**
  - For non-irradiated device at 20°C, for irradiated devices at -35°C
  - Acquisition of 5 minutes without external sources
  - Up to 5 most noisy pixel masked (less than 1% of the total pixels in the left sub-matrix)

- **Noise occupancy can be kept below $10^{-6}$ hits per 25 ns (ATLAS requirement)**
  - With chip irradiated with up to $10^{15}$ $n_{eq}$ cm$^{-2}$
  - For thresholds $\geq 1700$ e at the bias voltage of 120/150 V

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**Graph:**

- **PRELIMINARY**
- Noise occupancy [hits/(25 ns)]
- Threshold [ke]

- $[\Phi] = 10^{14}$ $n_{eq}$/cm$^2$
- $\Phi=0$, $U=150$ V - D5
- $\Phi=1$ (p), $U=150$ V - E10
- $\Phi=5$ (n), $U=150$ V - E5
- $\Phi=10$ (n), $U=150$ V - E7
- $\Phi=10$ (p), $U=120$ V - H7
- $\Phi=15$ (n), $U=150$ V - D6
- $\Phi=20$ (n), $U=150$ V - D9
The new LF2 chip
**High resistivity / High Voltage Monolithic Active Pixel prototype**
- 150 nm HV-CMOS process from LFoundry
- Two wafers of 500 Ω·cm and 1900 Ω·cm
- Small fully monolithic matrix of 40 x 78 pixels (3.9 x 2 mm²)
- Pixel size: 50 x 50 µm²
- Collaboration of IFAE, Uni. of Liverpool, Uni. of Geneva and KIT


**Triple well technology**
- Additional buried isolation layer for integration of analogue and digital electronics in the sensitive area of the pixel
- Two time-stamps for Time-over-Threshold (ToT) and offline Time Walk correction

**Four different sub-matrices**
- Two include pixel with Metal-Insulator-Metal (MIM) feedback capacitors
- Two pixels with diffusion feedback capacitors
- Two additional variants:
  - with linear transistors
  - with few circular transistors to make the pixels more radiation hard
**LF2 – first IVs**

- **First chips successfully produced and delivered**
  - Readout system with baby-boards developed at IFAE
  - Successful communication with the chip
    - Read and write of the shift registers and DAC registers
    - Monitoring of the DAC currents

- **Measurements of the leakage current of TCT structures:**
  - Breakdown around 50-60 V
  - Expected at 60 V from simulations [E. Vilella, Uni. Liverpool]

- **Leakage Current**
  - 1900 Ωcm
  - 500 Ωcm

- **PRELIMINARY**
Conclusions and outlook

- **Radiation hardness of the H35DEMO monolithic chip**
  - **Before irradiation:**
    - Better performance for high resistivity substrates (80-200 Ωcm) \(\Rightarrow\) larger depletion
    - Detection efficiency around 99% with a bias voltages \(\leq 80\) V
  - **After irradiation:**
    - Proven radiation hardness of the large fill factor design
      - Up to proton and neutron irradiation to \(1e15\) \(n_{eq}/cm^2\): \(>98\)% hit efficiency at \(\geq130\) V
      - Noise occupancy can be kept lower than \(10^{-6}\) hit in an LHC bunch crossing (25 ns)
      - Thresholds as low as \(1800\) e are necessary to get to these results

- **LF2 chip**
  - Analog and digital functionalities in a 50x50 μm² pixel size
  - First measurements show that the chip is working and behaving as expected from simulations (breakdown around 50-60 V)
  - Further measurements and characterisation ongoing

- **What’s next?**
  - New monolithic prototypes for ATLAS already designed and produced
    - ATLASPix1: 180 nm HV-CMOS AMS process (see Mridula Prathapan poster)
  - The challenge for the large fill factor is the 25 ns in time efficiency which will need to be investigated in the new prototypes
Backup slides
First estimation of the injection capacitance for the CMOS matrix of the H35DEMO chip was obtained from simulations: 0.84 fF.

Measured also with the X-ray fluorescence setup at CERN:
- Very first estimations in agreement with the simulated value.

Threshold [V]

NEntries

<table>
<thead>
<tr>
<th>E_k = 6400 eV</th>
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<tbody>
<tr>
<td>4500</td>
</tr>
<tr>
<td>4000</td>
</tr>
<tr>
<td>3500</td>
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<tr>
<td>1000</td>
</tr>
<tr>
<td>500</td>
</tr>
<tr>
<td>0</td>
</tr>
</tbody>
</table>

Threshold [V]
Sensor characterization

- **H35 pixel cell structure**
  - p-substrate + 3 deep n wells
    - Lower capacitance (noise, timing)
    - Reduce trapping
  - Bias from the top -> single sided

- **Characterization of H35 test structures:**
  - 3x3 pixel structures w/o electronics
  - **External pixels** shorted together
  - Separate readout of the central pixel
  - $\rho = 80 \, \Omega cm - 200 \, \Omega cm - 1 \, k\Omega cm$

- **The Edge-TCT setup:**
  - Infra-red laser (1064 nm)
    - Beam spot about 10 $\mu m$ FWHM
    - Pulses of about 500 ps
  - Readout: DRS4 evaluation board
    - 700 MHz bandwidth
    - 5 GSPS
    - 200 ns sampling depth
    - Four channels: 1 $\times$ trigger, 1 $\times$ beam monitor, 2 $\times$ readout
Depletion: before irradiation

- Depletion depth is defined by the FWHM of the charge collection profile

\[ d(V) = d_0 + \alpha \sqrt{\rho V} \]

with \( \alpha = \sqrt{2\varepsilon\varepsilon_0\mu} \)

<table>
<thead>
<tr>
<th>Sensor</th>
<th>( \rho ) nominal</th>
<th>( \rho ) measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensor 1</td>
<td>80 ( \Omega )cm</td>
<td>50 ( \pm ) 11 ( \Omega )cm</td>
</tr>
<tr>
<td>Sensor 2</td>
<td>200 ( \Omega )cm</td>
<td>230 ( \pm ) 49 ( \Omega )cm</td>
</tr>
<tr>
<td>Sensor 3</td>
<td>1000 ( \Omega )cm</td>
<td>4500 ( \pm ) 300 ( \Omega )cm</td>
</tr>
</tbody>
</table>

- Resistivity obtained fitting the depletion depth as a function of the bias voltages
Depletion: before irradiation

When depletion gets larger of 100 µm the central pixel starts to collect charge from the neighboring pixels.
Depletion: after irradiation

- Irradiation at the TRIGA neutron reactor at JSI, Ljubljana:
  - Now: 2e14, 5e14, 10e14, 20e14 n$_{eq}$cm$^{-2}$
  - Next steps: 5e15 and 1e16 n$_{eq}$cm$^{-2}$

- Acceptor removal effect visible for lower substrate resistivities which leads to an increase of the depletion depth after irradiation up to 2e15 n$_{eq}$cm$^{-2}$

- Due to the low initial acceptor concentration in the 1000 Ωcm sample the creation of stable acceptors dominates and the depletion depth decreases after irradiation
Effective doping concentration

- Effective doping concentration obtained from:

\[ d(V) = d_0 + \alpha \sqrt{\rho V} = d_0 + \sqrt{\frac{2\varepsilon \varepsilon_0}{eN_{eff}} V} \]

\[ N_{eff} = N_{eff0} - N_c \cdot (1 - \exp(-c \cdot \Phi_{eq})) + g_c \cdot \Phi_{eq} \]

Initial doping | Acceptor removal | Acceptor introduction

<table>
<thead>
<tr>
<th>Sensor 1 (80 Ωcm)</th>
<th>Sensor 2 (200 Ωcm)</th>
<th>Sensor 3 (1 kΩcm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( N_c ) [10(^{-14}) cm(^{-3})]</td>
<td>1.8 ± 0.4</td>
<td>0.7 ± 0.5</td>
</tr>
<tr>
<td>( c ) [10(^{14}) cm(^2)]</td>
<td>0.5 ± 0.2</td>
<td>0.3 ± 0.3</td>
</tr>
<tr>
<td>( g_c ) [cm(^{-1})]</td>
<td>0.02 ± 0.01</td>
<td>0.07 ± 0.04</td>
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</table>

After about 1e15 n\(_{eq}\)/cm\(^2\), \( N_{eff} \) tends to the similar values for all resistivities

E.Cavallaro et al., JINST 12 (2017) no.01, C01074
• 200 Ωcm chips have been irradiated with neutrons in the TRIGA reactor in Ljubljana up to 2e15 n_{eq}cm^{-2}

• And at KIT with 23 MeV protons up to 1e15 n_{eq}cm^{-2} (about 150 Mrad)

• We observed a digital pattern in the injection test:
  • After proton irradiation >=1e14 n_{eq}cm^{-2}
  • After neutron irradiation >=1e15 n_{eq}cm^{-2} at low temperature
• The number of pixel misbehaving increases with the fluence and it is particularly enhanced for proton irradiations
Address crosstalk

- The 16x300 analog pixels in the CMOS matrix are connected one-to-one to 40x120 pixels in the digital periphery.

- The addresses are generated in the periphery with adjacent transistors.

- Due to strong capacitive couplings between adjacent lines it is possible to have crosstalk between addresses.

- This has been corrected in the design of the H18 ATLASPix1 by adding additional capacitors between the lines.

```
1 0 1
1 -> 0 <-1
1 1 1
```
Solution

- Standard settings of the digital voltage: VDDD = 3.3V

- Increasing VDDD from 3.3V -> 5V

- The digital voltage needs to be increased depending on the irradiation levels:
  - Proton irradiated samples require very high VDDD which lead to a noise increase
  - Neutron irradiated samples require instead moderate VDDD increase (less than 4V)
Power vs. rise time

- Simulation of the power consumption as a function of the rise time for analog pixels with high gain
- For low gain pixels (-p-tub +extra capacitor) the rise time can go down to 20 ns with aggressive settings

Measured on monolithic CMOS matrix

E. Vilella et al. JINST11 (2016) C01012
Possible CMOS devices

- **Depleted Si sensors produced in High Resistivity/High Voltage CMOS technology**
  - Charge generated in a small depleted region
  - Industrial CMOS process
  - potentially cheaper to cover large areas (full ITk pixels ~14 m²)

- **Investigating the possibility of a 5th pixel layer of CMOS for ITk:**
  - Hybrid passive pixel detectors:
    - Industrial CMOS process potentially cheaper
    - Standard interconnection to Front End chips

- Hybrid Active Capacitive Coupled Pixel Detectors (CCPDs):
  - Active: in pixel amplification
  - Glue interconnection ➔ reduced costs wrt. bump bonding
  - Already proven radiation hardness: “M. Benoit et al., arXiv:1611.02669“

- **Fully Monolithic Active Pixel Sensors (MAPS):**
  - On chip discriminator and digital electronics
  - No interconnection costs
  - Reduced material budget
LF2 analog FE electronics

- **Schematic diagram of the pre-amplifier**
  - Single folded cascode amplifier with a PMOS input transistor
  - The sensor is AC coupled to the detector via a coupling capacitance $C_c$ of 130 fF

- **Cross-section of transistors M1 and M0**

- **Diffusion feedback capacitor**
  - No PSUB below the transistors of the pre-amplifier
  - $C_f$ is formed by the parasitic drain-bulk capacitance of M1

- **MIM feedback capacitor**
  - $C_f$ is a 1.2 fF Metal-Insulator-Metal (MIM) capacitor
  - M1 and M2 isolated from the DNWELL by a PSUB isolation layer
Time resolution of H35 CCPDs

Time Distribution constrained to less than 50 ns for V > 80 V

Not affected significantly by the gain or the feedback transistors used

Time resolution dominated by the intrinsic jitter of the pre-amplifier

M. Benoit et al., arXiv:1712.08338