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Radiation hard Depleted Monolithic Active Pixel Sensors with high-resistivity substrate

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The H35DEMO is a HV/HR-DMAPS large area chip fabricated in AMS 350nm HV-CMOS technology. It includes two monolithic matrices with pixels of $50 \times 250 \mu m^2$ with analog electronics embedded in a Deep N-WELL also acting as collecting electrode.
Chips were irradiated with both protons and neutrons up to the radiation doses expected for the outermost layers of the ATLAS pixel detector at HL-LHC and their radiation hardness was investigated in beam test experiments.
Results of these characterisations will be presented and a new LFoundry 150nm production including HR/HV-MAPS featuring sensors with $50 \times 50 \mu m^2$ pixels will be introduced.

Summary

High Voltage/High resistivity Depleted Monolithic Active Pixel Sensors (HV/HR-DMAPS) is a technology which is becoming of great interest for high energy physics applications.
With respect to hybrid pixel detectors the monolithic approach offers the main advantages of reduced material budget and production costs due to the absence of the bump bonding process. The latter aspect is important especially when large areas need to be covered as in the tracking detectors of the LHC experiments. Thus, the possibility of employing this technology in the outermost layers of the upgraded ATLAS pixel detector at HL-LHC is being investigated.

Different HR/HV-DMAPS prototypes have been recently developed for the future ATLAS Inner Tracker (ITk) with the aim of studying their radiation hardness and the feasibility of producing large area devices.

The H35DEMO is a large area demonstrator chip for the ITk designed by KIT, IFAE and University of Liverpool and produced in AMS 350 nm HV-CMOS technology with an engineering run on four different substrate resistivities: 20, 80, 200 and 1000 Ωcm. It consists of four large matrices, two of which include digital electronics and are thus fully monolithic. One, called CMOS matrix, has comparators made of CMOS transistors in the periphery only, while the other, called NMOS matrix, includes also comparators made of NMOS transistors directly in the pixels. The other two matrices have only analog front-end electronics and are meant to be coupled to ATLAS FE-I4 chips. All matrices feature pixels with a size of 50x250 μmˆ2 in which the analog electronics are embedded in a Deep N-WELL (DNWELL) also acting as collecting electrode.

A Data Acquisition (DAQ) system was developed at IFAE to read out and test the monolithic matrices of the H35DEMO both in the laboratory and with beam test experiments. Irradiation campaigns were carried out at KIT and Ljubljana, where 200 Ωcm chips have been irradiated with protons up to a particle fluence of 1e15 1MeV n_{eq}/cmˆ2, and reactor neutrons up to a fluence of 2e15 1MeV n_{eq}/cmˆ2.
The CMOS matrix of the H35DEMO chip was extensively characterised before and after irradiation in beam tests at CERN SPS, Fermilab and DESY, with pion, proton and electron beams, respectively.

These very first results after irradiation of a full size monolithic chip for ATLAS show good performance in terms of hit efficiency up to the expected fluence for the outermost pixel layer of ITk (1e15 1 MeV n_{eq}/cmˆ2), and will be presented in this contribution.

Another production of monolithic HV-CMOS prototypes in LFoundry 150 nm technology (LF2) has been recently completed. It includes sensors with a similar DNWELL concept as the H35DEMO but with a smaller

pixel size of 50x50 µmˆ2. Design and preliminary measurements of LF2 chips will be also presented.

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