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The Barrel Calorimeter Processor demonstrator board for the Phase II Upgrade of CMS

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In order for the CMS electromagnetic and hadronic calorimeters in the barrel region (EB, HB) to support the high-luminosity upgrade of the LHC, the off-detector electronics (Back-End) must be replaced. For EB, the new Back-End has been designed to take over functions of the legacy Front-End electronics in order to handle the required increase in the sampling frequency and the granularity of the system. In addition, both upgraded EB and HB must cope with phase II upgrade technical requirements. On the roadmap to a prototype hardware platform, the Barrel Calorimeter Processor demonstrator board (BCP demo) has been designed.

Summary

The phase II upgrade of the LHC is foreseen for the 2023-2025 timeline. In order to cope with the increase of the luminosity from 2×10^34 cm-2 sec-1 (phase I upgrade) to 7.5×10^34 cm-2 sec-1 and 200 Pile-Up, the CMS electromagnetic calorimeter (ECAL) in the barrel region (EB) will be upgraded. The upgrade concerns replacement of the on-detector and off-detector electronics where existing functions of the legacy Front-End (FE) will be moved to a new Back-End (BE) system. These functions concerns: the Trigger Primitive Generation (TPG) and the Data Acquisition (DAQ). The new back-end system will also handle the FE control (FE-CTRL) and a high precision clock distribution to the front-end (PH-CLK). The upgraded EB system will increase the sampling frequency from 40 to 160 MHz and the granularity from tower level to crystal level (25 times). In addition, the Back-End system will have to fulfill the phase II trigger requirements such as: a maximum trigger rate of 750 KHz and event pipeline of 500 bunch crossings (BXs), from 100 KHz and 128 BXs respectively.

EB and HB Back-End systems are moving from VME and µTCA, respectively, to the Advanced-TCA (ATCA) standard. The ATCA system offers high backplane bandwidth, increased reliability, more cooling and more power. The processing capabilities of the system are based on state of the art Xilinx UltraScale(+) FPGAs hosted in blades.

On the roadmap to a final prototype hardware platform, the design of the Barrel Calorimeter Processor demonstrator board (BCP demo) is presented. The BCP demo has been designed as a development platform which fulfills all EB and HB functions as well as the trigger requirements. It hosts one KCU115 Kintex UltraScale and provides 56 bidirectional serial links, running any serial protocol that is synchronous or asynchronous to the LHC (~40.08MHz) within the 1 to 16Gb/s data rate range. The target for the BCP demo board is not to have a fully equipped board like the final BCP platform which will host two FPGAs, but instead to have a hardware platform flexible enough to be able to evaluate all EB functions and define the margins. For example the jitter performance will be measured through a high precision clock network from the BCP demo to the FEs.

A System-on-Chip (SoC) in a Xilinx ZYNQ device will be used to control the board. The ZYNQ Processing System (PS) is based on a Dual-core ARM processor running embedded Linux and the Programmable Logic (PL) instantiates the interfaces to control onboard devices (I2C, SPI, AXI-stream, AXI-chip2chip ⋯). ZYNQ offers the AXI protocol and useful tools to control BRAMs and registers in the FPGA, to upload firmware to the FPGA, to debug the design, and to record eye diagrams, all over Ethernet. BCP demo will also support 10Gb Ethernet connectivity useful for standalone DAQ tests like test beams for barrel ECAL (EB) or HCAL (HB). A ZYNQ-based IPMC is chosen for the BCP demo. The ZYNQ approach insures fast response of the IPMC required for board health monitoring.

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