The Phase-I Trigger Readout Electronics Upgrade of the ATLAS Liquid Argon Calorimeters

TWEPP18 – 21 September 2018

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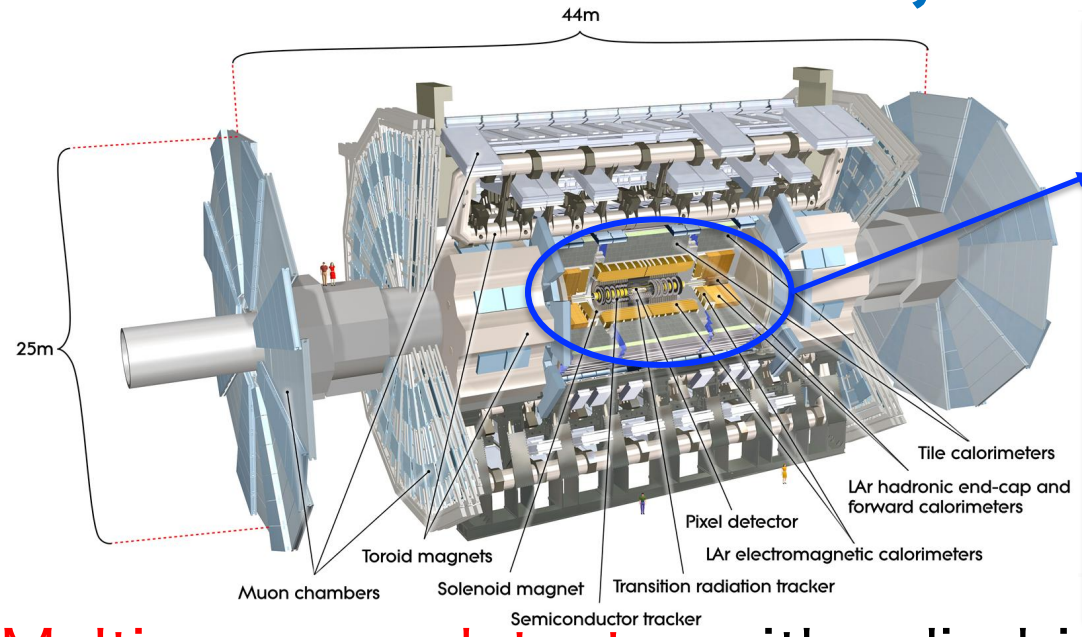
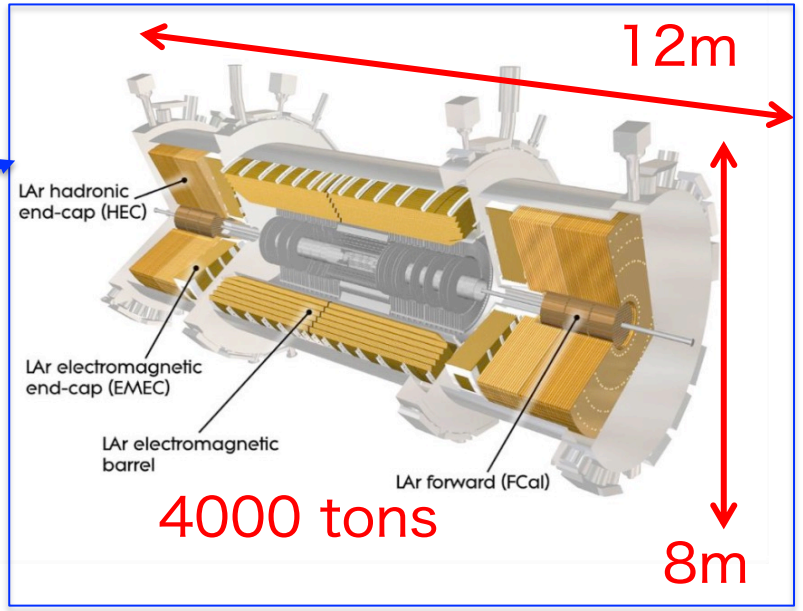
on the behalf of ATLAS Liquid Argon Calorimeter group
The University of Tokyo

ATLAS detector, LAr Calorimeter





Multi-purpose detector with cylindrical geometry

- Study of elementary particles/Search for new physics

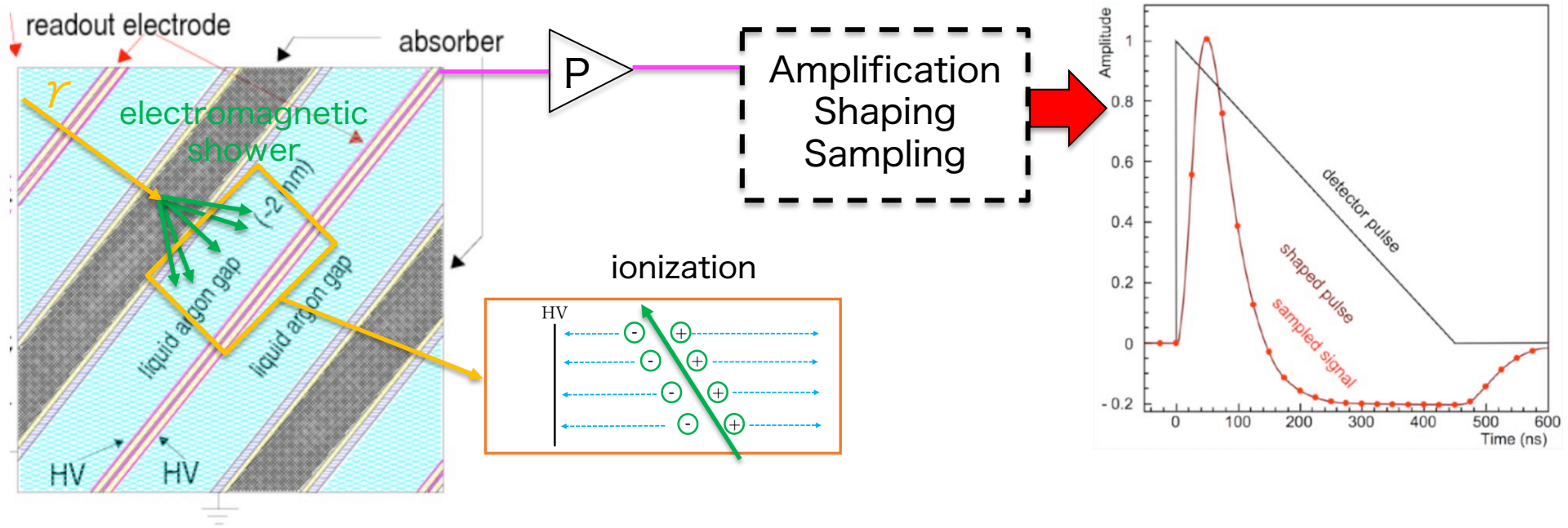
Consists of several sub-detectors

- Pixel, Silicon-Strip, calorimeter, Muon chambers

Liquid Argon (LAr) Calorimeter: for electron and photon

- Measures energy, position and shower shapes
- Lead (Pb) - LAr sampling calorimeter with accordion shape
- 4 different layers (Layer0 - Layer3), total 180k cells.
  - Fine granularity: Eg. $\Delta\eta \times \Delta\phi = 0.025 \times 0.025$ for Layer2

Liquid ionization pulse



- Incoming particle creates a electromagnetic shower in Pb.
- Electrons in shower ionize liquid argon
- Ionization creates a triangle current pulse on electrode.
- Triangle current pulse is amplified and shaped: $(CR - (RC)^2)$
  - Bipolar pulse with ~ 600 ns duration
  - Peaking time is about 45 ns

Current LAr readout electronics

There are two readout path : Main/Trigger readout

Main readout

Frontend

- Amplification and shaping of cells.
- Buffering with analog pipeline
- Digitization on Level1 trigger accept
- Data transmission via optical link

Backend

- Compute transverse energy and time

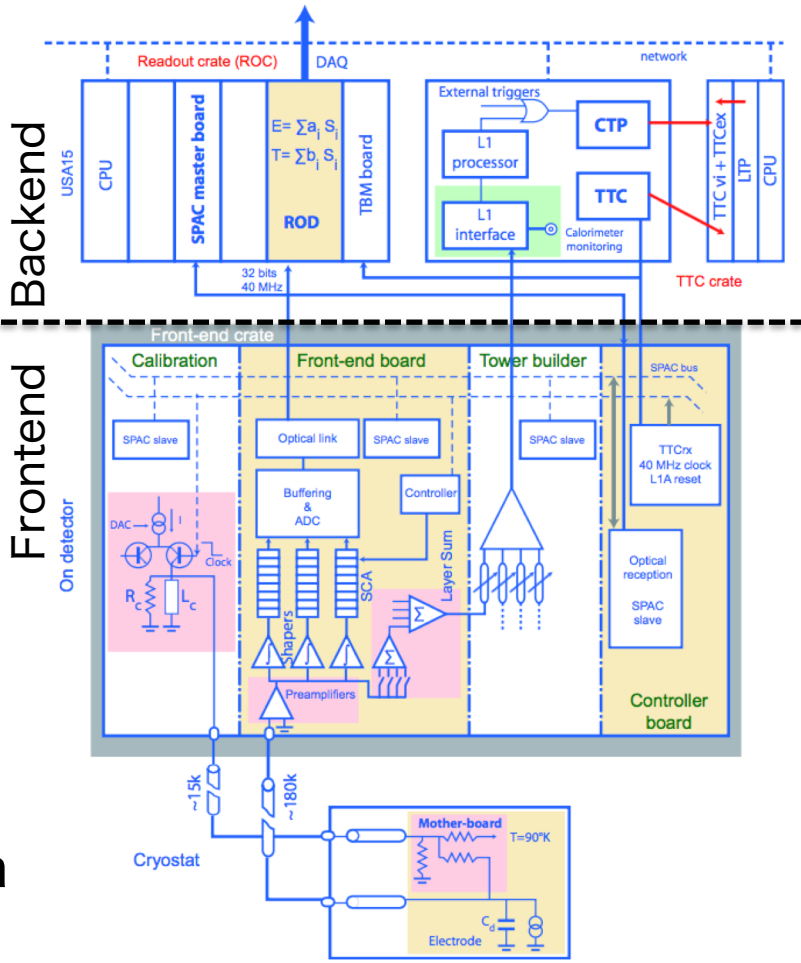
Trigger readout

Frontend

- Sums cell energies per layer
- Forms trigger readout signals
- Sends them (analog) to Level1 system

Backend

- Sampling and digitization at 40 MHz
- Compute transverse energy and time



Trigger path

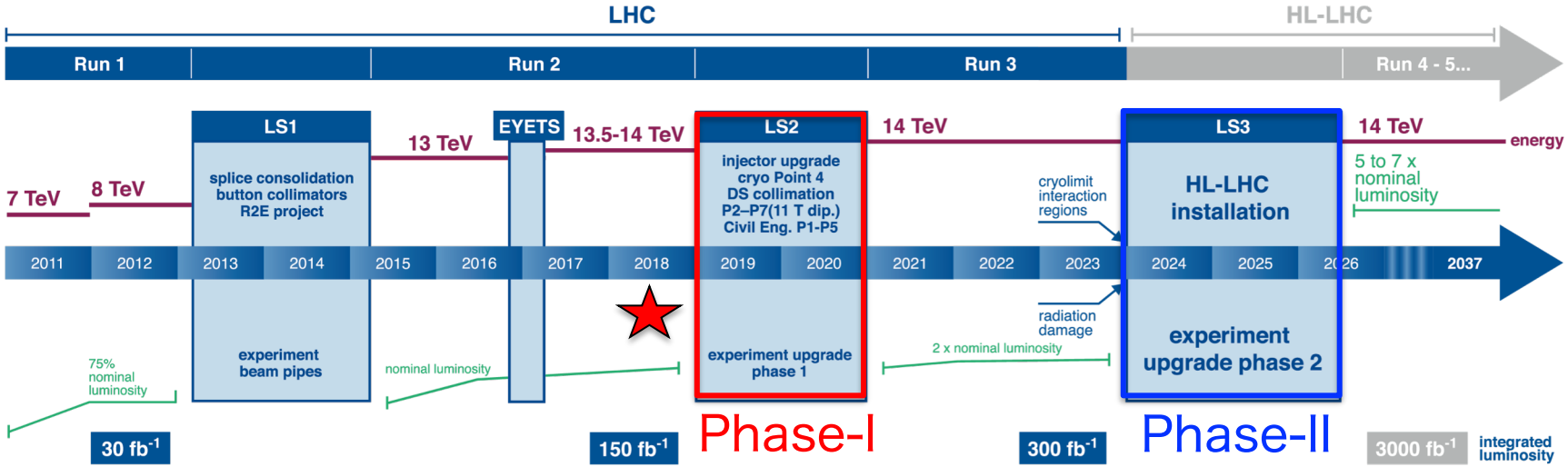
Data reduction is mandatory to perform low-latency

→ hardware-based

Upgrade schedule

Run2 : L_{max} 1.8 x 10^{34} cm^{-2} s^{-1}
Run3 : L_{max} 3.0 x 10^{34} cm^{-2} s^{-1}
Run4 : L_{max} 7.0 x 10^{34} cm^{-2} s^{-1}

LHC / HL-LHC Plan



ATLAS LAr calorimeter upgrade:

- Phase-I upgrade
  - Main role : **Trigger readout upgrade**
  - Level1 Trigger : 100 kHz, latency 2.5 μs
- Phase-II upgrade
  - Main role : **Main readout upgrade**
  - Level1 Trigger : 1 MHz, latency 10 - 20 μs

ATLAS LAr Phase-I upgrade

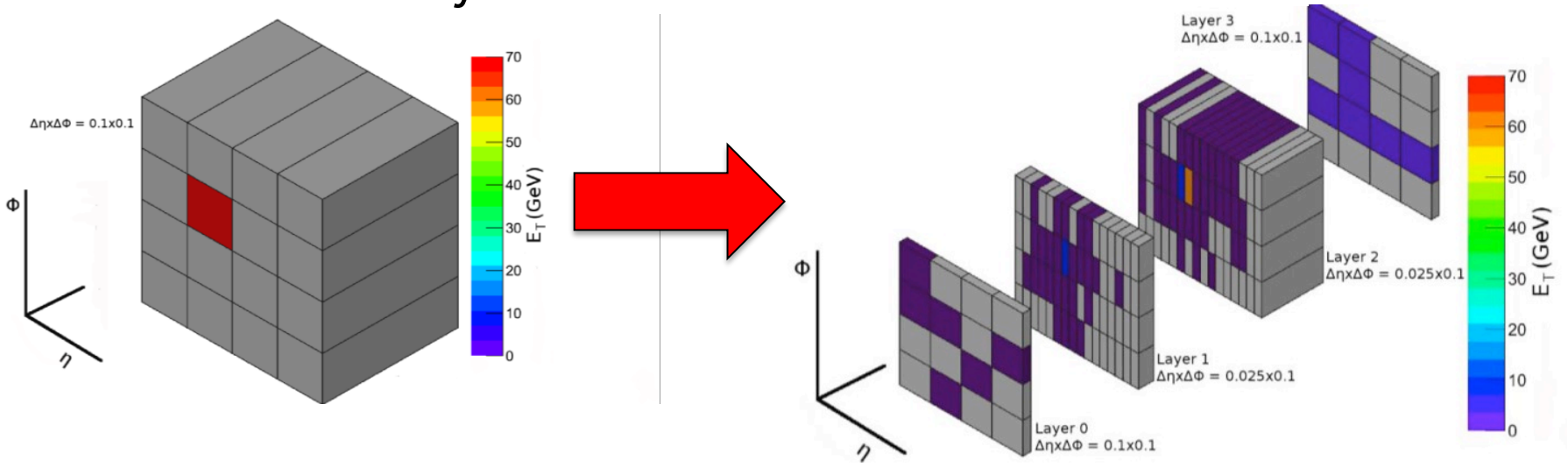
Situation: Inject electron with 70 GeV energy

Current Trigger readout

- $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$
- Sums cells of all layers.

New Trigger readout

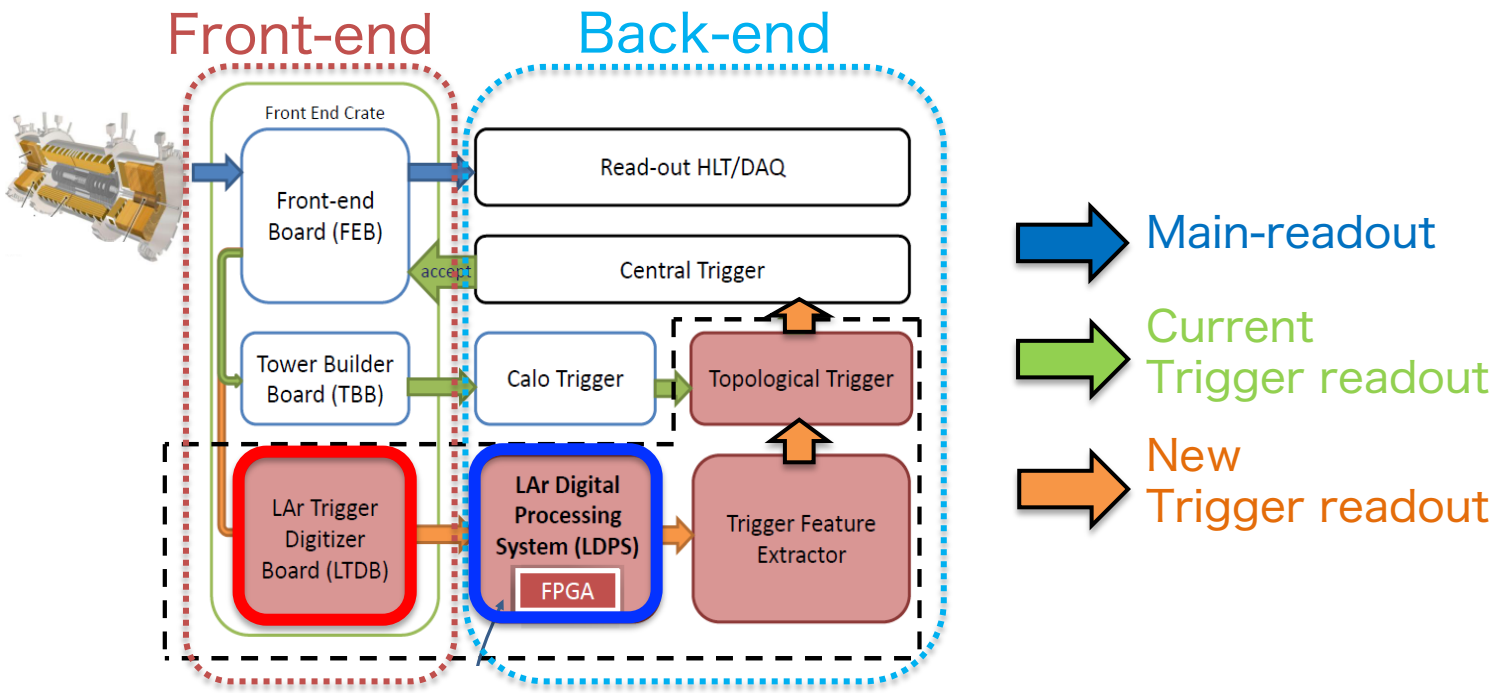
- $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$ (Layer0,3)
- $\Delta\eta \times \Delta\phi = 0.025 \times 0.025$ (Layer1,2)



New Trigger readout : Super Cells

- Sends 4 layer info + finer segmentation in η direction
  → 10 times finer granularity : challenging!
- Better background rejection (Eg. $\pi^{\pm}$)

New hardware for Phase-I



Introduce two hardware for Run3 experiment

LAr Trigger Digitizer Board (LTDB)

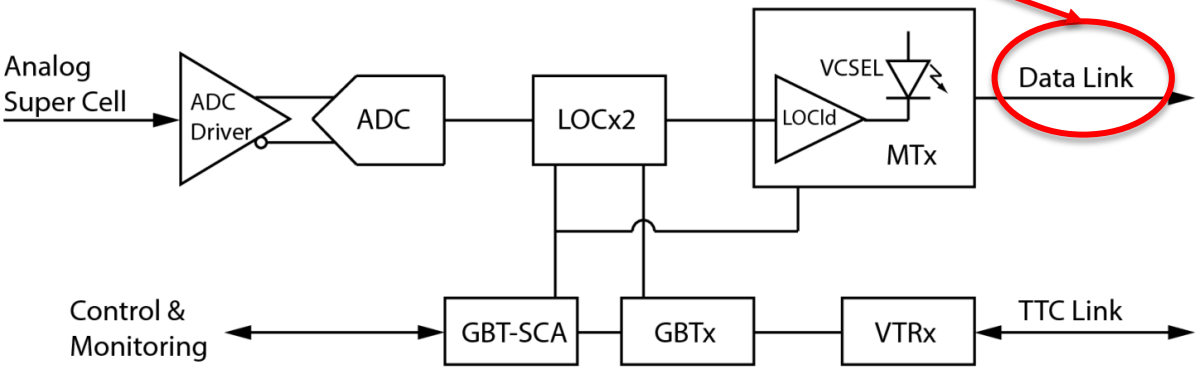
- Digitize Super Cell information on 12 bits at 40 MHz
- Transmit ADC data to Backend : total ~25 Tbps

LAr Digital Processing Board (LDPB)

- Compute transverse energy (E_T) and time with Super Cells at 40 MHz
- Transmit to Level1 system : total ~51 Tbps, 375 ns latency

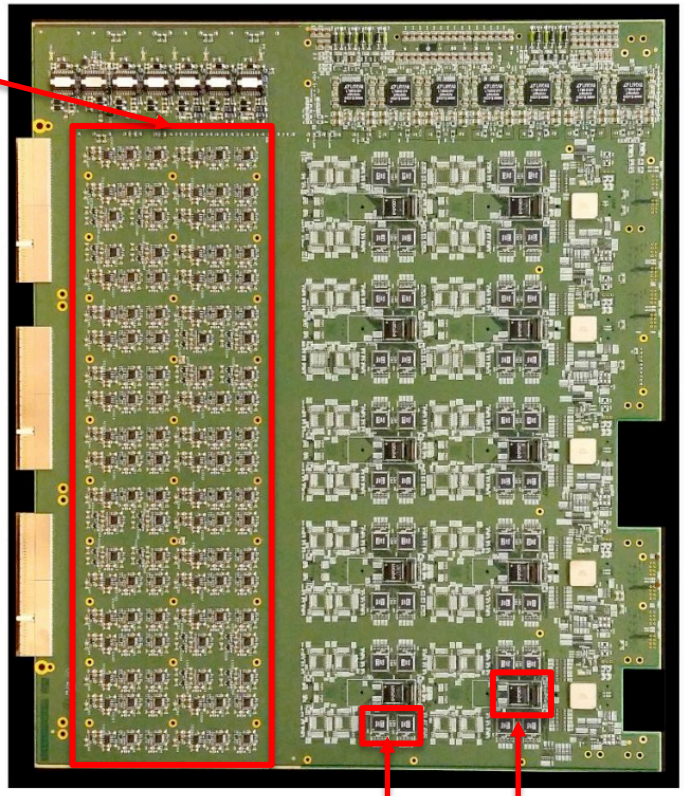
Frontend Upgrade : LAr Triger Digitizer Board (LTDB)

LTDB



320-ch analog circuit

40 fibers @ 5.12 Gbps



Specs:

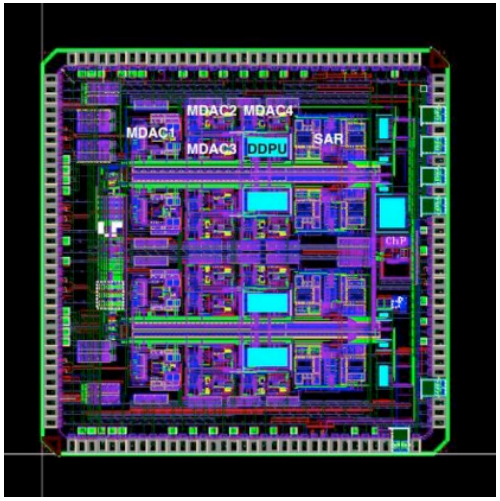
- 124 LTDBs : 320 Super Cells per board
- 24 layers PCB with 2.23 mm thickness
- Custom radiation tolerant ASICs (ADC, LOCx2(serializer))
- Latency < 275 ns
- GBT-SCA ASICs used as control interface to ADCs.
- GBT links used for LHC clock and Trigger information

Reference : Timing, Trigger Control (TTC) info, GBTX chip

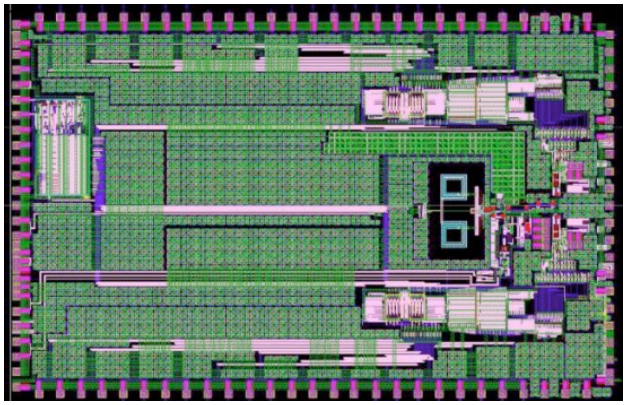
→ Some tests are ongoing for mass production

Custom-made ASICs

NevisADC
3.6x3.6 mm
72 pins QFN



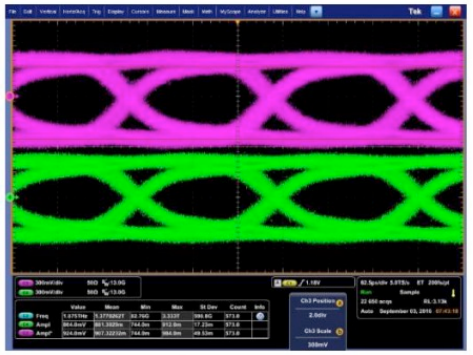
LOCx2: 6.036x3.68 mm, 100 pins QFN



4 channel 12 bit radiation-hard ADC : NevisADC

- IBM8RF 130 nm CMOS
- ENOB: 11 bits, Dynamic range: 11.7 bits
- Power < 50 mW/channel, Latency ~ 100 ns

→ Radiation tolerance established up to 10 Mrad!



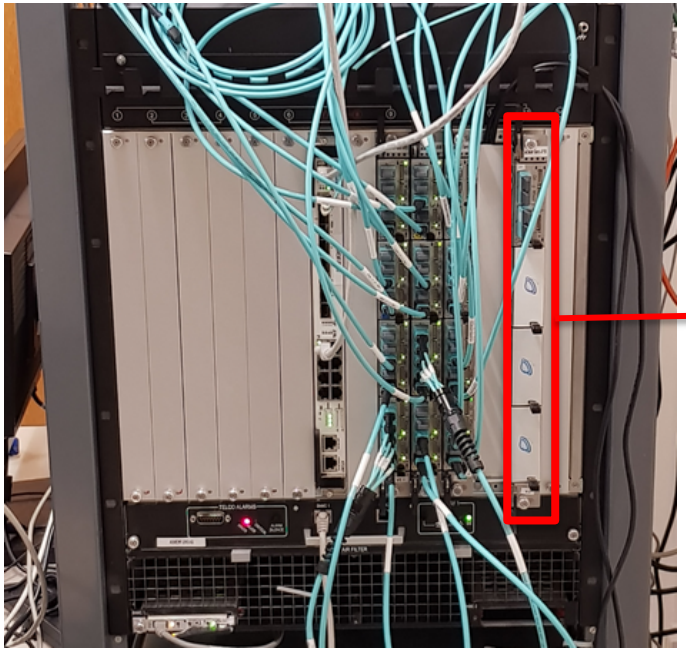
Serializer: LOCx2

- Dual channel 8x14 bits, 250 nm Silicon-on-Sapphire
- 5.12 Gbps transmission speed
- Fixed latency < 75 ns
- No change in output eye diagram after 200 krad

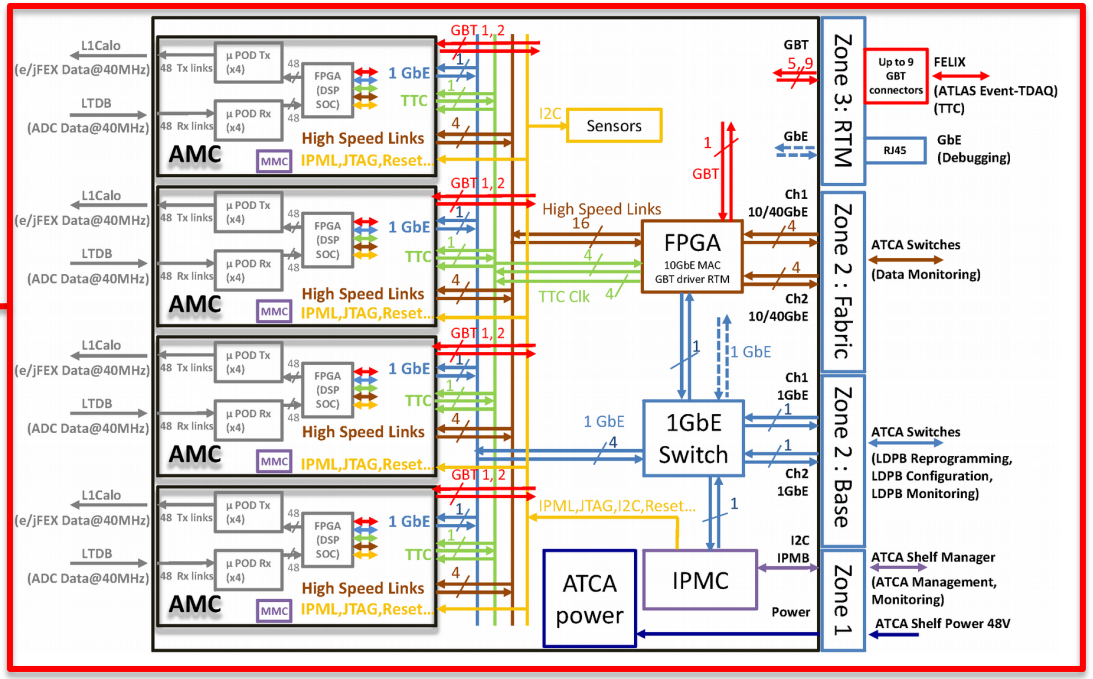
Backend Upgrade : LAr Digitizer Processing Board (LDPB)

The overview of LDPB

ATCA



LAr Digital Processing Board (LDPB)



ATCA standard board : In total 31 LDPB is used

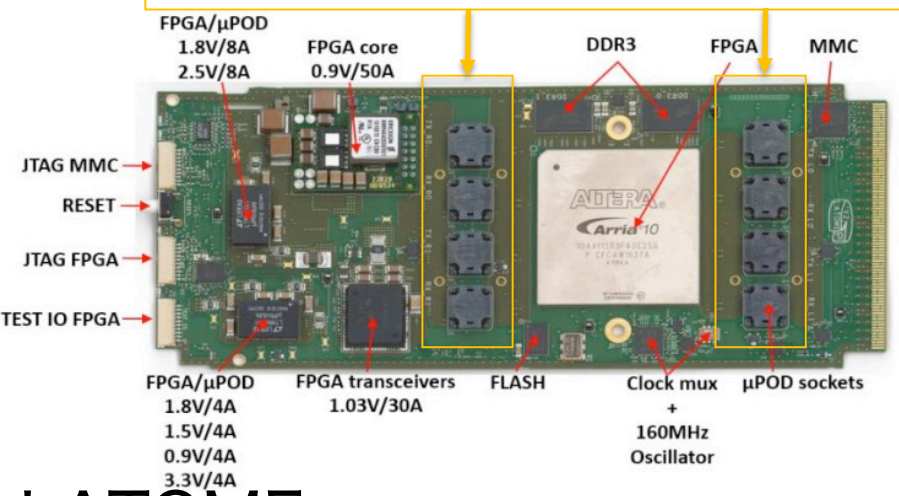
- Consists of 1 Carrier board and 4 AMC

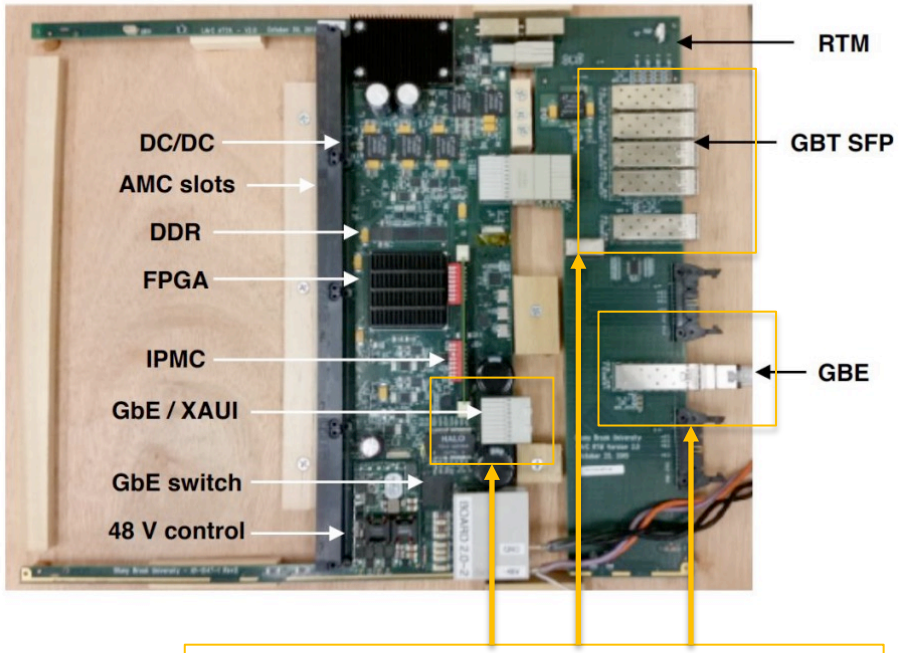
AMC is the main of trigger path : Performs Digital processing

- Receive 5.12 Gbps (×48 fibers) info per 1 AMC from Frontend
- Compute transverse energy and time of Super Cells at 40 MHz
- Transmit 11.2 Gbps (×48 fibers) info per 1 AMC to L1 system

AMC (LATOME), Carrier (LArC)

Input 48 fibers(5.12Gbps)
Output 48 fibers (11.2 Gbps)
- 8 microPOD^{TSM} : AFBR-77D4SZ





10 GBbps link via ATCA fabric
5 GBT links via RTM
1 Gbps links via RTM
(slow control)

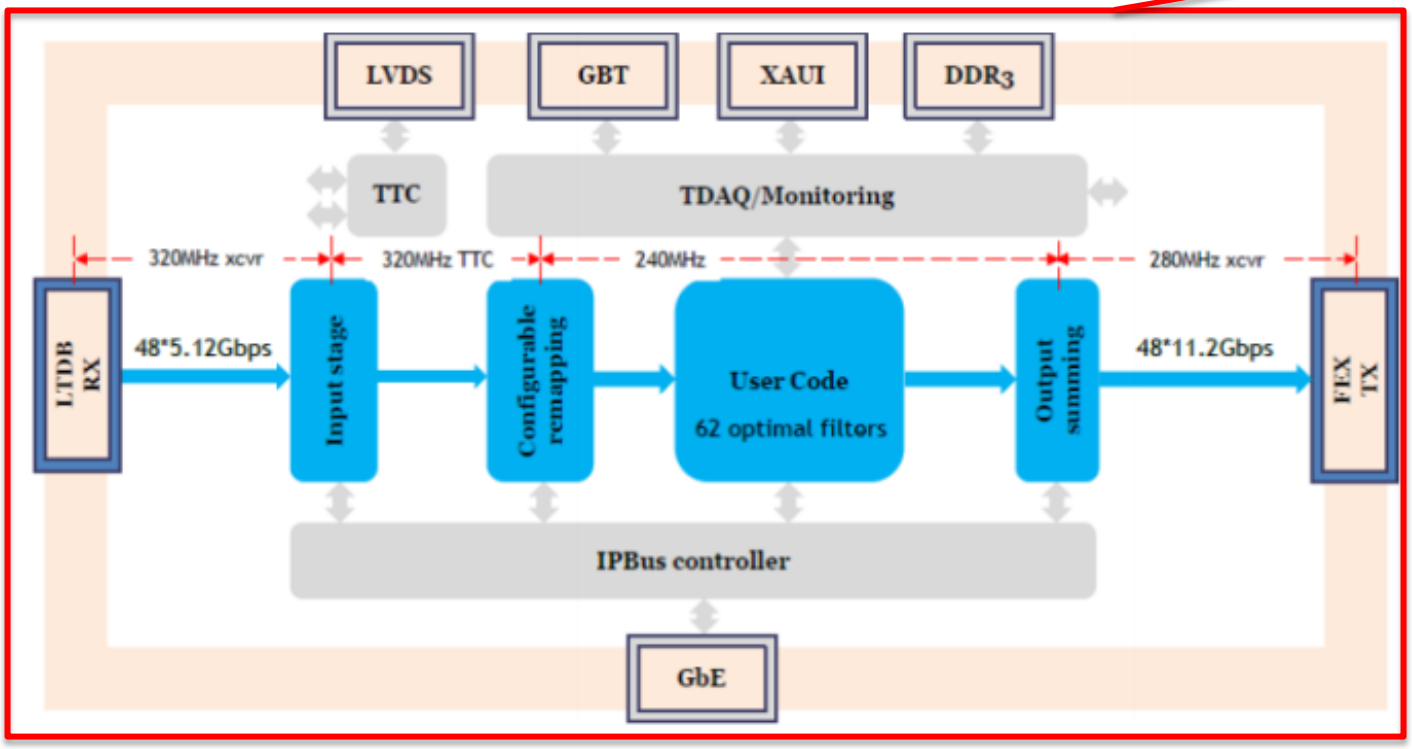
LATOME:

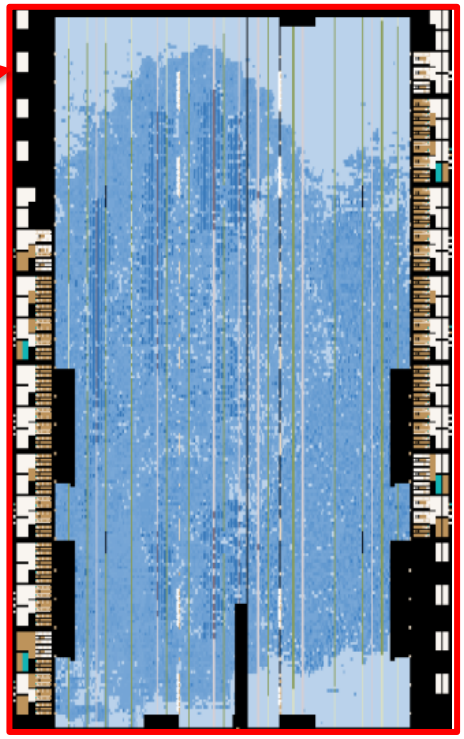
- 16 layer PCB with 1.6 mm thickness
- Power consumption: up to 80 W
- Use Intel Arria10 FPGA : 10AX115R3F40E2SG

LArC:

- 22 layer PCB with 2.4 mm thickness
- Power consumption: ~ 400 W
- Use Xilinx Virtex7 FPGA : VC7VX485TFFG1927-2

LATOME Firmware





Several function blocks : Drive by 240, 280, 320 MHz

- Receive 48 data streams (1 data streams = 1 fiber data)
- Remap channels (48 → 62 data streams, 320 MHz → 240 MHz)
- Compute the transverse energy and time of Super Cells
- Energy summing ($\Delta\eta \times \Delta\phi$ =0.1×0.1 and 0.2×0.2)
- Transmit 48 data streams

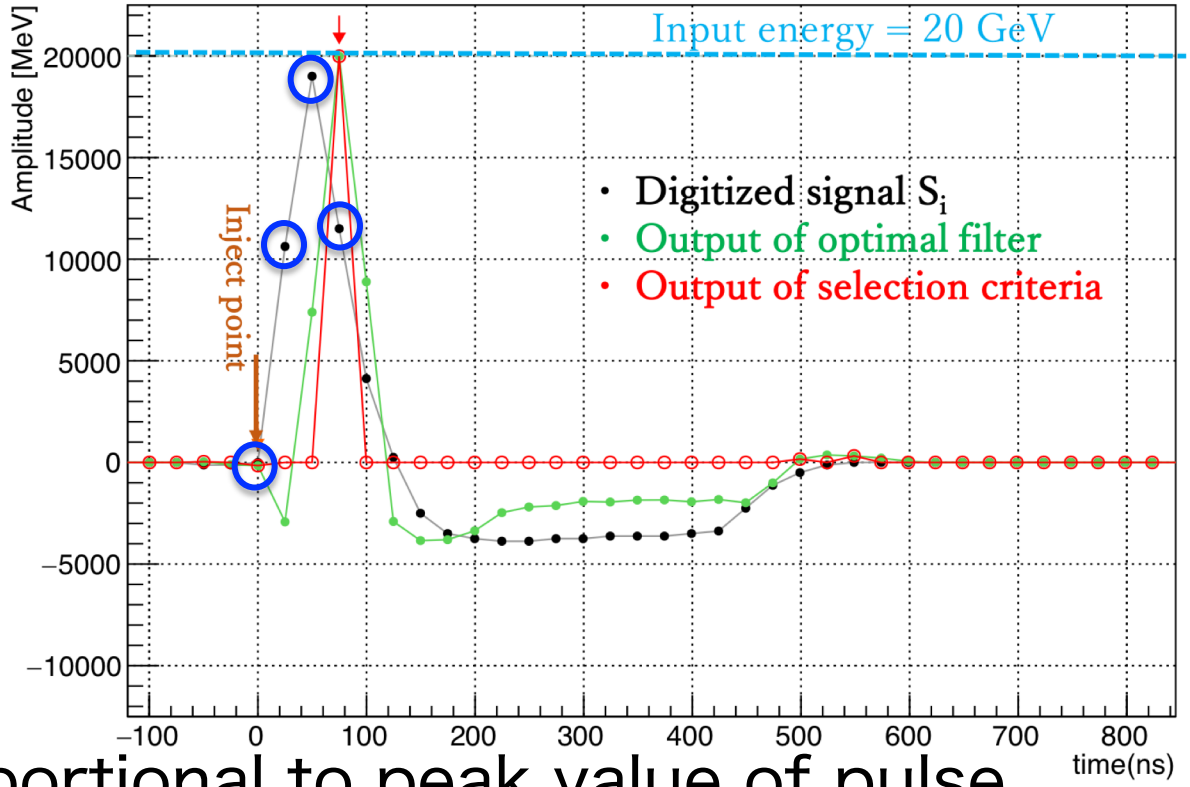
Energy reconstruction

$$E_T = \sum_{i=1}^{4} a_i (S_i - P)$$

$$E_T\,\tau = \sum_{i=1}^{4} b_i (S_i - P)$$

P: Pedestal

τ : relative phase



The energy is proportional to peak value of pulse.

- The peak is around 3rd sampling point

FIR Filter: Optimal filter

- Coefficients are optimized to minimize noise by calibration data

Selection Criteria: Eg. $|\tau| < 2$ ns ($E_T > 10$ GeV)

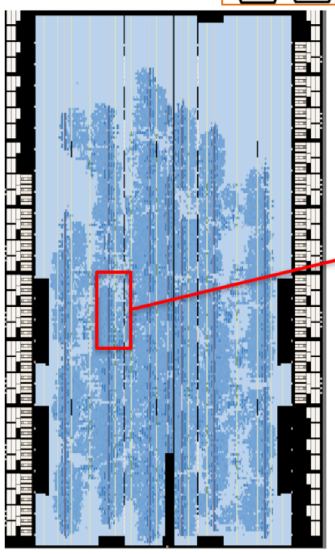
- One energy at the correct time can be output for one pulse.

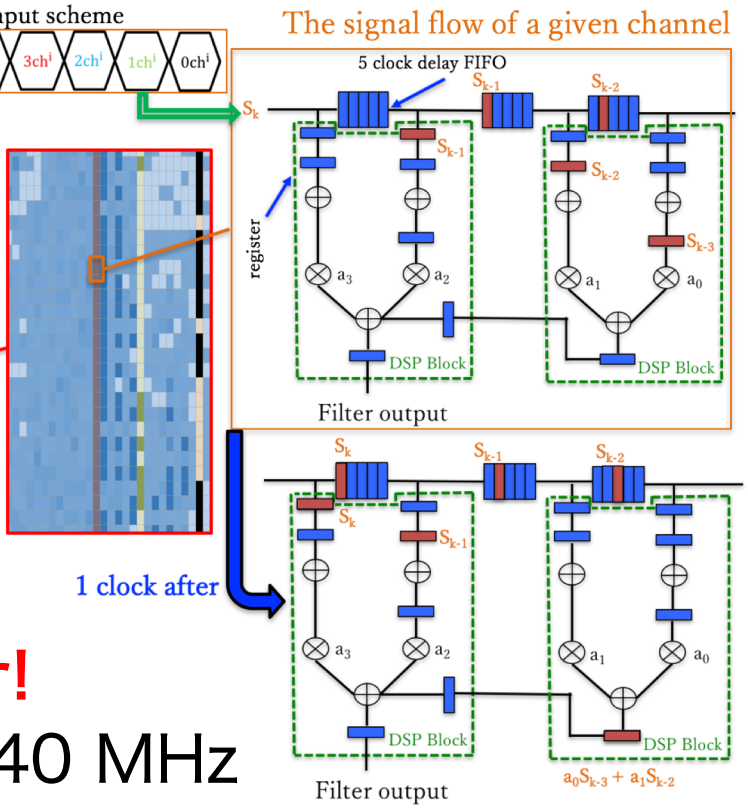
Energy reconstruction firmware

$$E_T = \sum_{i=1}^{4} a_i (S_i - P)$$

$$E_T\,\tau = \sum_{i=1}^{4} b_i (S_i - P)$$

Map of component in Arria10 FPGA





Implemented multi-stage FIR Filter!

Energy reconstruction is done at 240 MHz

- Serialize 6 Super Cells (40 MHz x 6)
- 62 parallel processing

Latency : 4.5 BC

F_{max} ~ 260 MHz

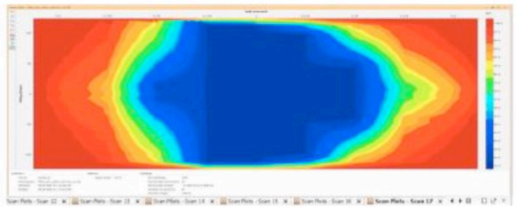
Firmware features

- Cascade connections of DSP Block
  - Minimized the wiring delay
  - Realized all calculations in DSP Block

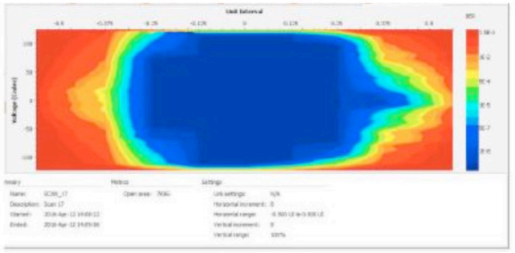
Confirm it is working on hardware!

Performance test

Data transmission

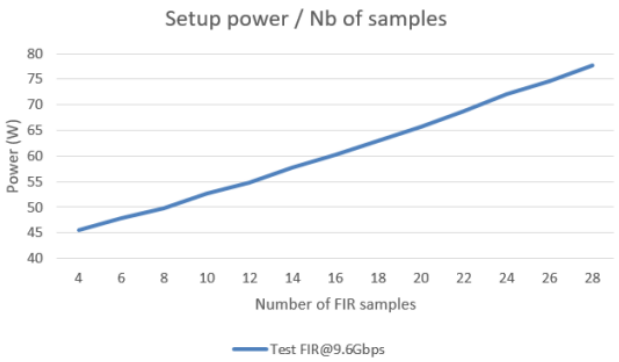


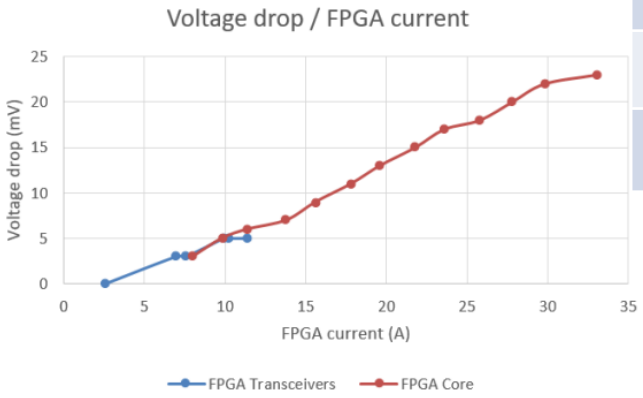
To gFEX



To eFEX

Power consumption





Latency (BC=25 ns)

Block	Spec	Meas
Interface	2	2
Input stage	3	2.63
Remapping	1.5	1.75
Energy calc	5	4.5
Summing	1.5	2.5
Interface	2	2
Total	15	15.38

Confirmed a fixed latency!

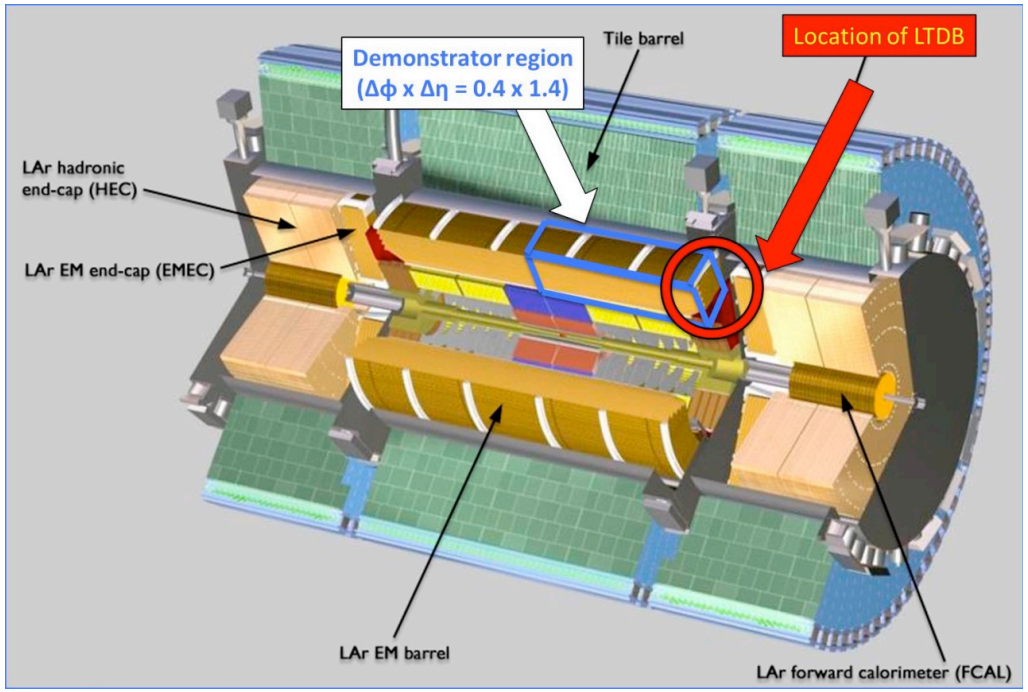
All 48 Rx/Tx:
BER ($<10^{-14}$)@11.2 Gbps

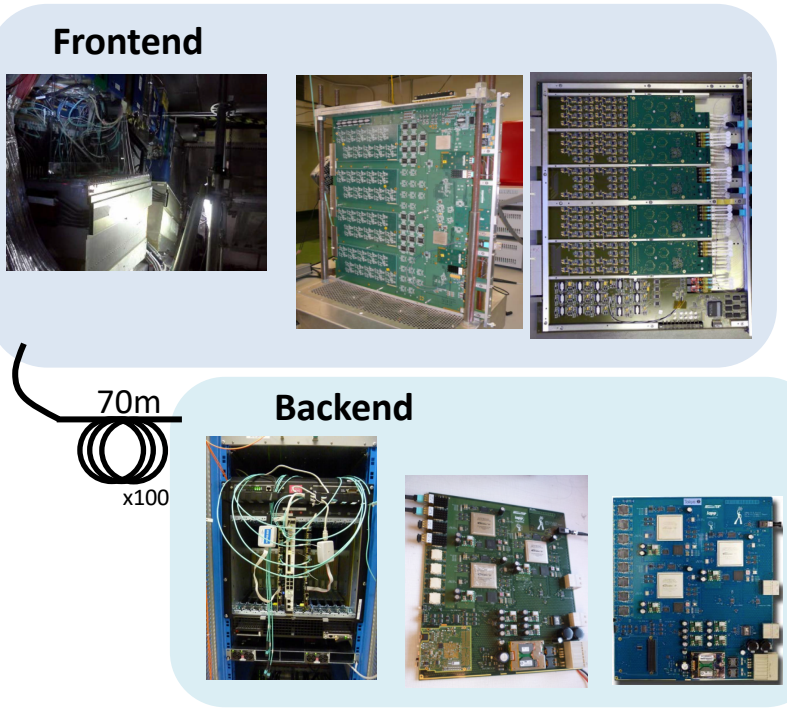
Confirmed LATOME operation with full load on FPGA.

All requirement: OK
Started production!

Demonstrator project

LAr Phase-I Demonstrator





Demonstrators are in ATLAS since 2014 Aug.

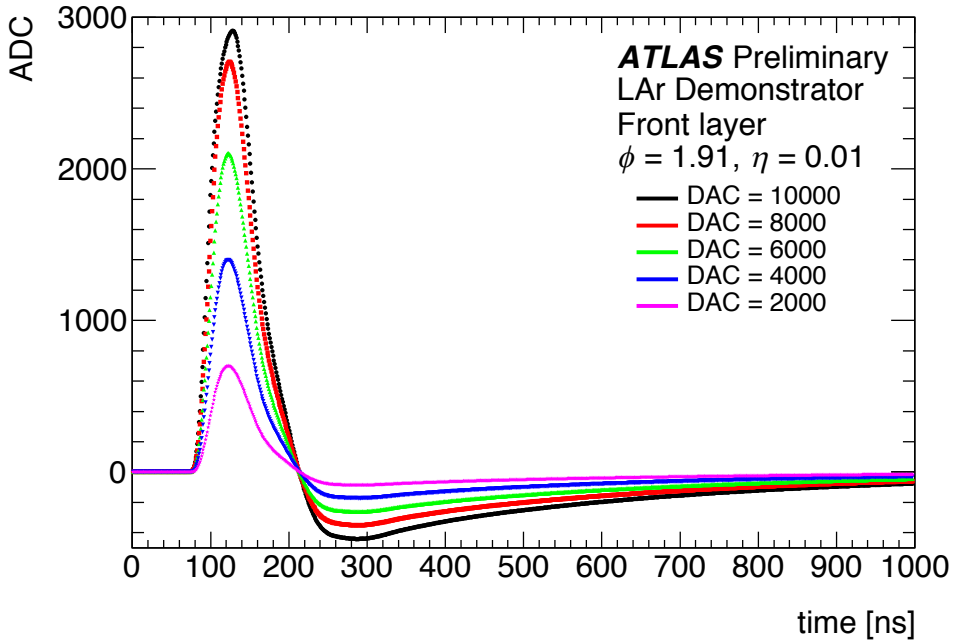
- Different from production board:
  - Eg. No radiation hardness Frontend ADC, FPGA

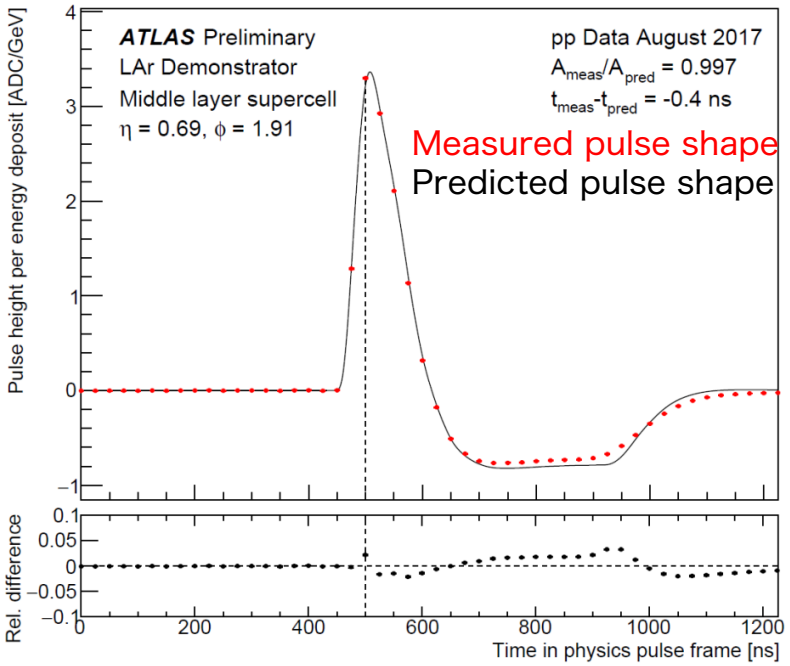
Purpose

- Take a collision data in Run2
- Check installation procedure, system stability

Replaced the demonstrator into two pre-production board in 2018

Demonstrator calibration





Inject a calibration pulse with different amplitude (DAC)

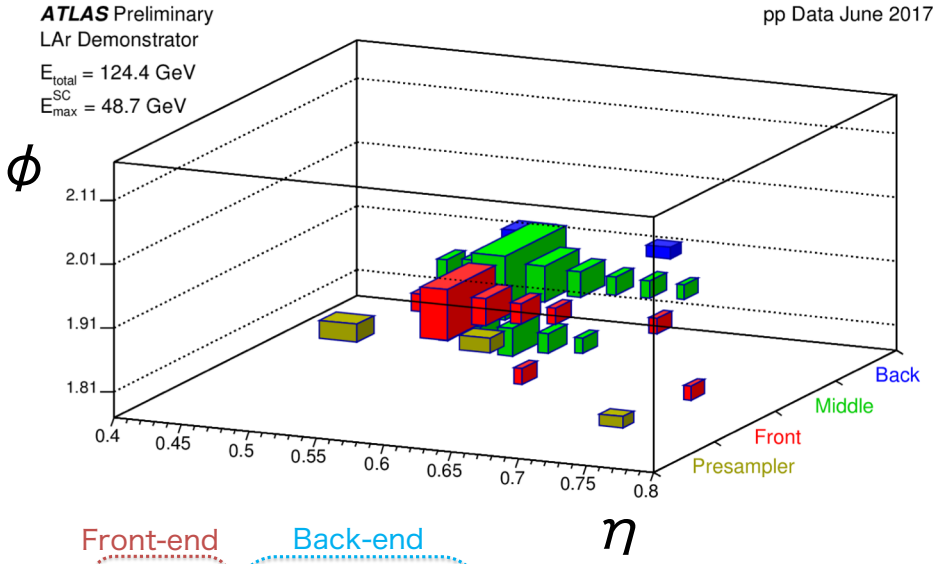
- Established calibration method for Super Cells.
- Good linearity is observed

Estimated the physics pulse from calibration pulse

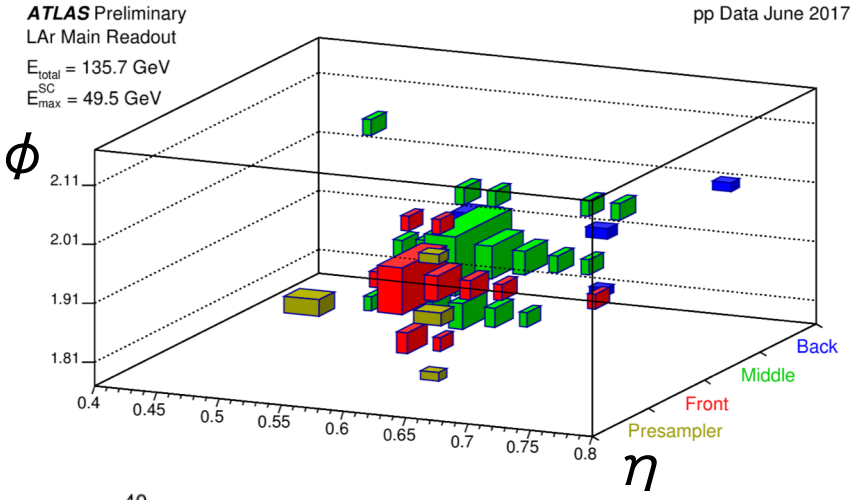
- Compared to collision data : Good matching is observed

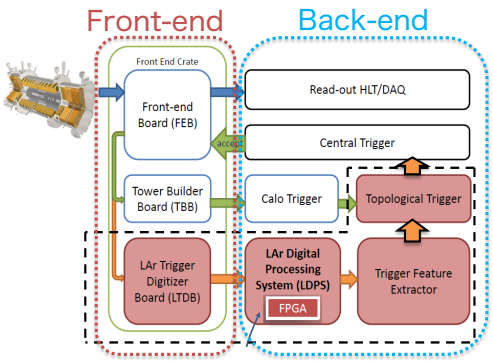
Collision data with demonstrator

Demonstrator



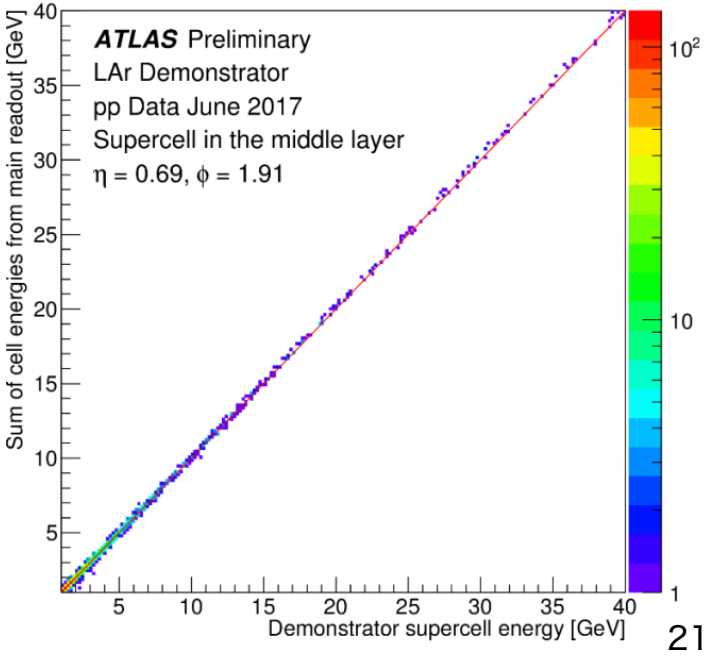
Main readout





Main-readout

Demonstrator



Comparison with Main readout

- Good match on cluster level
- Good linearity is observed

Summary and Prospect

ATLAS LAr Calorimeter Phase-I upgrade

- The electronics will be upgraded to increase readout granularity and precision
  - Keep trigger rates (still low single items thresholds) under Run3 environment

Frontend and Backend system are developed

- Radiation tolerant custom ASICs are produced for Frontend
- High-end FPGAs are used for Backend
- Production is already started.

Take data using demonstrator system in Run2

- Compatibility test with Main readout is done.
- Replaced with pre-production board in 2018 Jan
  - Complete functionality of the FE+BE system under test.
  - The data analysis taken from this board is on-going.

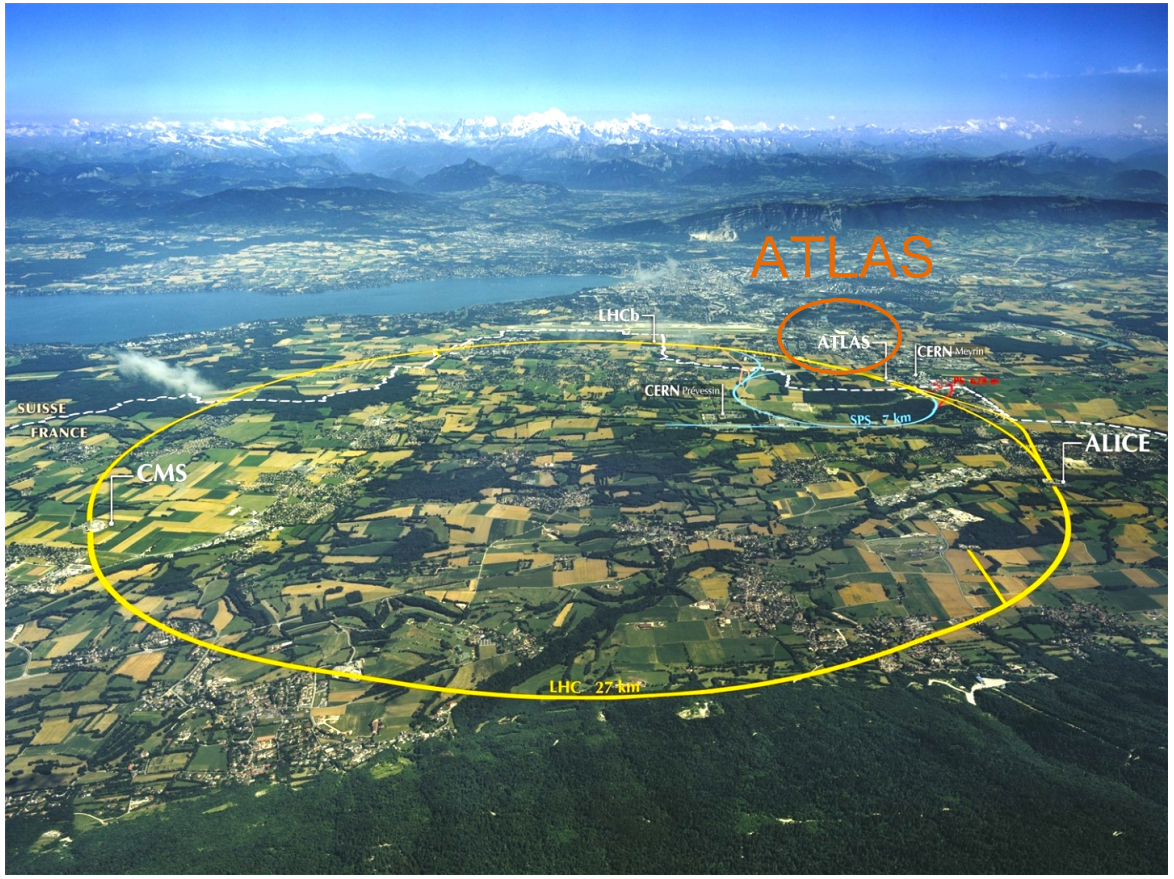
Back up

Outline

- Introduction
  - ATLAS detector
  - Liquid ionization pulse
  - Phase-I upgrade

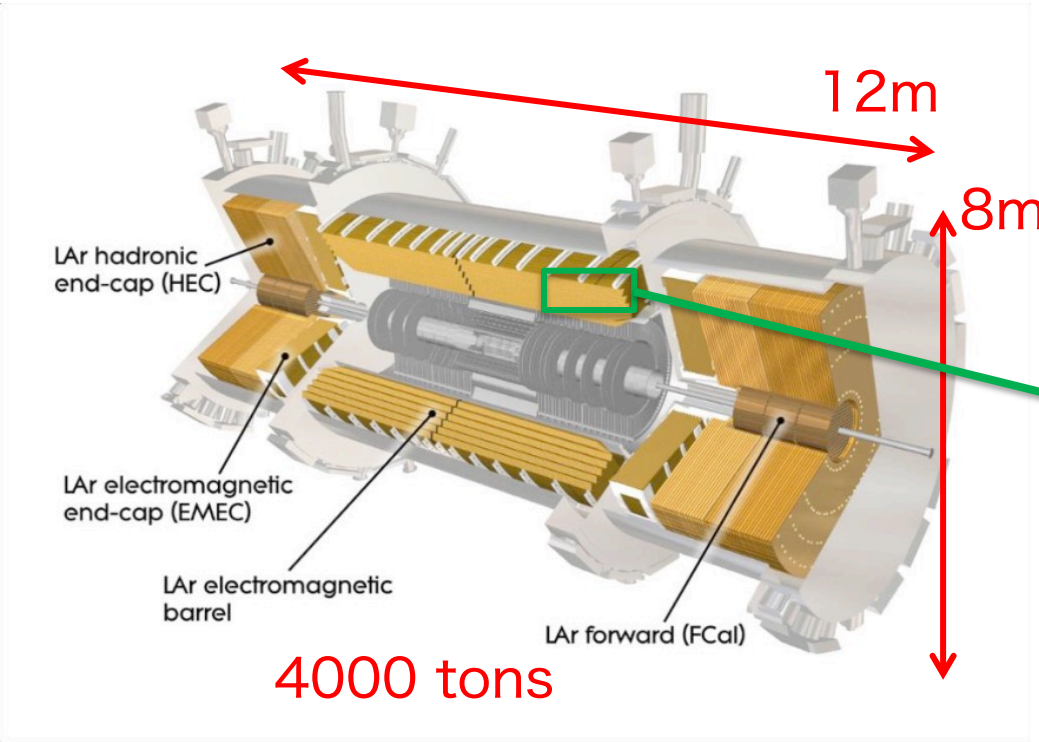
- LAr Frontend electronics upgrade
- LAr Backend electronics upgrade
- Demonstrator project

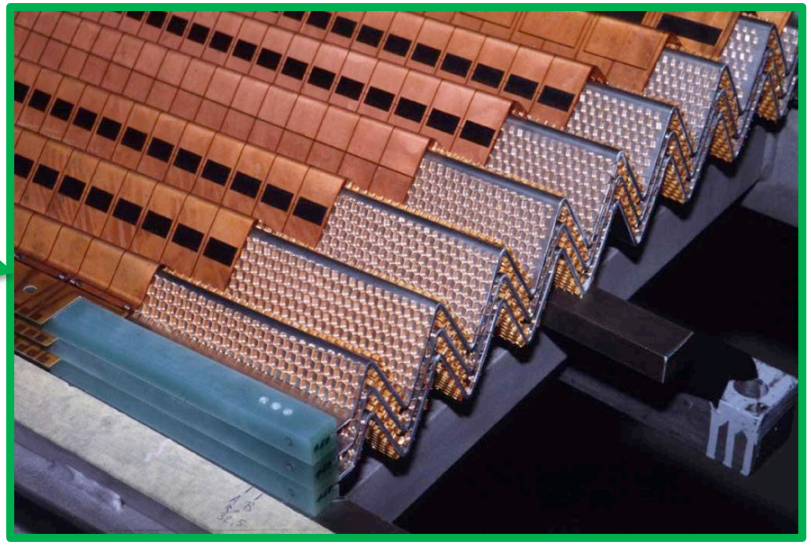
Large Hadron Collider



- Proton-proton circular collider (13 TeV, 40 MHz)
- 27 km circumference
- There are 4 main detectors
  - ATLAS, CMS, ALICE, LHCb

ATLAS Liquid Argon Calorimeter

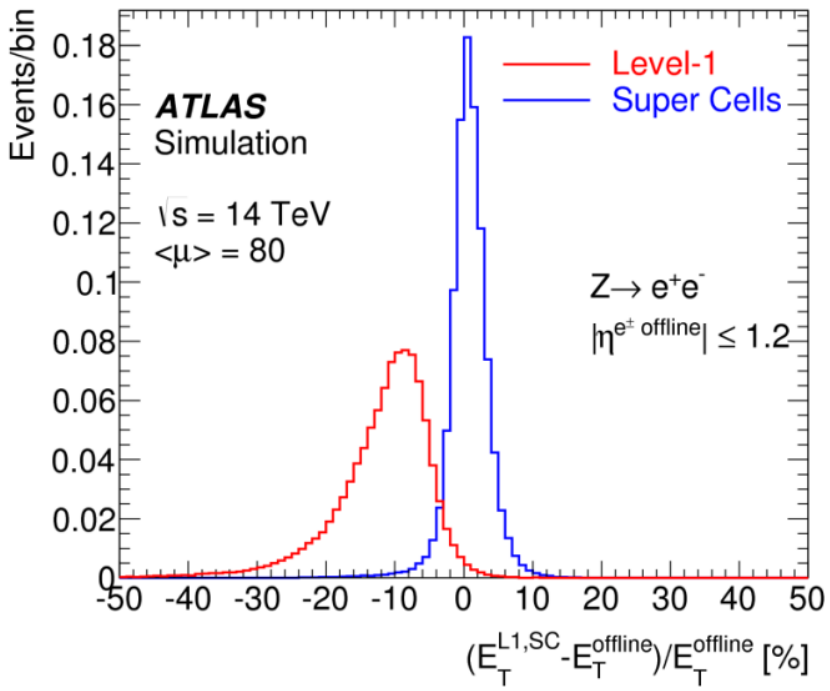


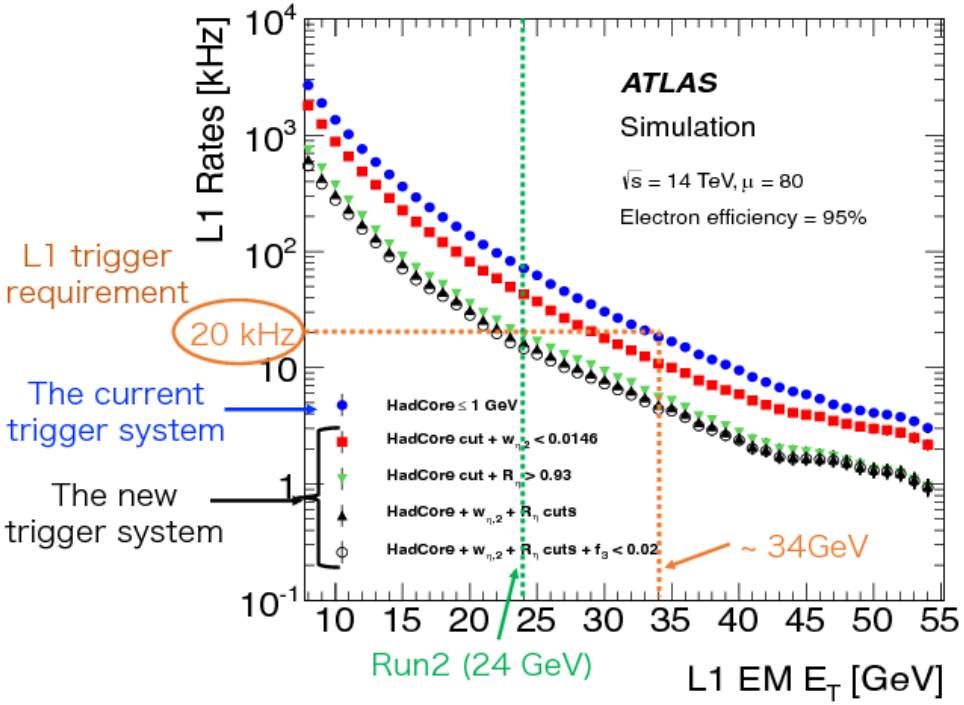


Measure energy and position of electron and photon

- Pb - LAr sampling calorimeter with accordion shape
- 4 different layers (Layer0 - Layer3), total 180k cells.
  - Fine granularity: $\Delta\eta \times \Delta\phi = 0.025 \times 0.025$ for Layer2
- $\sigma/E \sim 10\ \%/\sqrt{E} \oplus 0.7\%$

Expected performance





~ 34 GeV E_T threshold without Phase-I upgrade

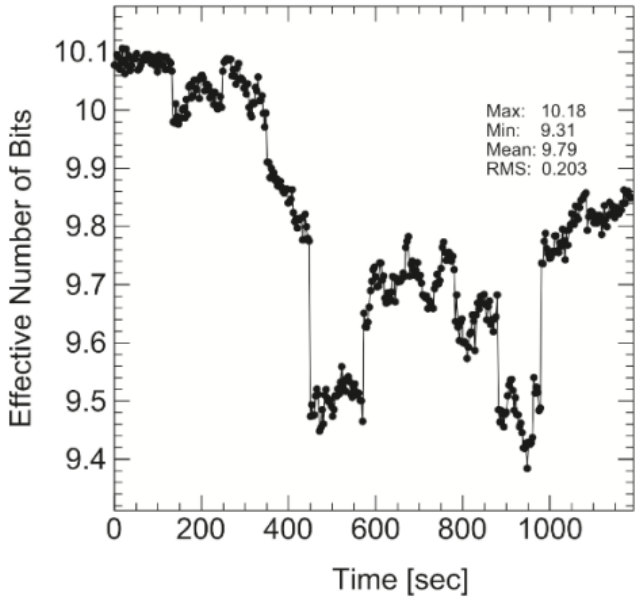
- W→eν, Z→ee, H→$\gamma\gamma$: Trigger on EM object with 20 - 30 GeV
  → May lost these efficiencies : it is a problem for physics side!

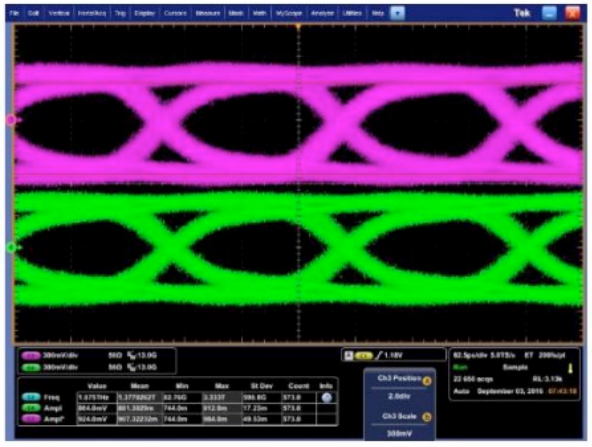
Obtain a better performance after Phase-I upgrade

- The threshold in Run3 can be almost same as Run2.

Radiation tolerance on ASICs

- HL-LHC requirement
  - 100 kRad of total dose and SEE tests with total fluency of 3.8 x 10^{12} h/cm^2.
- Quad channel ADC: Nevis-15
  - Radiation tolerance established up to 10 MRad
  - See cross section as 10^{-12} cm^2 per channel
- Serializer(LOCx2) and Laser driver(LOCld)
  - No change in the output eye diagram has been observed after ~ 200 kRad TID.





Optimal filter principle 1

The digitized signal is described under the following formula.

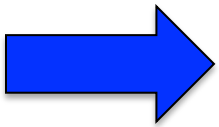
$$\begin{aligned} S_i &= Ag(t_i - \tau) \\ &\cong Ag(t_i) - A\tau \frac{dg(t)}{dt}|_{t=t_i} + n_i \\ &= Ag(t_i) - A\tau \dot{g}(t_i) + n_i \end{aligned}$$

S_i : Digitized signal
A : Pulse height
g : Normalized ideal pulse
n_i : noise term

Define the following two values, then calculated the mean.

$$u = \sum_{i=0}^{N-1} a_i S_i$$

$$v = \sum_{i=0}^{N-1} b_i S_i$$



$$< u > = \sum_{i=0}^{N-1} \{A < a_i g(t_i) > - A\tau < a_i \dot{g}(t_i) > + < a_i n_i >\}$$

$$< v > = \sum_{i=0}^{N-1} \{A < b_i g(t_i) > - A\tau < b_i \dot{g}(t_i) > + < b_i n_i >\}$$

$$< u > = A \sum_{i=0}^{N-1} a_i g(t_i) - A\tau \sum_{i=0}^{N-1} a_i \dot{g}(t_i)$$

$$< v > = A \sum_{i=0}^{N-1} b_i g(t_i) - A\tau \sum_{i=0}^{N-1} b_i \dot{g}(t_i)$$

Optimal filter principle 2

If <u> = A, <v> = A τ , we can get the following condition.

$$\sum_{i=0}^{N-1} a_i g(t_i) = 1$$
$$\sum_{i=0}^{N-1} a_i \dot{g}(t_i) = 0$$
$$\sum_{i=0}^{N-1} b_i g(t_i) = 0$$
$$\sum_{i=0}^{N-1} b_i \dot{g}(t_i) = -1$$

Then, we calculate the variance of u, v.

$$Var(u) = < u^2 > - < u >^2 = \sum_{i=0}^{N-1}\sum_{j=0}^{N-1} a_i a_j < n_i n_j > = \sum_{i=0}^{N-1}\sum_{j=0}^{N-1} R_{ij}$$
$$Var(v) = \sum_{i=0}^{N-1}\sum_{j=0}^{N-1} b_i b_j < n_i n_j > = \sum_{i=0}^{N-1}\sum_{j=0}^{N-1} b_i b_j R_{ij}$$

Finally, the coefficient is determined to minimize the noise.

$$\sum_{j=0}^{N-1} R_{ij} a_j = \lambda g(t_i) - \kappa \dot{g}(t_i)$$
$$\sum_{j=0}^{N-1} R_{ij} b_j = \mu g(t_i) - \rho \dot{g}(t_i)$$