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The Phase-I Trigger Readout Electronics Upgrade of the ATLAS Liquid Argon Calorimeters

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Electronics developments are pursued for the trigger readout of the ATLAS Liquid-Argon Calorimeter towards the Phase-I upgrade scheduled in the LHC shut-down period of 2019-2020. The LAr Trigger Digitizer system will digitize 34000 channels at a 40 MHz sampling with 12 bit precision after the bipolar shaper at the front-end system, and transmit to the LAr Digital Processing system in the back-end to extract the transverse energies. Results of ASIC developments including QA and radiation hardness evaluations, performances of the final prototypes and results of the system integration tests will presented along with the overall system design.

Summary

The upgrade of the Large Hadron Collider (LHC) scheduled for a shut-down period in years 2019-2020, referred to as the Phase-I upgrade, will increase the instantaneous luminosity to about three times the design value. Since the current ATLAS trigger system does not allow for sufficient increase of the trigger rate, without an important loss of interesting physics, an improvement of the trigger system is required. The Liquid Argon (LAr) Calorimeter read-out will therefore be modified to use digital trigger signals with higher spatial granularity and higher precision in order to improve the identification efficiencies of electrons, photons, tau, jets and missing energy, at high background rejection rates already at the Level-1 trigger. The new trigger signals will be arranged in 34000 so-called Super Cells which achieve increased precision and 5-10 times better granularity than the trigger towers currently used and allow an improved background rejection.

The LAr trigger system will digitise the signals of the Super Cells at the front-end, close to the cryostat feedthrough outputs, at every LHC bunch-crossing with 12-bit precision at 40 MHz frequency. The data will be transmitted to the back-end on 5.12 Gb/s optical links using custom serialisers and optical converters. ASICs have been developed for the ADC, serialiser and transmitters for this project and prototype front-end boards are under test now, approaching series production. In the new back-end system, the received digital data will be processed with a FIR filter, on a FPGA (Intel-FPGA Arria-X) to identify the bunch crossing and extract the transverse energy with a fixed latency. The results of the digital processing are transferred to the level-1 trigger system “feature extractors” for trigger object reconstruction. The backend system is developed using the ATCA architecture. ATCA carrier blades with RTM will carry Advanced
Mezzanine Cards with the main FPGAs.

In order to verify the full functionality of the new LAr trigger readout system, a demonstrator set-up has been installed on one small section of ATLAS detector and has been operated in parallel to the regular ATLAS data taking during the LHC Run-2. We have collected data with 13 TeV proton-proton collisions during the LHC Run-2, and have observed real pulses from the detector through the demonstrator system. An upgraded demonstrator with pre-production boards are being installed on detector during the 2017-18 year end technical stop.

The talk will give an overview of the Phase-I Upgrade of the ATLAS Liquid Argon Calorimeter trigger readout and present the custom hardware including the real-time data processing and fast data transfer. The contribution will show the performance of the prototype boards in the demonstrator system including the newly developed ASICs with their radiation tolerance certification and quality assurance. Results of the system integration test with the final prototypes will be reported.

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