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First performance measurements of the Fast Tracker Real Time Processor at ATLAS

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Real-time track reconstruction at hadron colliders is one of the most powerful tools to select interesting events from the huge background while mitigating the pile-up effect. The Fast Tracker, an upgrade to the current ATLAS trigger system, will feed the high level trigger with high quality tracks reconstructed over the entire detector at 100 kHz rate. Half of the system has been produced and integration in ATLAS is proceeding in order to demonstrate functionality with real data with a partial detector coverage. The performance of the system from tests with real data and laboratory measurements will be reviewed.

Summary

The ATLAS [1] Fast TracKer [2] is a custom electronics system that will operate at the full Level-1 accept rate, 100 kHz, to provide high-quality tracks as input to the high level trigger (HLT). The detector is subdivided into towers of 12 layers. Each slice is processed in its own asynchronous, data-driven pipeline. The pipeline first computes hit centroids inside boards called Data Formatters (DF) and feed them to the Processing Unit (PU) that finds coincidences to form 8-layer track candidates. Hits from the 8-layer track candidates are fit and selected based on the goodness of fit. Finally, the Second Stage Board (SSB) adds silicon hits to the selected good track candidates and refit tracks with 12 layers providing them to the HLT through the Interface Card (FLIC).

The combinatorial challenge inherent to tracking is solved by the PU exploiting the massive parallelism of Associative Memories that can compare inner detector hits to millions of pre-calculated patterns simultaneously. The tracking problem within matched patterns is further simplified by using pre-computed linearized fitting constants and leveraging fast Digital Signal Processing in modern commercial FPGAs. Testing and reliability are aided by built-in logic state analysis and test-data sourcing at each board input and output. Adaptability is enhanced by the use of modern FPGAs.

Half of the system has been produced and will be integrated into ATLAS during 2018 to verify functionalities with real data. The FTK Configuration for 2018 includes 32 DFs, 64 PUs, 32 SSBs, 16 FLICs. Commissioning up to now focused on two slices of FTK: a complete pipeline producing 12 layer tracks (Slice1) and a reduced version without the SSB and FLIC producing 8-layer tracks (Slice2). Detector input to both slices is chosen to cover small eta/phi range, a detector tower. First Slice2 and after Slice1 were incorporated into ATLAS and reconstructed tracks were validated with FTK functional simulation. The 2018 plan includes a progressive increase of the system to reach stable track processing by 50% of FTK.

Tracking efficiency and tracking resolution and timing performances will be measured with acquired data. We will describe the system features needed to improve data processing reliability. Among these features are the use of trigger pre-scale to reduce back pressure if necessary; the pattern bank optimization improving the PU timing performances and increasing the efficiency in the presence of non-functioning channels; error detection and propagation; monitoring tools that identify and recover errors in real time; synchronization handling.

Finally, the 2018 data taking is a first valid test benchmark for the FTK-HLT integration. FTK trigger performance is being evaluated in Trigger re-processing (using FTK full simulation on data) and MC validation samples. The 2018 trigger deliverables related to FTK will be presented.

[1] ATLAS Collaboration., "The Fast Tracker (FTK) Technical Design Report"CERN-LHCC-2013-007 ; ATLAS-TDR-021; available online: https://cds.cern.ch/record/1552953

[2] The ATLAS Collaboration, "The ATLAS Experiment at the CERN Large Hadron Collider,"Journal of Instrumentation 3 S08003, 2008.

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