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Status of the Readout Electronics for the Triple-GEM Detectors of the CMS GE1/1 System and Performance of the Slice Test in the 2017-18 LHC Run

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In this contribution, we will present the status of the electronics system of the triple-GEM detectors for the CMS GE1/1 upgrade, which is planned for installation in 2019-2020, as well as the performance of ten prototype detectors which have been installed in CMS since 2017.

For this new CMS muon sub-detector, a new front-end chip, the VFAT3, has been designed. The VFAT3 communicates with the back-end microTCA electronics through the GBTx chipset and the versatile link. Each of the 144 triple-GEM detectors has 24 VFAT3s, 3 GBTx chipsets, and a Virtex-6 FPGA, all powered by 10 FEAST DC-DC converters.

Summary

In this contribution, we will present the status of the readout electronics system of the triple-GEM detectors of the GE1/1 system, an upgrade which is planned for installation into the CMS experiment during the next LHC long shutdown (LS2) in 2019-2020. We will also report on the performance of the ten "slice test"detectors which have been present in the CMS muon endcap since the 2017 LHC run.

Ten "slice test"detectors were installed into the CMS muon endcap in January 2017. These detectors are read-out on the front-end by 24 VFAT2 chips and a corresponding v2 optohybrid board, and from the back end utilizing a microTCA crate containing CTP7 and AMC13 boards. The v2 optohybrid board is equipped with a Virtex-6 FPGA and one GBTx chipset which communicates with the back-end electronics through the versatile link. On each detector, the 24 VFAT2s communicate with the optohybrid through a 1m-long PCB, called the GEM electronics board (GEB), which they plug into. Two of the ten detectors also include temperature sensors, and are powered via a multichannel power supply, as the final GE1/1 detectors will be. Data was recorded throughout the 2017 run, using both cosmic ray muons and LHC collisions. This, and the overall performance of the slice test detectors, will be reported.

Using the lessons learnt from this slice test allowed for the further development of the final GE1/1 v3 electronics which will be used in the LS2 installation. These new detectors will be read out by the VFAT3 chip, which runs at 320 MHz, four times higher than the frequency of the VFAT2 chip, as well as the v3 optohybrid board which is equipped with a Xilinx Virtex6 FPGA and three GBT chipsets. The on-detector electronics are powered via ten FEAST DC-DC converters. The GEB has been re-designed to accommodate the faster VFAT3 digital signals and to bring the power from the FEASTs to the various front-end components. In February 2018, two of such v3 detectors have replaced two of the v2 "slice test"detectors and the GE1/1 electronics production has now started.

This contribution will report on the improvements made to the electronics in view of the installation of GE1/1 and on the very first results of the final GE1/1 v3 electronics obtained in CMS.

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