Frontend and backend electronics for the New Small Wheel Upgrade of the ATLAS muon spectrometer

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On behalf of the ATLAS Muon Collaboration

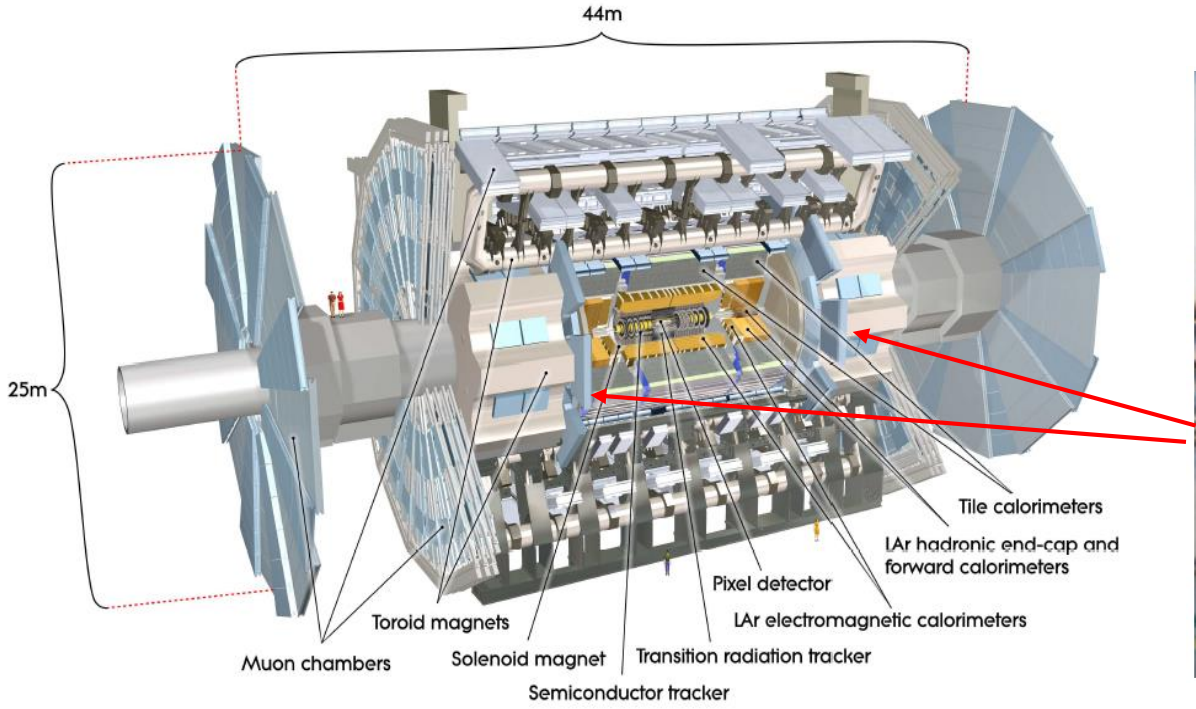
TWEPP 2018

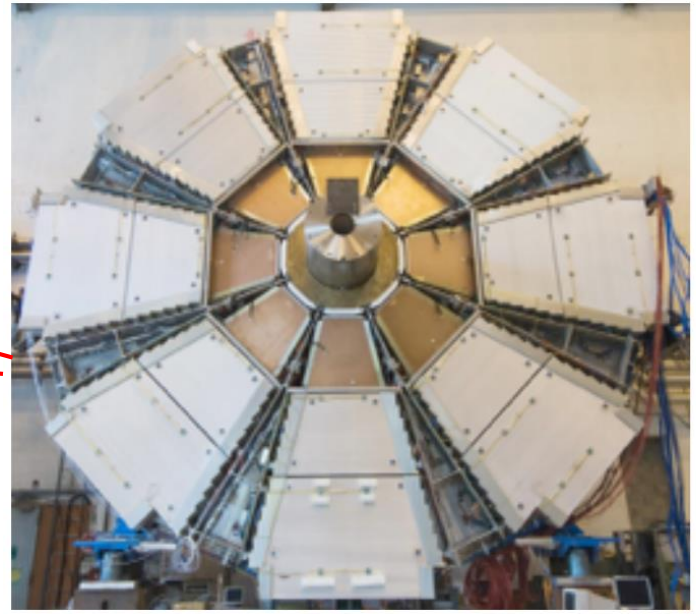
Outline

- ❑ATLAS NSW Upgrade
- ❑NSW Readout Chain
- ❑NSW Trigger Chain
- ❑NSW Frontend and Backend Electronics

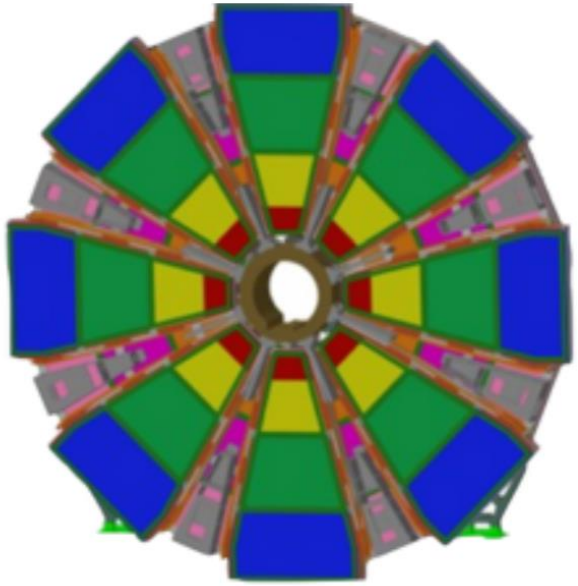
ATLAS NSW Upgrade

Atlas Experiment at CERN





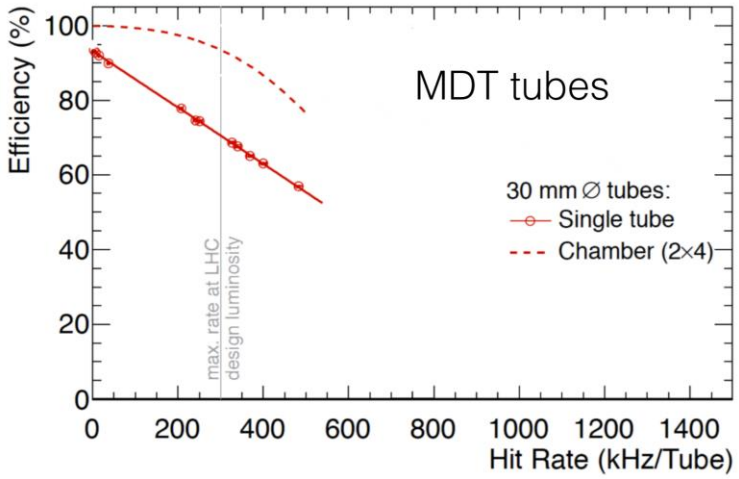
Small Wheel

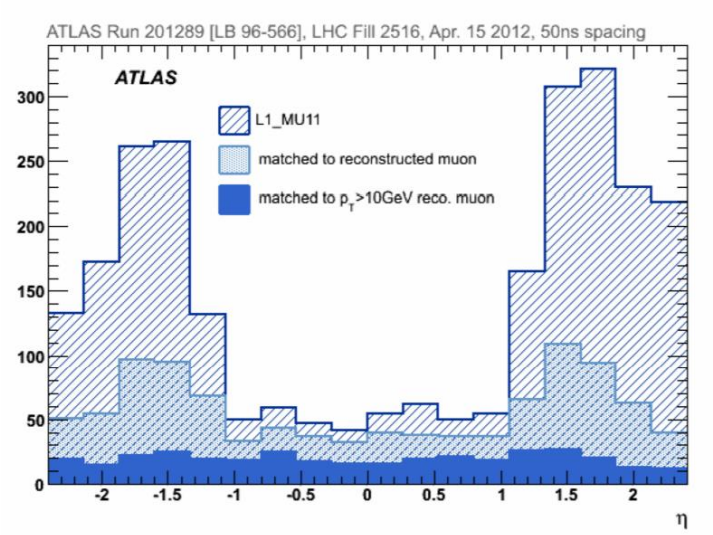


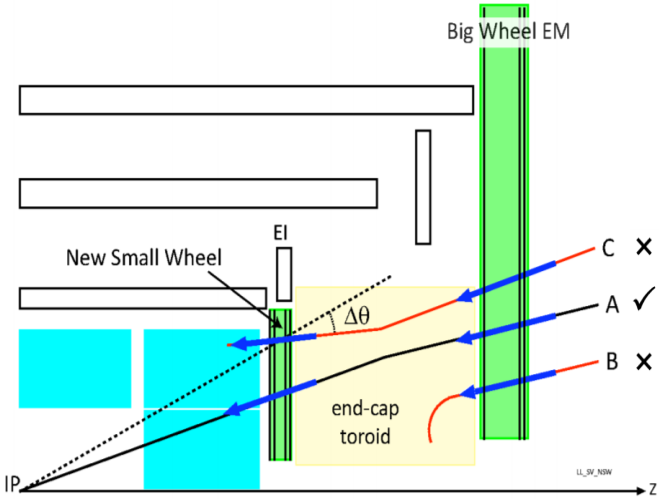
New Small Wheel

LHC Upgrade:
After the LS2 (2019-2020),LHC reaches design energy 14 TeV and increases collision intensity L=2-3x10^{34}/ cm^2/s
After the LS3 (2023-2024),LHC moves to High Luminosity LHC (HL-LHC) phase and increases collision intensity to L=5-7x10^{34}/cm^2/s

The upgrade of NSW





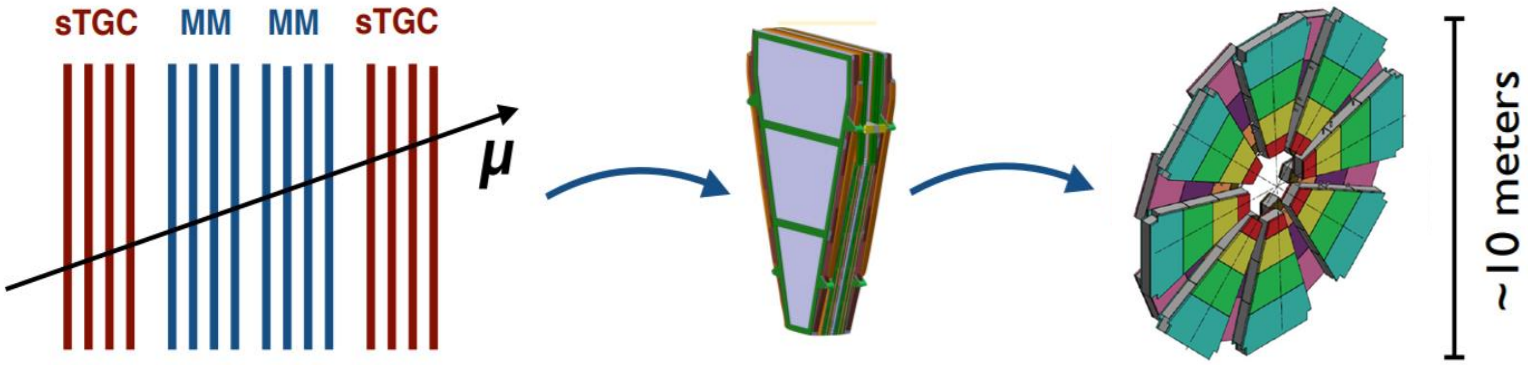


- Current Small Wheel Chambers will loose efficiency at high rate
- 90% of the current End-cap muon triggers are fakes

NSW:

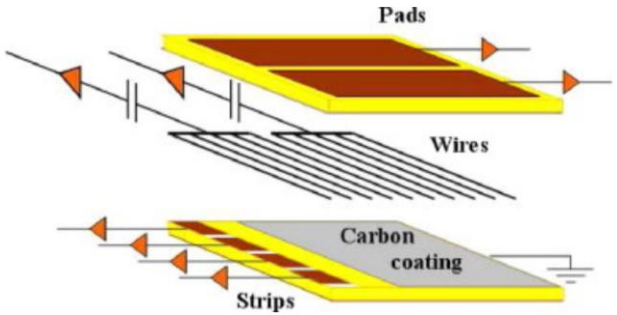
- A set of precision tracking and trigger detectors able to work at high rates
- Will provide online high quality (Δθ ~1 mrad) IP pointing segments
- <1035ns latency to be in time with Big Wheel trigger (~ 500 ns for fiber)
- 95% on-line track reconstruction efficiency
- Significant reduction of fake Level-1 muon triggers

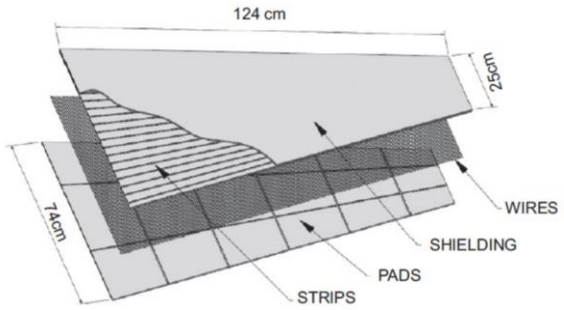
NSW structure

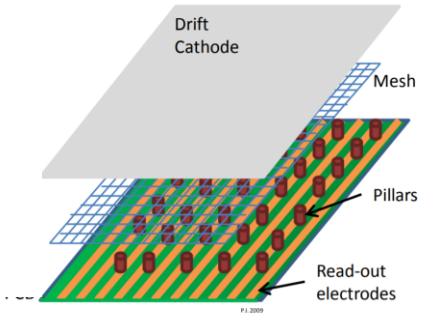


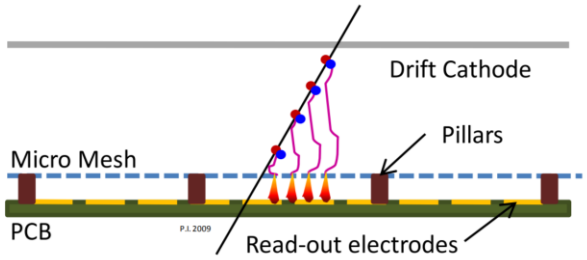
16 planes

16 sectors







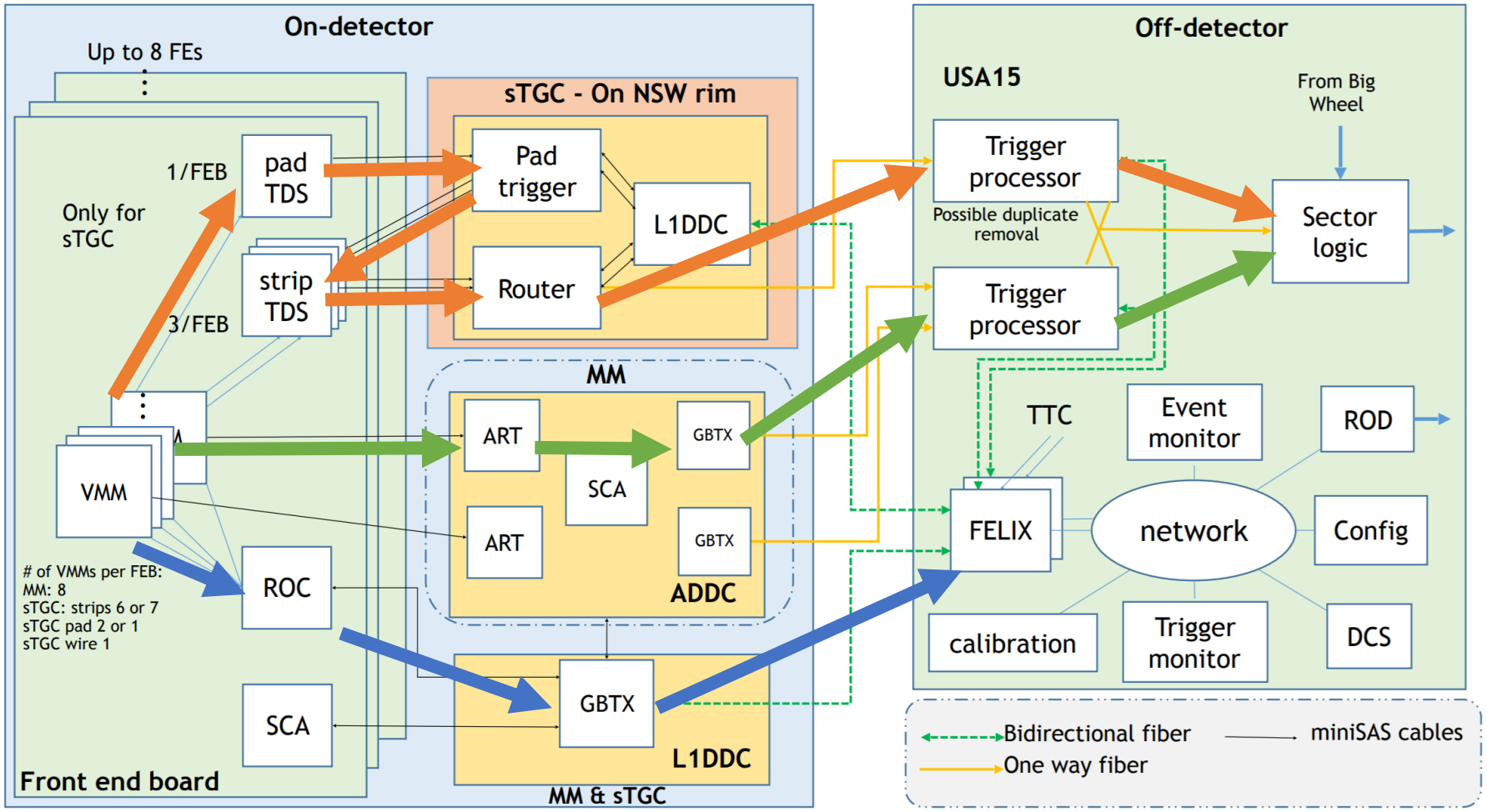


Small-strips Thin Gap Chamber(sTGC):
Mainly for trigger, also for precision tracking
Good timing resolution:Drift time for most electrons < 25ns
Better than 1mrad angular resolution

Micronegas(MM):
Mainly for precision tracking, also for trigger
Space resolution < 100 μm independent of track incidence angle
Good tracking due to 0.4mm readout strips
Low operating HV at 550V

NSW Electronics

Poster #67



sTGC Trigger MM Trigger NSW Readout

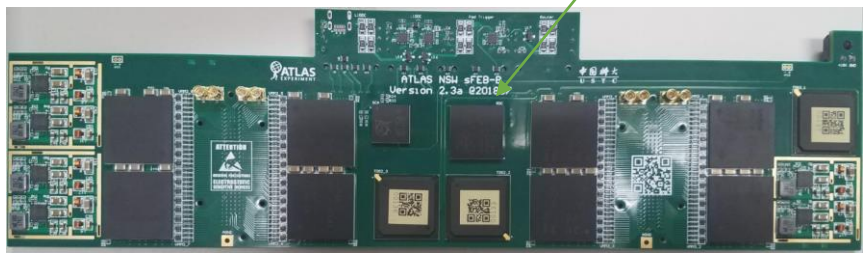
Radiation tolerant ASICs:
- VMM (amplifier, shaper, discriminator)
- Read Out Controller (ROC)
- Trigger Data Serialiser (TDS)
- Address Real Time (ART)
- Slow Control Adapter (SCA)
- GigaBit Transceiver (GBTX)

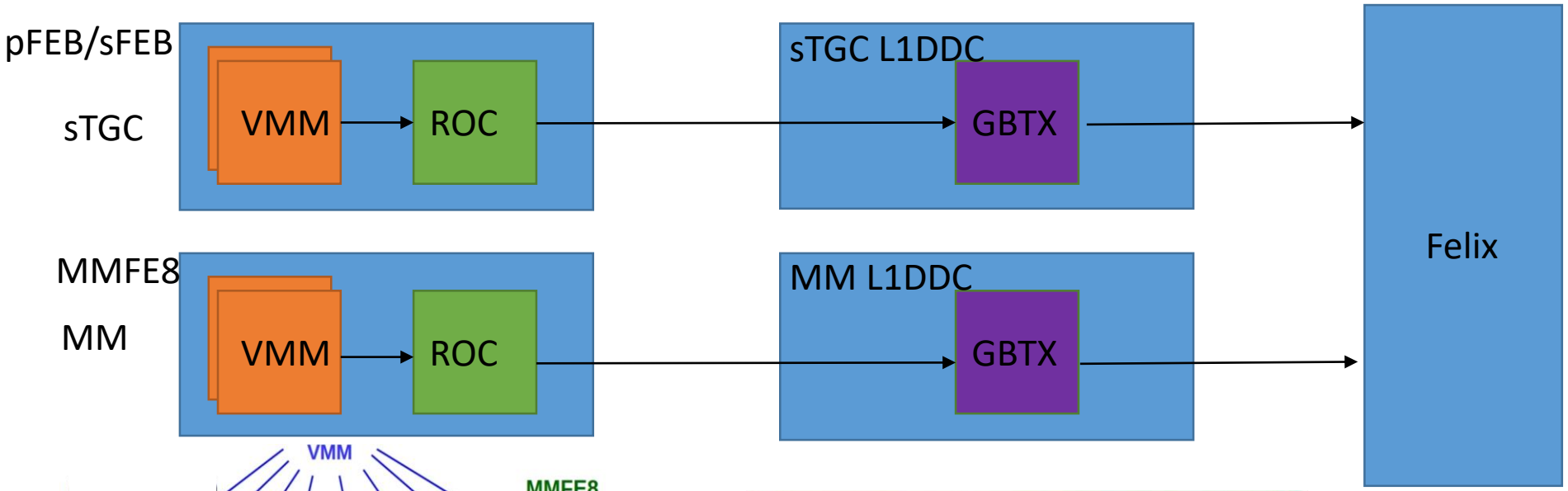
PCBs:
pFEB/sFEB(sTGC pad/strip front-end board)
MMFE8(Micromegas front-end board)
L1DDC(Level-1 Data Drive Card)
Pad Trigger
Router
ADDC
FELIX(Front-End LInk eXchange)
Trigger Processor

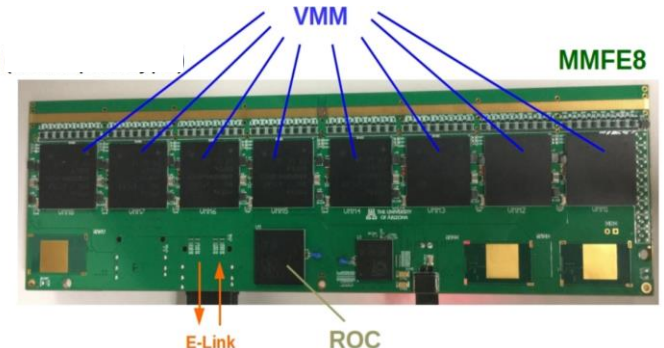
NSW Readout Chain

NSW readout chain

ROC

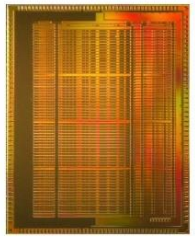




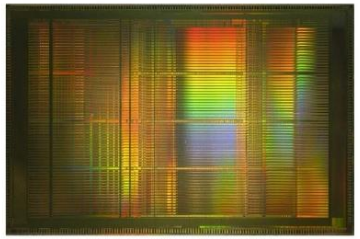


VMM ASIC

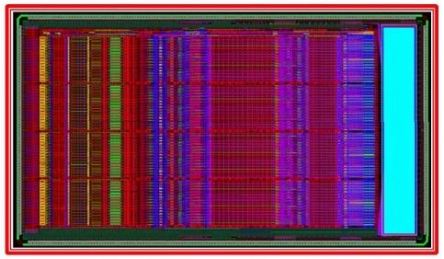
Path Towards VMM3



VMM1 (2012)
50 mm²
500k MOSFETs (8k/ch.)
- mixed-signal
- 2-phase readout

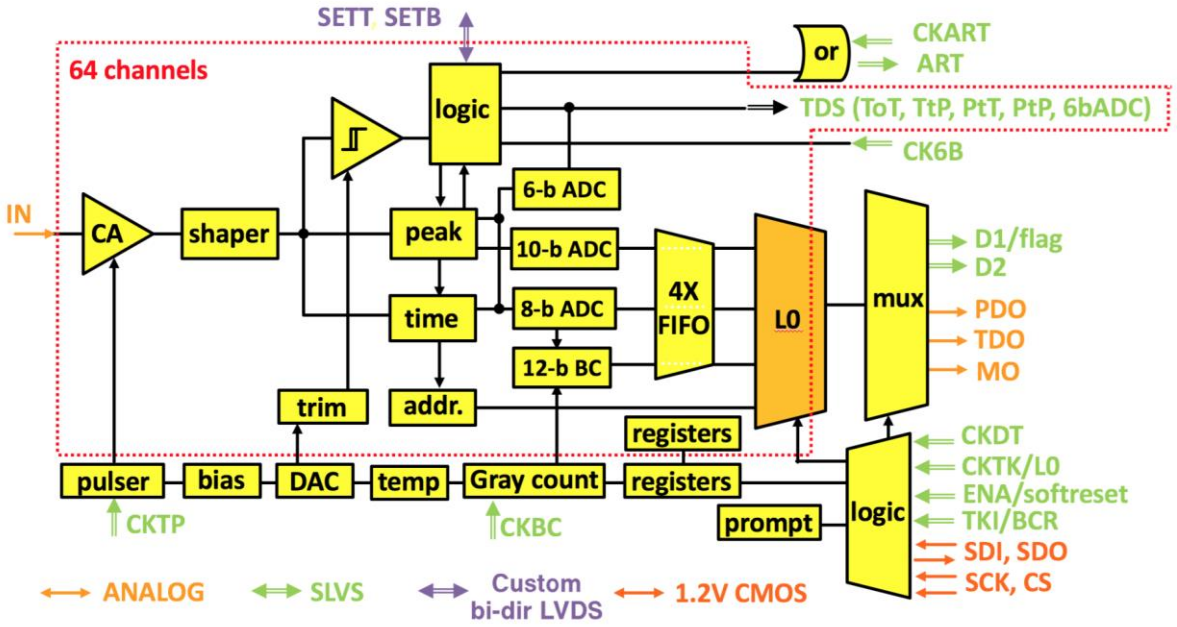


VMM2 (2014)
115 mm²
> 5M MOSFETs (>80k/ch.)
- planned deep re-design of VMM1
- much higher functionality and complexity than VMM1
- continuous fully-digital readout



VMM3 (2015-16)
130 mm²
> 6M MOSFETs
- **L0 handling, SEU-tolerant, SLVS IOs, deeply revised front-end for sTGC signals, various additional functions, various fixes**
- **input from many collaborating teams with broad range of expertise**
- **aims at pre-production**

- ❑ VMM is the front-end ASIC to be used in the front end electronics readout system of both the Micromegas and sTGC detectors of the New Small Wheels Upgrade project.
- ❑ 64 channel ASD,ADC,TDC,L0 trigger matching



Front-end Electronics (ASIC)
- ❑ more than 2.3 million channels total(64 per chip)
- ❑ operate in both polarities of charge
- ❑ sensing element capacitance 10-200 pF
- ❑ charge meas. up to 2 pC @ < 1 fC rms
- ❑ time meas. ~ 100 ns @ < 1 ns rms
- ❑ low power (< 10mW/ch)

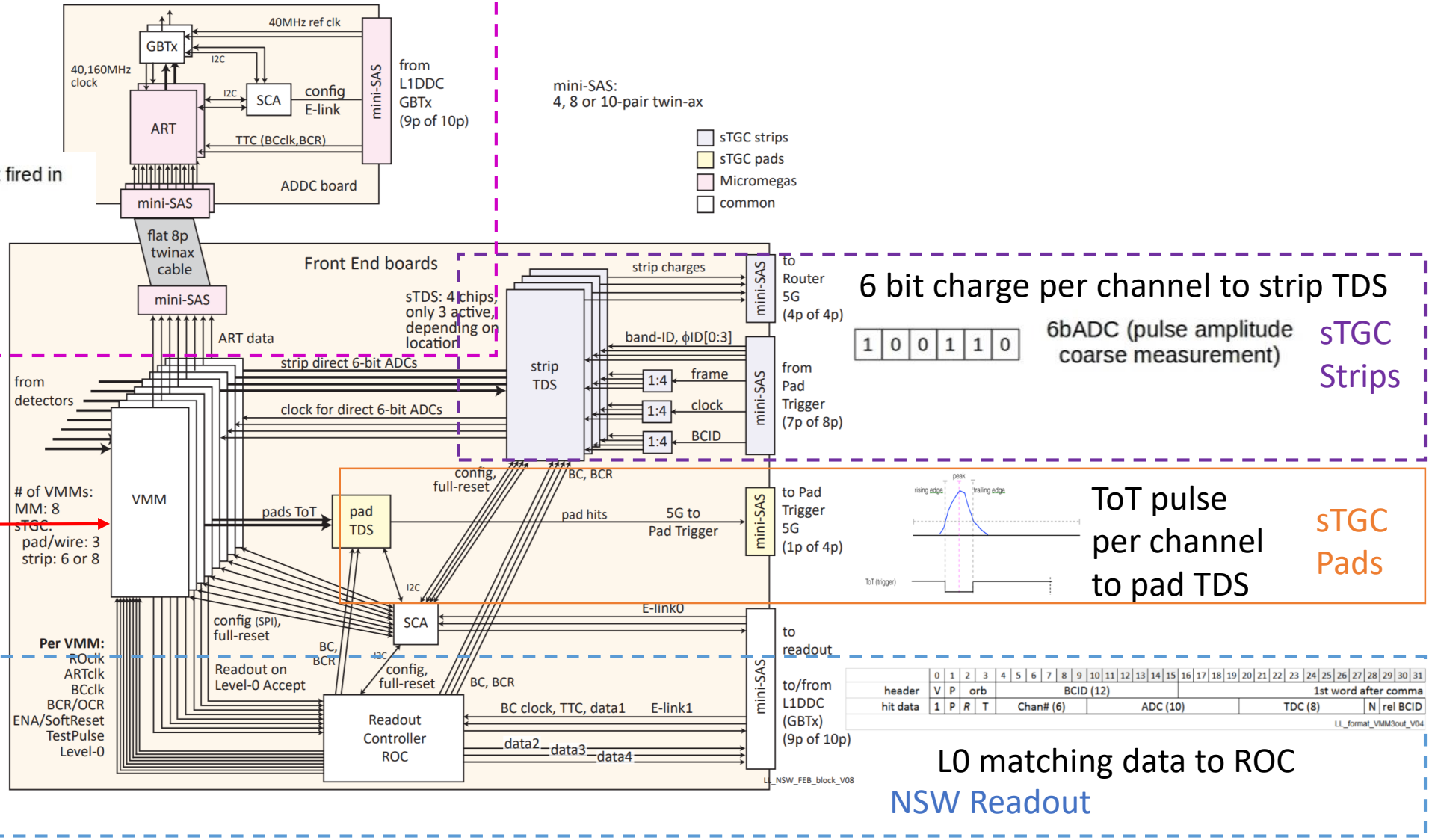
VMM Interface

6bit first channel number to ADDC

1	0	1	0	1	1

ID of first channel that fired in the chip

MM trigger



6 bit charge per channel to strip TDS

1	0	0	1	1	0

6bADC (pulse amplitude coarse measurement)

sTGC Strips

64 channel input from detectors

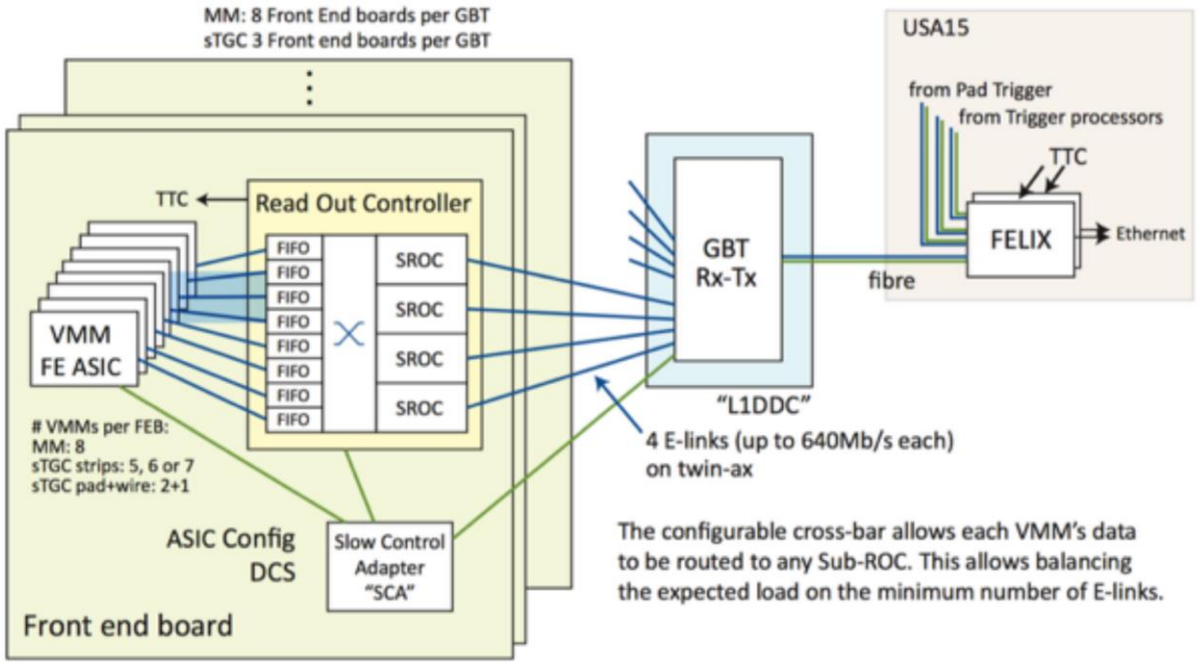
ToT pulse per channel to pad TDS

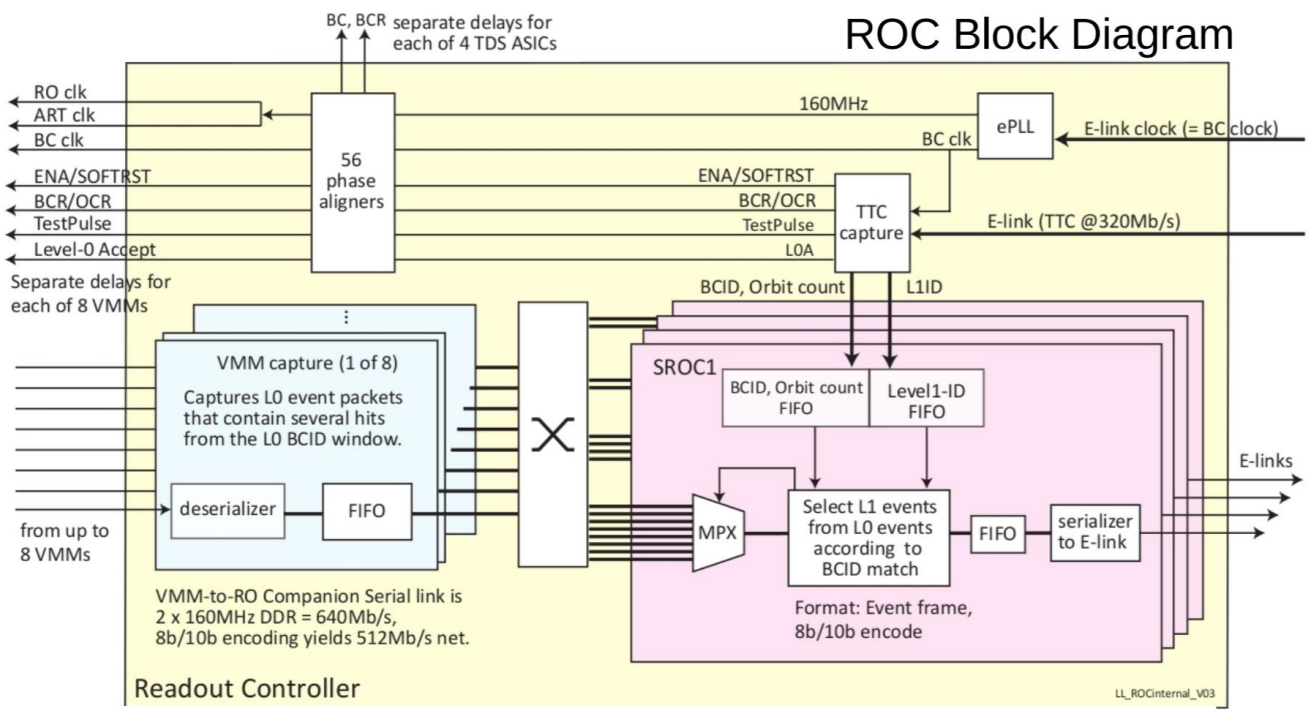
sTGC Pads

L0 matching data to ROC

NSW Readout

ROC(Readout Controller) ASIC

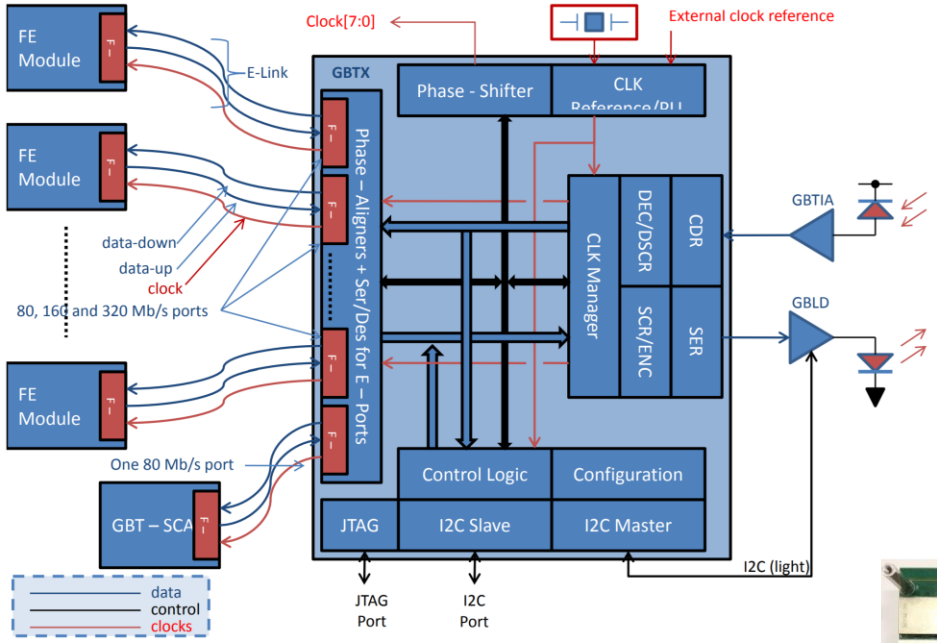




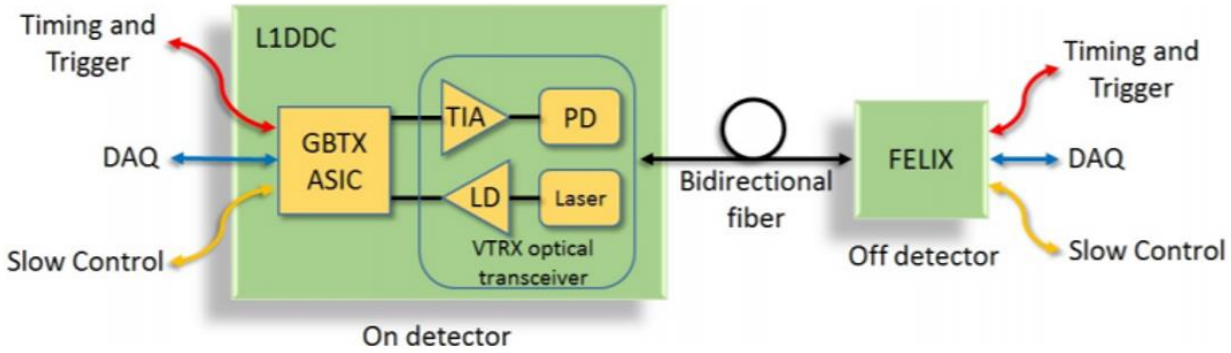
Block Diagram for ROC

- ROC interface up to 8 VMMs, 2 input lines per VMM chip ,512Mbps effective bandwidth
- Decodes and forwards TTC signals (e.g. BCR,L0A) to the VMMs, distribute BC clocks
- Captures the Level-0 selected data from the VMMs, selects Level-1 matching data, formats and sends via E-link
- 4 sROC is connected upstream with the L1DDC board via E-link, at up to 640 Mbps speed

L1DDC and GBTX



- The GBTX is a radiation tolerant chip that can be used to implement multipurpose high speed (3.2-4.48 Gb/s user bandwidth) bidirectional optical links for high energy physics experiments.
- Allow a single bidirectional link to be used simultaneously for data readout, trigger data, timing control distribution, and experiment slow control and monitoring.

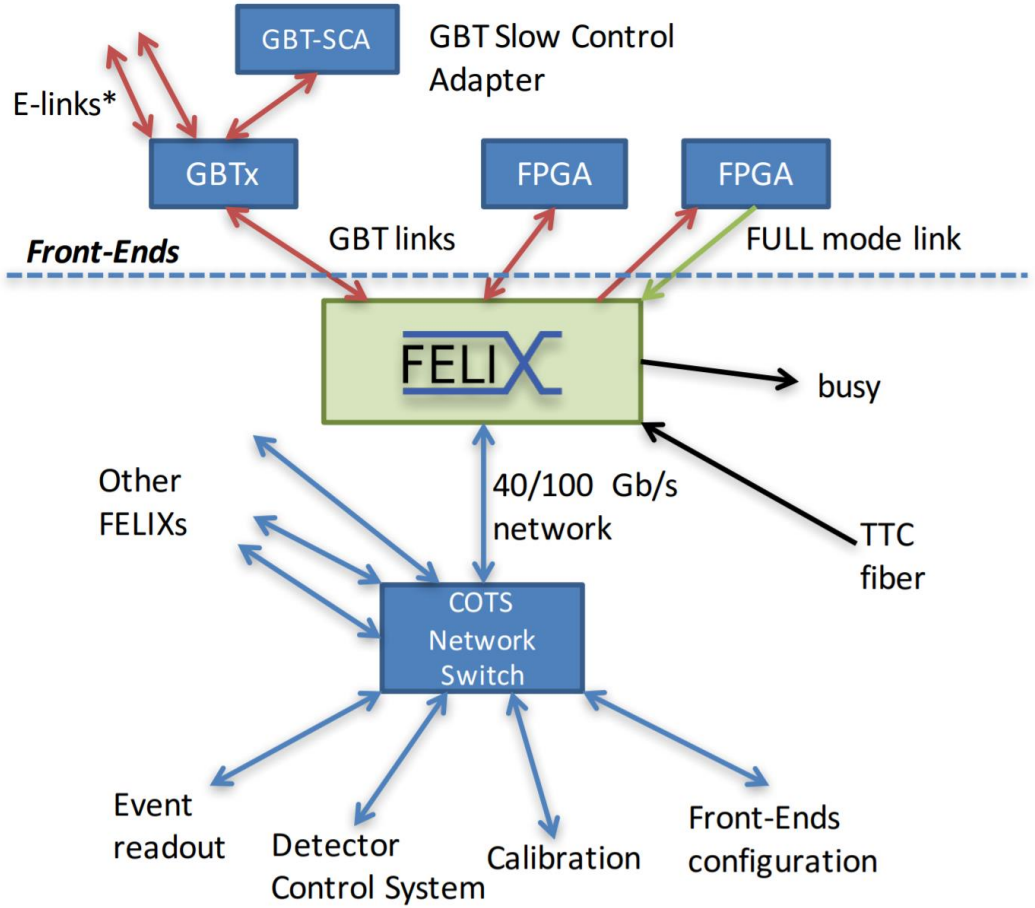


The Level-1 Data Driver Card (L1DDC) is an intermediate board that aggregates and transmits the Level-1 data (time, charge and strip address corresponding to a single hit) from multiple front-end (FE) boards to FELIX

3 different types of L1DDC in NSW upgrade

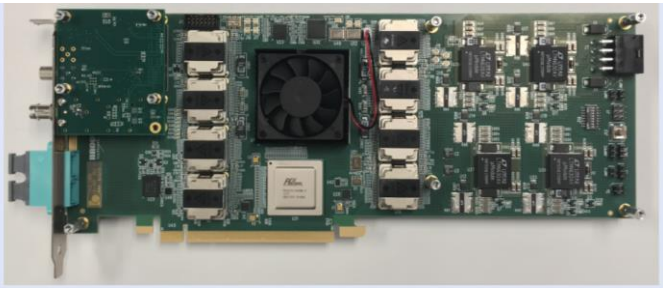
Poster #71

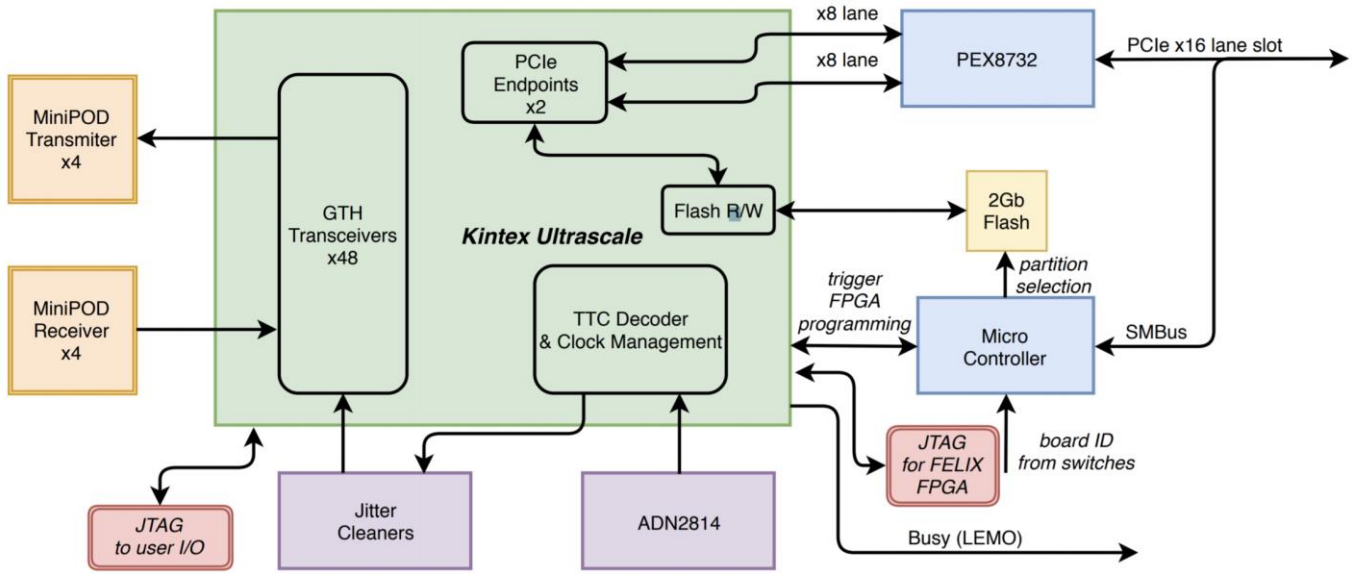
FELIX(Front-End LInk eXchange)



FLX-712 (or BNL-712)

- Final production board
- Xilinx Kintex UltraScale XCKU115
- 48 optical links (MiniPODs)
- TTC input ADN2814
- PCIe Gen3 x16 (2x8 with switch)
- Si5345 jitter cleaner





Block Diagram for FELIX

- FELIX is a router between front-end serial links and a commodity network, which separates data transport from data processing.
- Routing of detector control, configuration, calibration, monitoring and detector event data
- TTC (Timing, Trigger and Control) distribution integrated Configurable E-links in GBT Mode
- Detector independent

NSW Trigger Chain

sTGC Trigger Chain

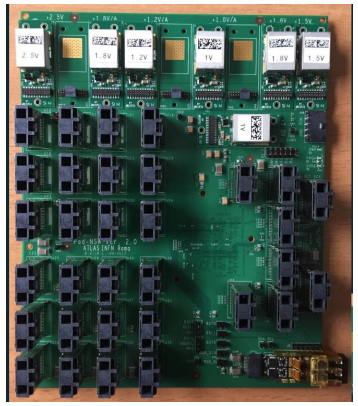
Pad TDS

pFEB

Pad Signal

VMM

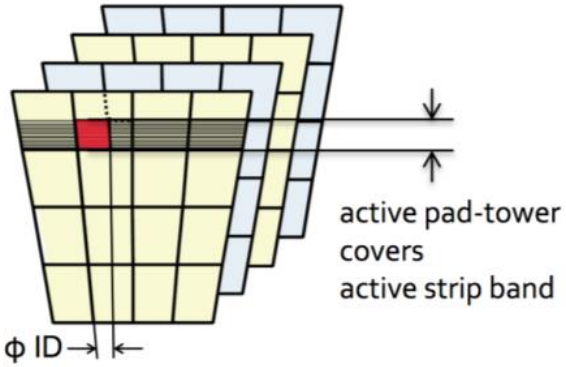
Pad TDS



Pad Trigger

FPGA

3 out of 4 coincidence and send BCID+ band phi ID to strip TDS



sFEB

Strip Signal

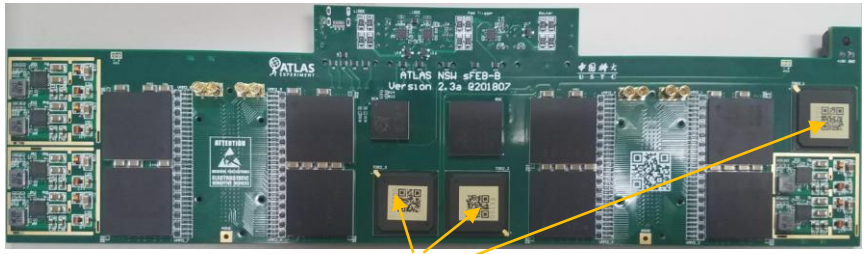
VMM

Strip TDS

Router

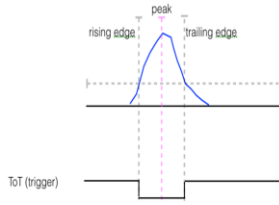
FPGA

Trigger Processor

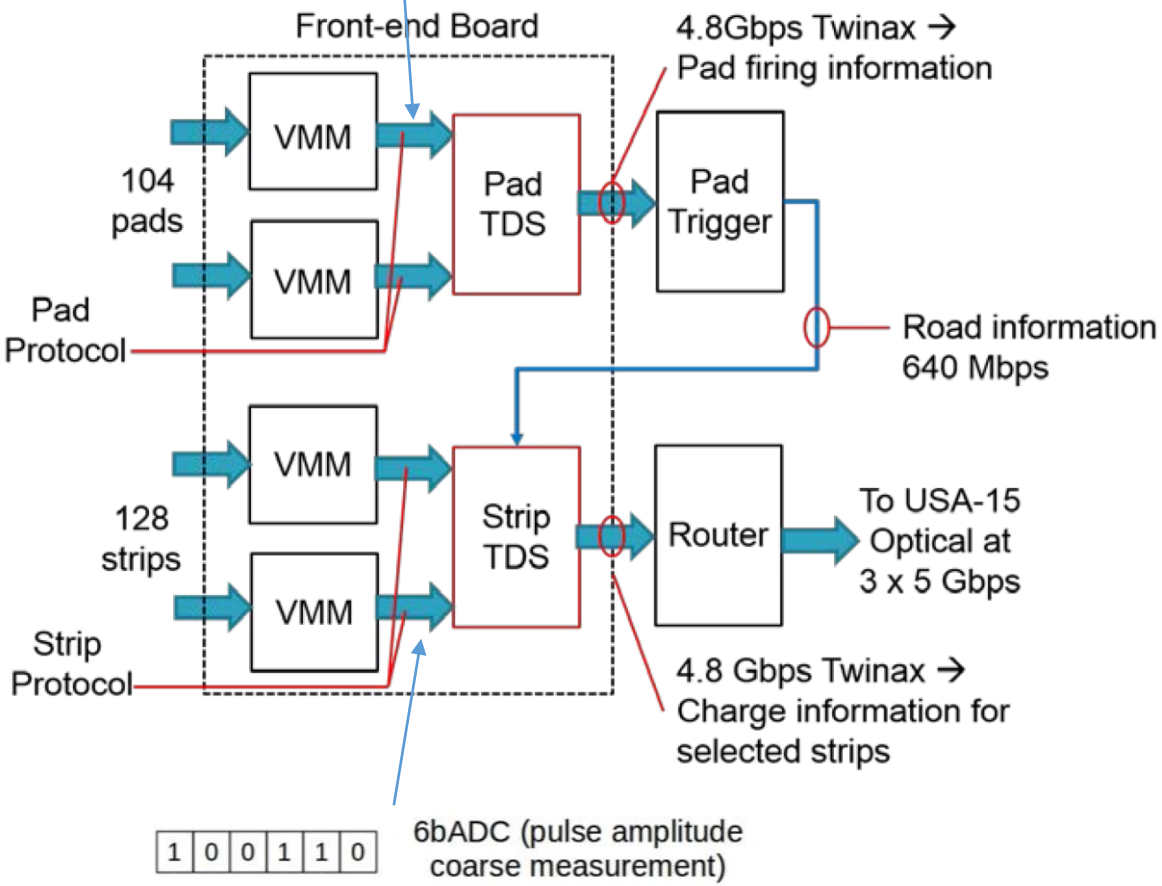


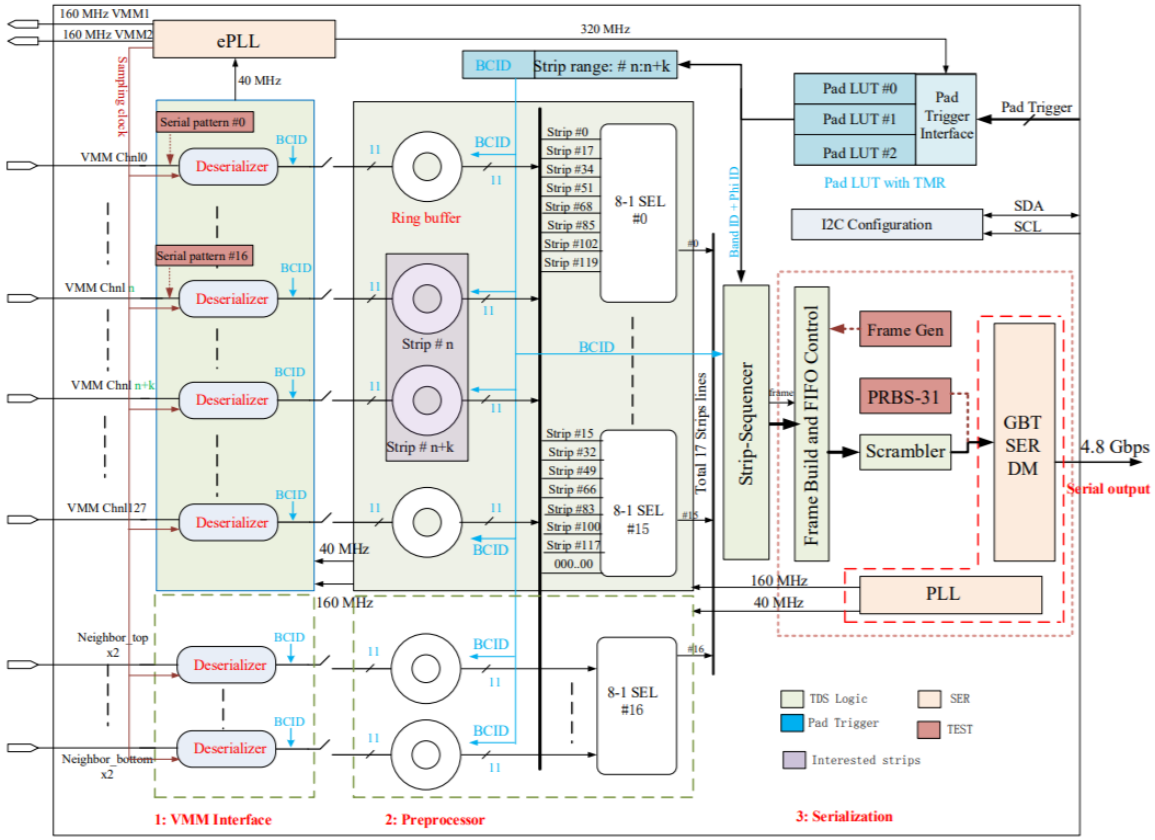
Strip TDS

TDS(Trigger Data Serializer)



ToT(time over threshold)
pulse per channel

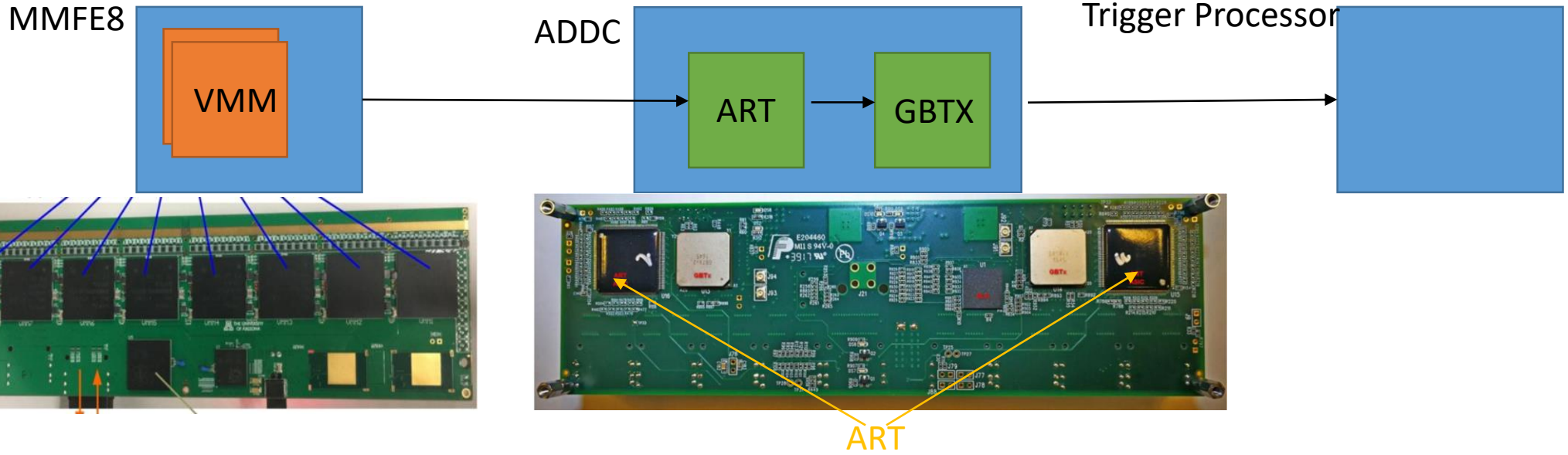


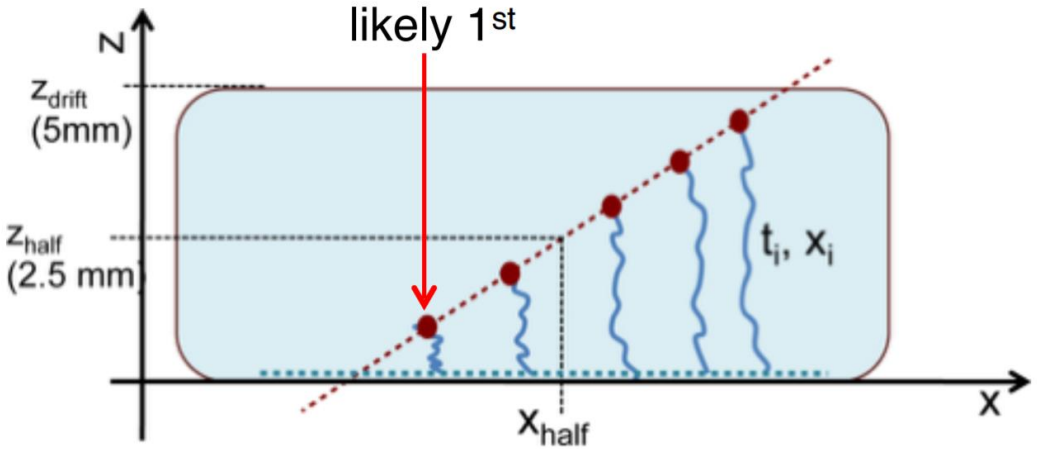


Block Diagram for Strip TDS

The TDS ASIC is responsible for preparing trigger data for both sTGC pads and strips, performing pad-strip matching, and serializing data for transmission to the circuits on the rim of the NSW detector.

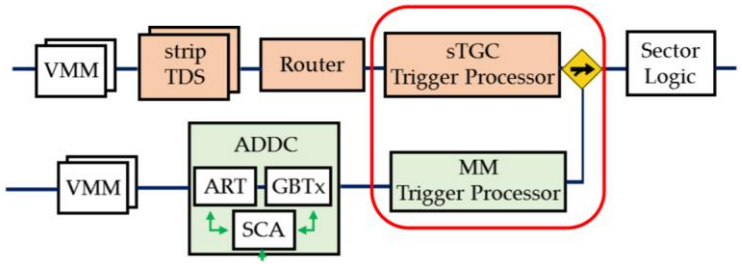
MM Trigger Chain

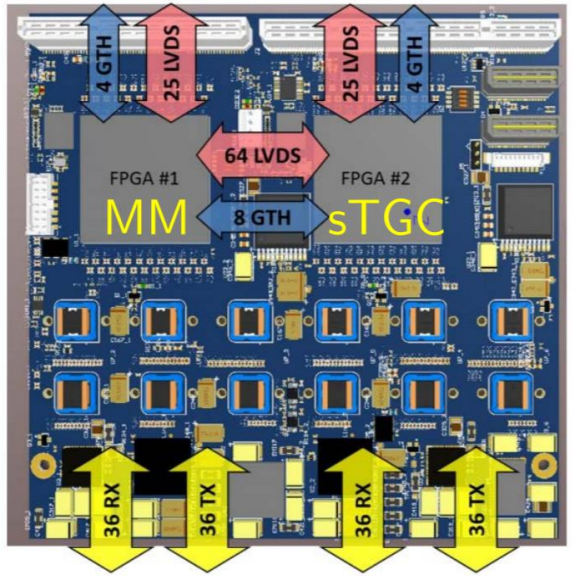




- MM trigger is relatively simpler due to the 0.4mm strip pitch, just recording the strip number with the earliest hit across the chip will be good enough
- Each VMM sends the address (channel #) of only its first hit in each proton-proton collision to an ART(Address in Real Time) ASIC located on a so-called “Art Data Driver Card” (ADDC) located on-detector
- The ART ASIC chooses at most 8 addresses from 32 VMMs to an on-board GBTx which will forwards to the MM Trigger Processor

Trigger Processor

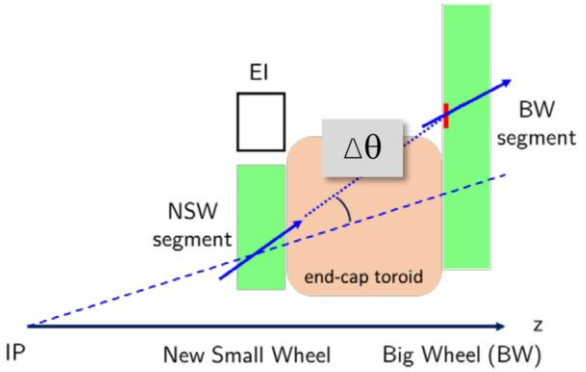


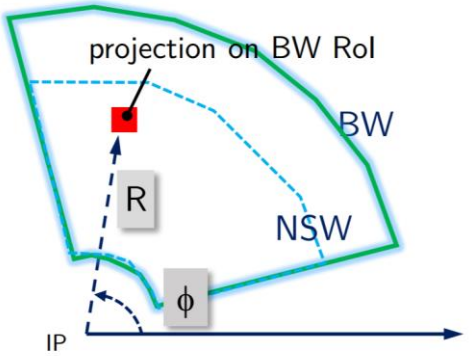


Data format for 1 segment

Segment pointing — Projection on BW RoI

Field	sTGC hit	MM hit	Δθ (mrad)	ϕ index	R index	Spare
#. of bits	2	2	5	6	8	1
Resolution:			1 mrad	20 mrad	0.005 (η)	





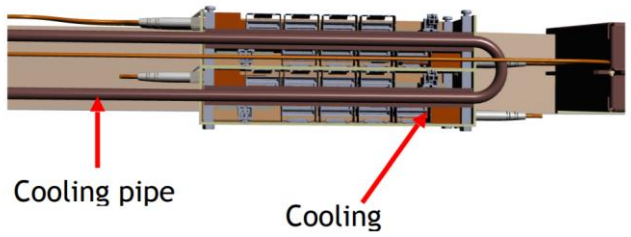
Information sent from TP to SL

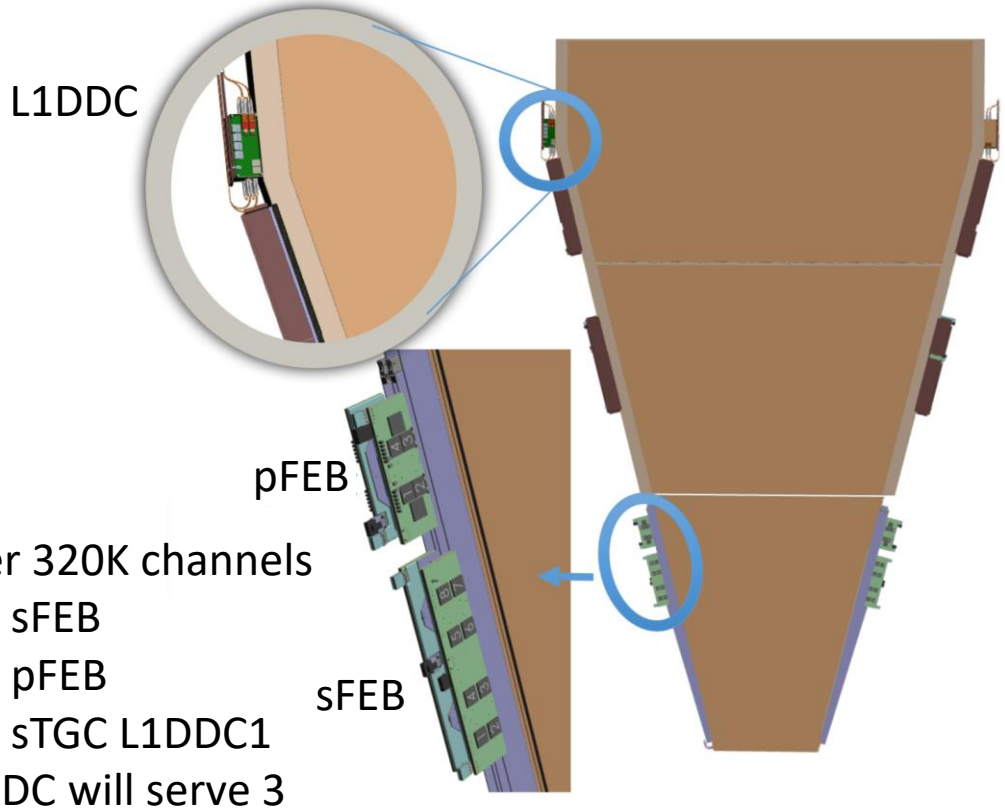
- ❑ R-ϕ pointing to Big Wheel regions of interest (RoI)
- ❑ Δθ between local segment slope and slope of “IP pointing” track

- ❑ MM & sTGC trigger processor located on FPGA-based ATCA Mezzanine Cards
- ❑ Independent trigger path and algorithms on different FPGAs for sTGC&MM
- ❑ Creating powerful redundant trigger system with sufficient resolution

NSW Frontend and Backend Electronics

On Detector Electronics

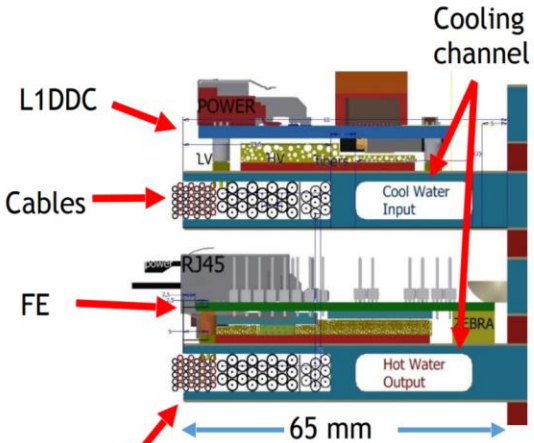


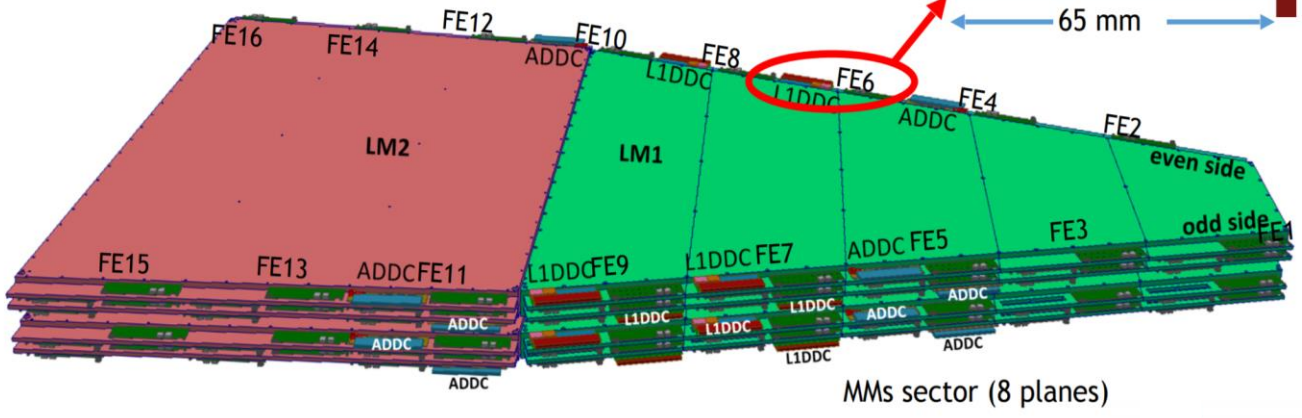


- Over 320K channels
- 768 sFEB
- 768 pFEB
- 512 sTGC L1DDC1
- L1DDC will serve 3 front ends of each plane

sTGC

- Over 2 million channels
- 512 MM L1DDC
- 512 ADDC
- 4096 MMFE8
- 1 L1DDC & 1 ADDC will serve the 8 MMFE8 located on each side of a plane

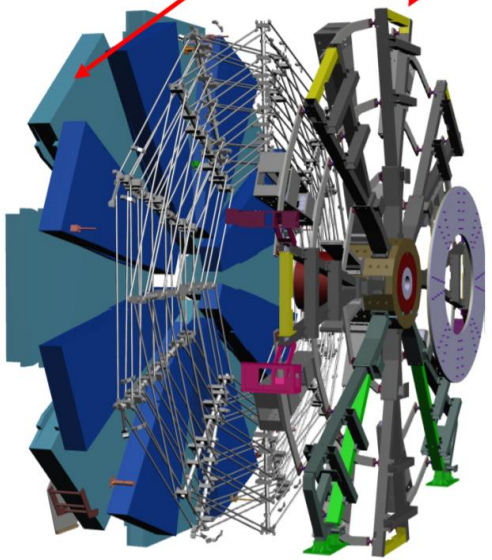


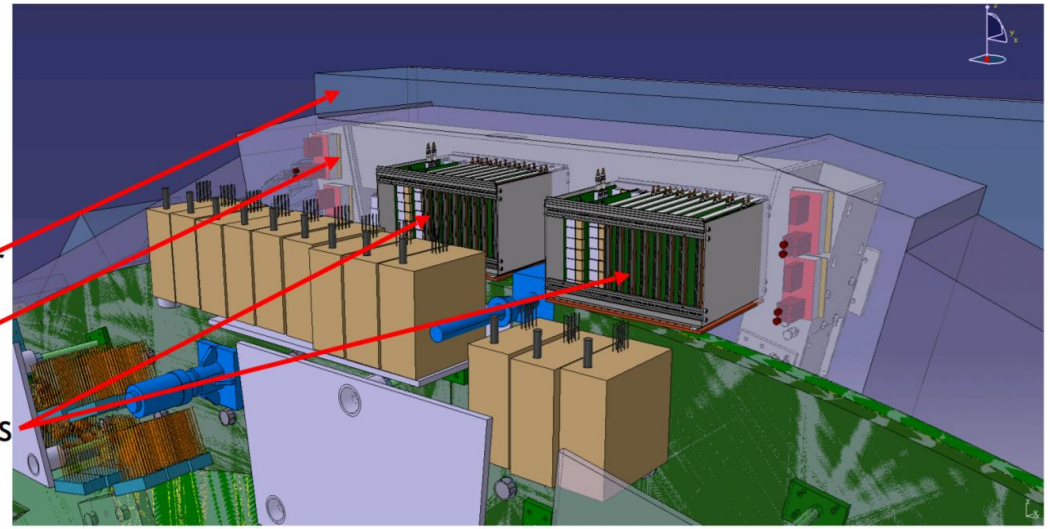


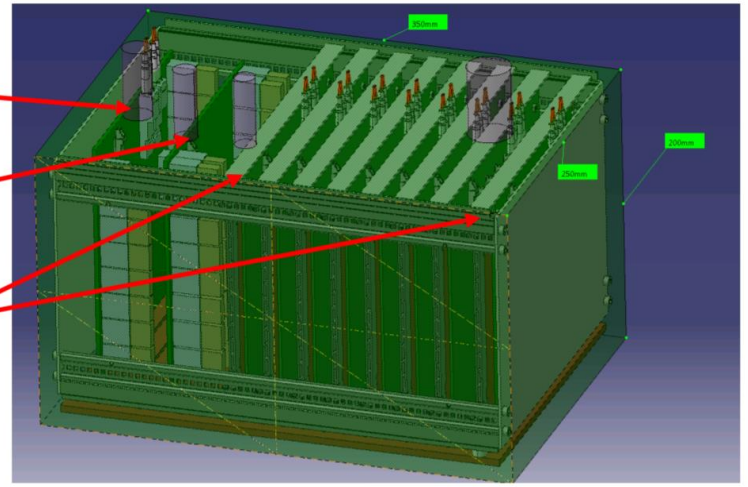
MMs sector (8 planes)

Micromegas

On RIM Electronics







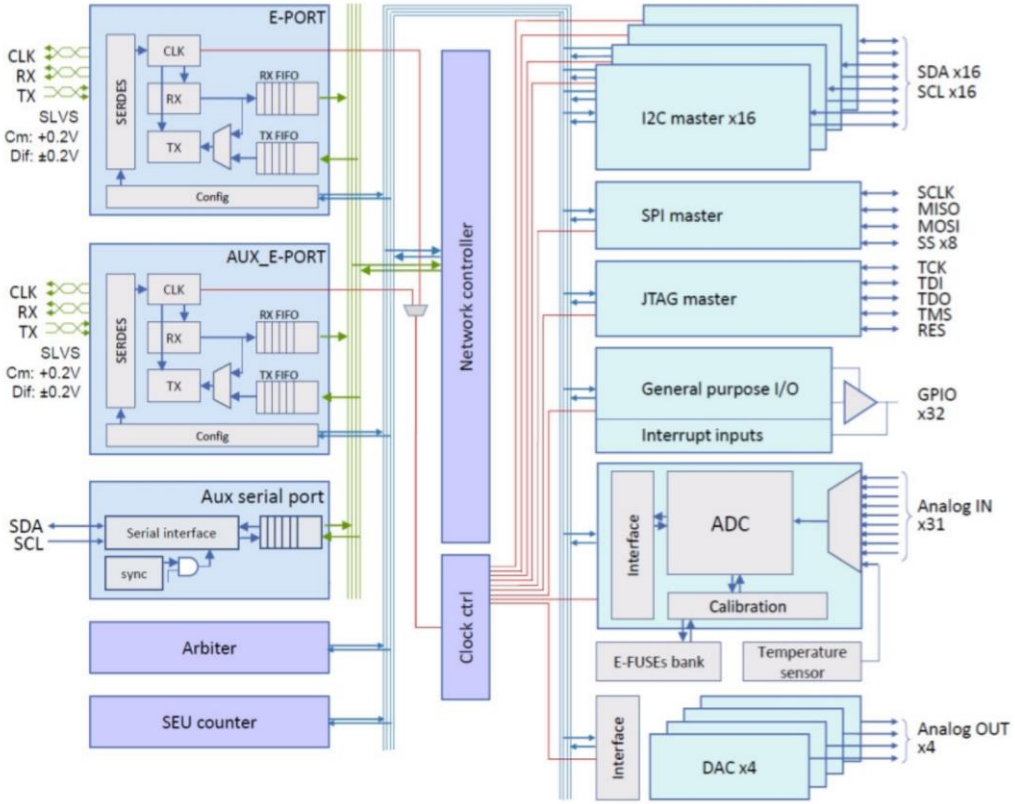
- 1 RIM box per sector
- Commercial boxes and electronics will be used
- 32 RIM-L1DDC
- 32 Pad trigger boards
- 256 Routers boards

Summary

- NSW electronics will be able to cope with the high data rates of the HL-LHC under a harsh radiation environment
- All the ASICs and PCB prototypes has been demonstrated during the latest integration week
- Preproduction for the ASICs and PCBs are ongoing or scheduled
- Final integration will be performed next year

Thank You!

SCA(Slow Control Adapter) ASIC



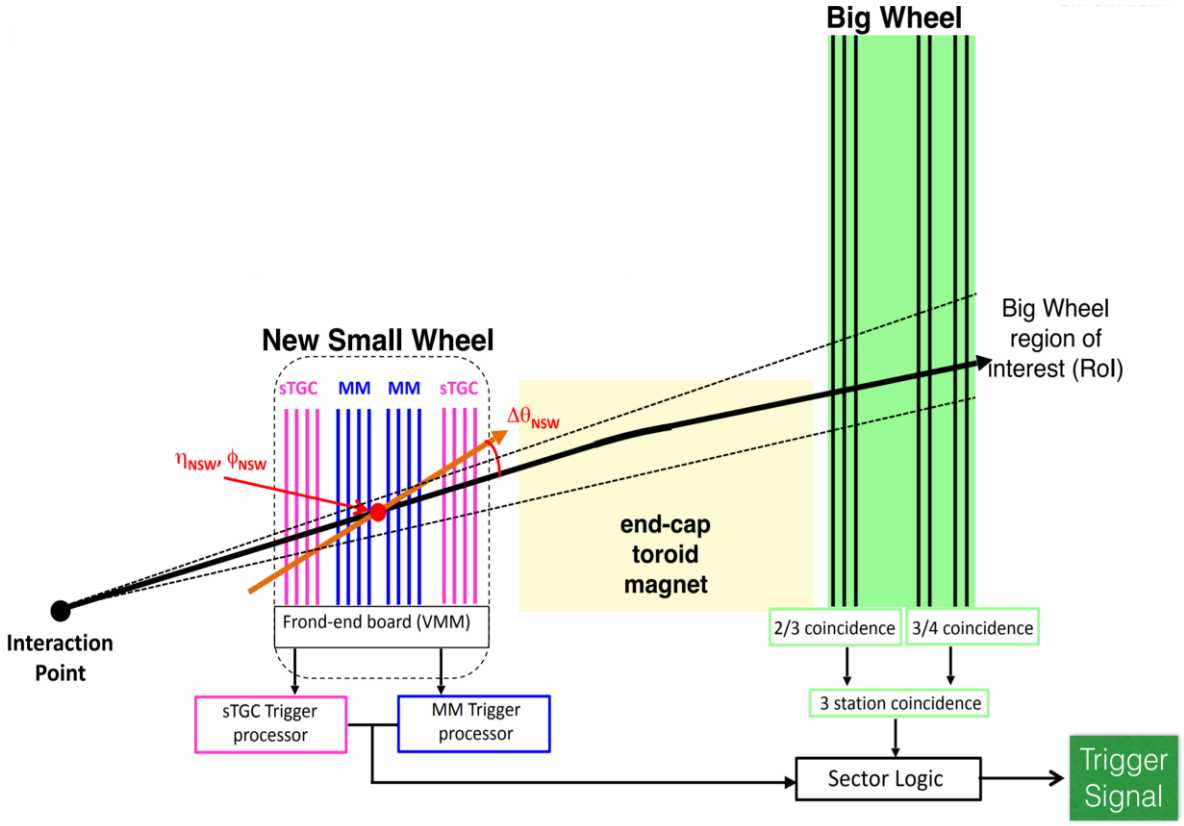
SCA ASIC

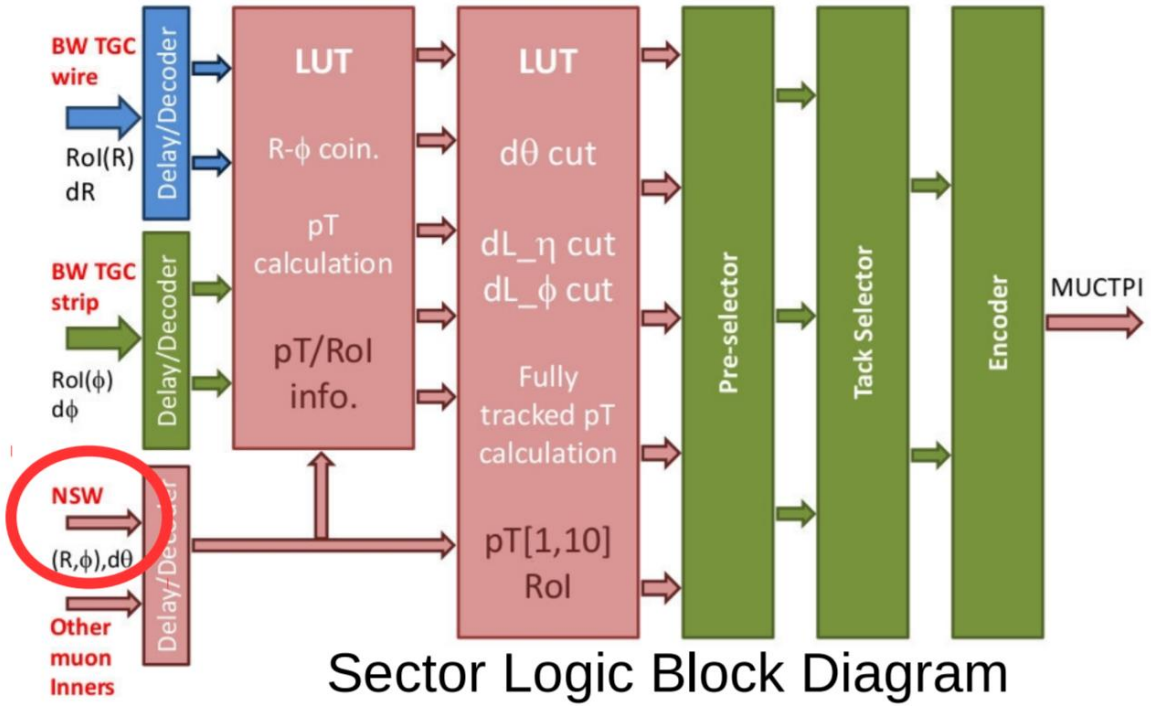
- Interfaces with the GBTx via E-link at a speed of 80 Mb/s, over the HDLC protocol
- Configuration all the ASICs and FPGAs on NSW boards(FEB,Pad Trigger,Router,ADDC,L1DDC etc)
- Configures chips over I2C (ROC,TDS,ART), SPI (VMM), JTAG (FPGA)

GPIOs for Reset,Mode Select and Error Monitoring

- ADCs for calibration, current and temperature monitoring etc

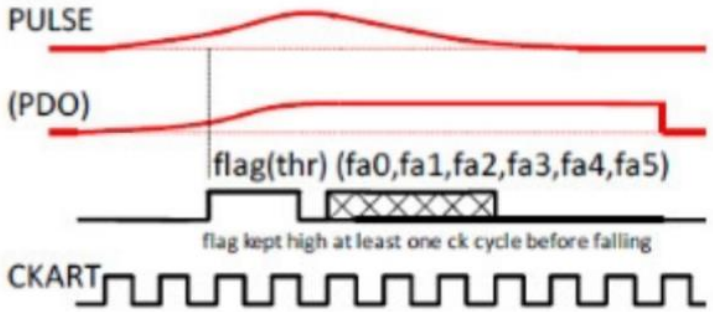
Sector Logic



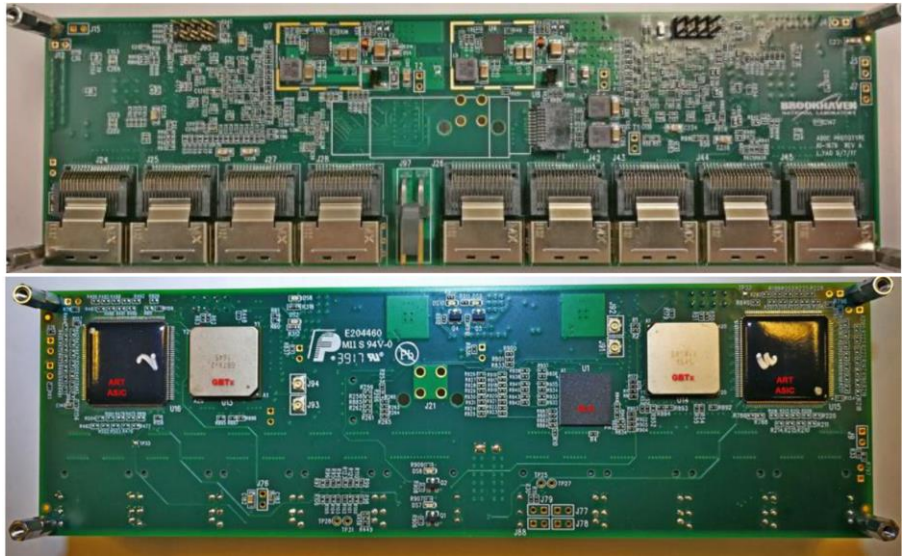


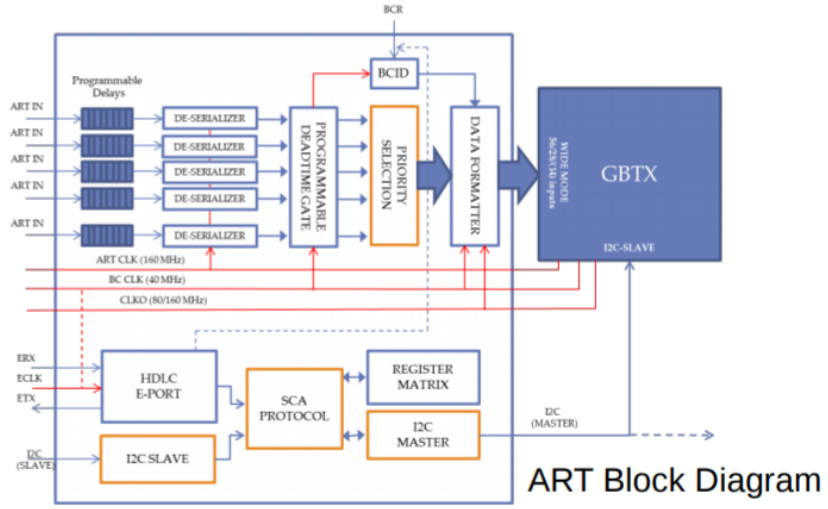
- The NSW muon candidates are sent to the Sector Logic to confirm muon candidates found in other muon detector(eg. Big Wheel)
- 1016 ns latency from initial p-p collision to NSW TP sending out the segments

ART and ADDC



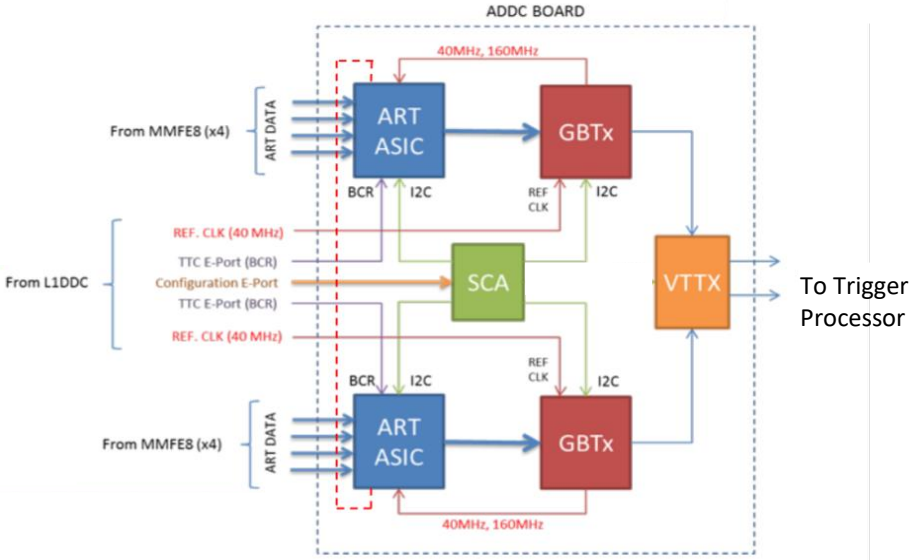
In VMM's Address-in-Real-Time (ART) mode, VMM will send out the address of the first strip that crosses threshold





ART Block Diagram

- ❑ The ART stream is sent to the ART ASIC at 320 Mbps.
- ❑ ART ASICs aggregates strips addresses from 4 MMFE8s (32VMMs)
- ❑ The ART formats a packet with up to 8 hit addresses + 5-bit VMM geographical addresses + BCID to trigger processor via GBTx

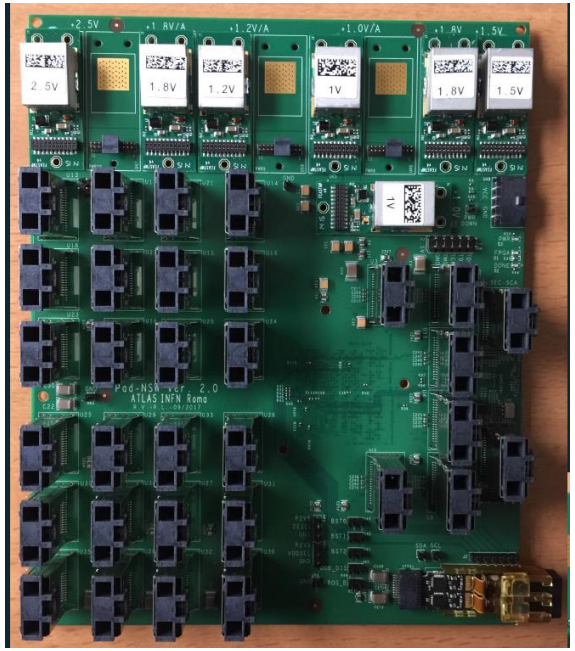


ADDC(ART Date Drive Card):

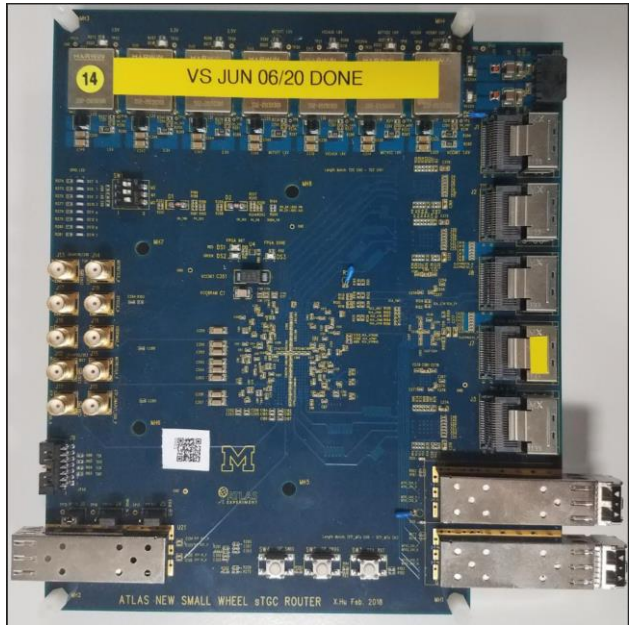
- ❑ incorporate 2 ART, GBTx and transmit data using optical link (CERN VTTx)
- ❑ 2 ADDC per layer

Pad Trigger and Router

Pad Trigger



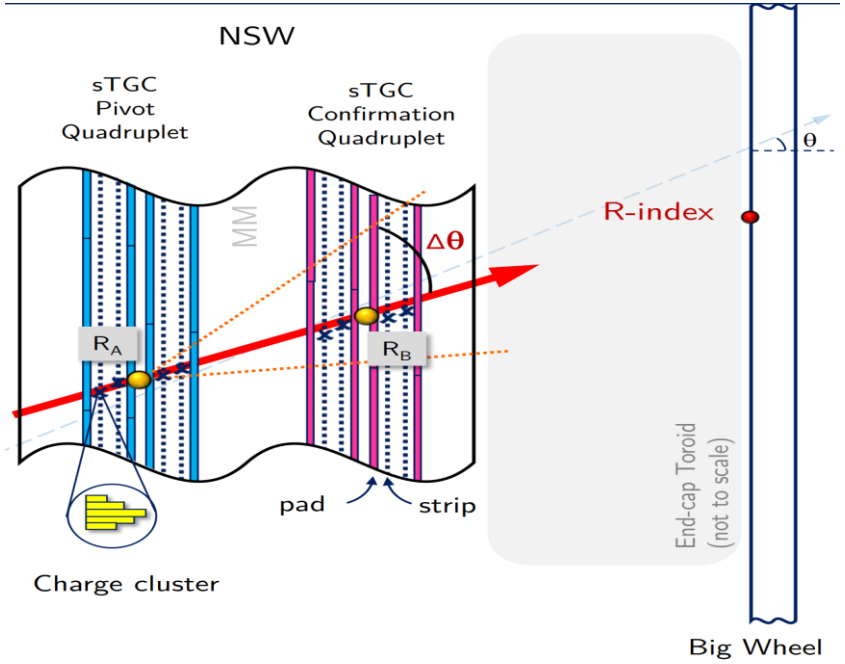
Router

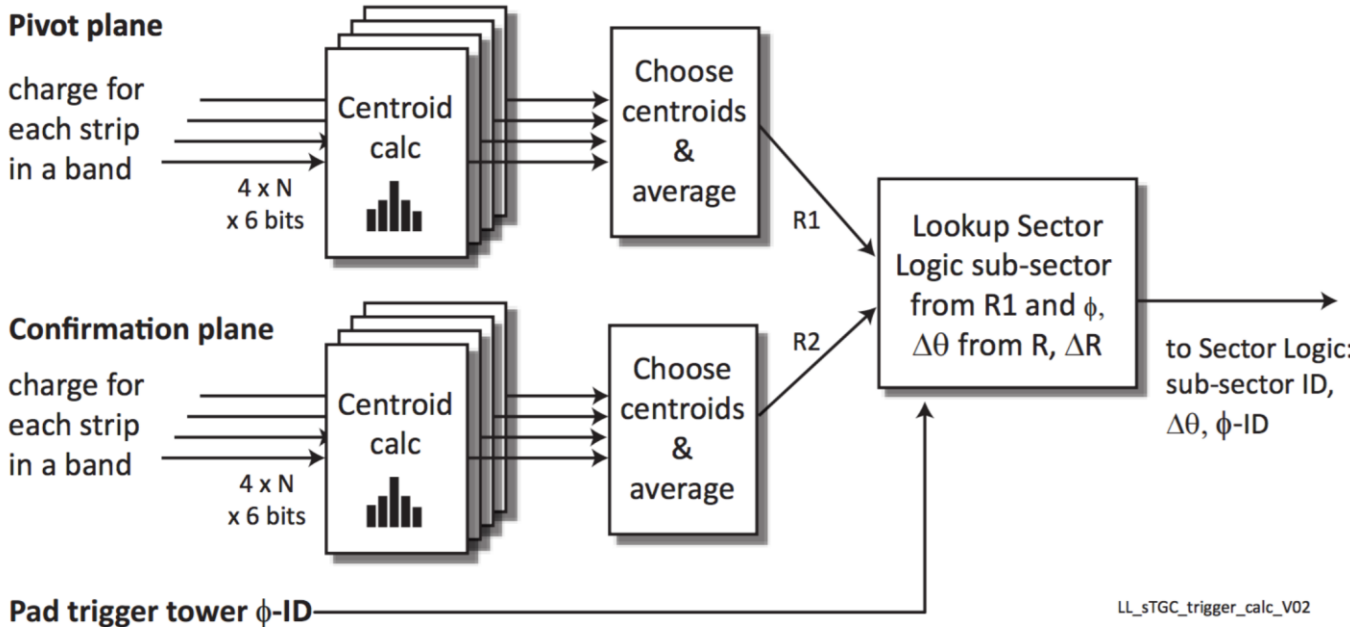


- Functionality: Two 3 out of 4 pad coincidences per BC to form pad trigger road (tag BCID, define strip band to be read out)
- 1 board per sector
- Inputs:6 cables,24 pad-TDSs at 4.8 Gbps
- Outputs:24 cables,24 x 7 lines at 640 Mbps to sFEB,including 320 MHz clock,trigger enable, trigger BCID and trigger band-phi ID
- trigger optical data to NSW trigger processor

- Functionality: Collect data packets from active TDSs and transmit data to trigger processor
- 1 board per detector layer per sector
- Input: from 9 strip-TDSs per plane, each at 4.8 Gbps
- Output: 4 fibers (Up to 6.4 Gbps per link with baseline FPGA)

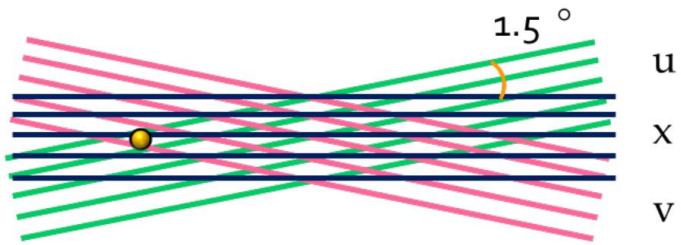
sTGC Trigger Processor Algorithm



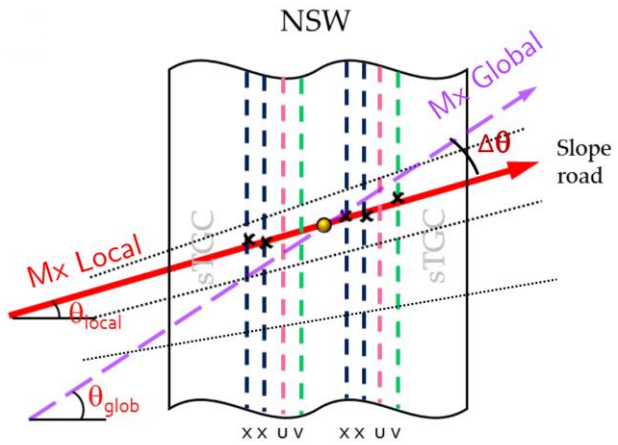


- ❑ Layer centroid calculated using strip charges on each sTGC layer
- ❑ Two quadruplet centroids(averages centroids) calculated to define the segment pointing(Δθ)
- ❑ R-index calculated based on pivot quad. Centroid and segment pointing
- ❑ ϕ-index directly available from pad trigger

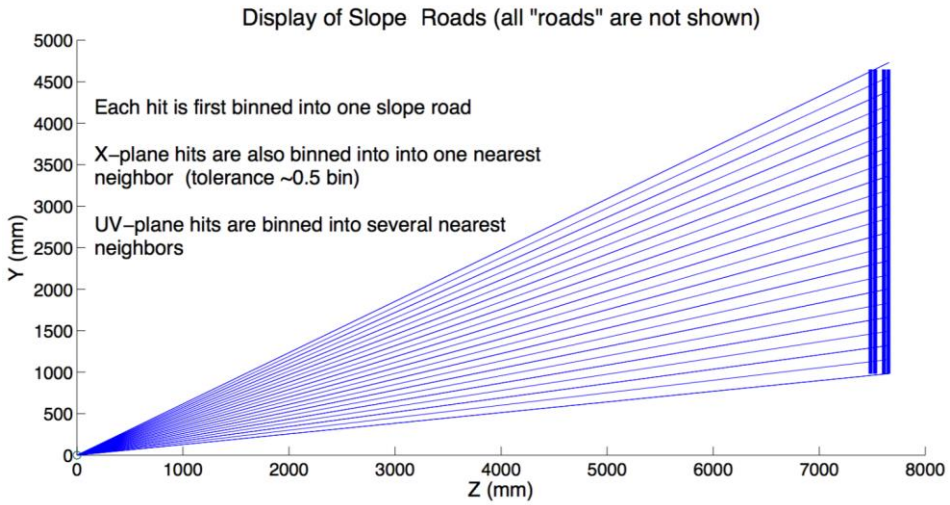
MM Trigger Processor Algorithm



x: horizontal strip (2 plans per quad.)
u,v: stereo strip (1 each per quad.)



- Global slope: average of x/u/v slopes
- Local slope: least square fit of x plane slopes (n=2,3,4)



- ❑ Translate hit addresses into slopes by dividing detector into “roads”
- ❑ Use circular buffer to look for coincidences between the roads
- ❑ Calculate local and global slopes for track candidates using LUTs