# The End-of-Substructure (EoS) card for the Strip Tracker Upgrade of the ATLAS experiment


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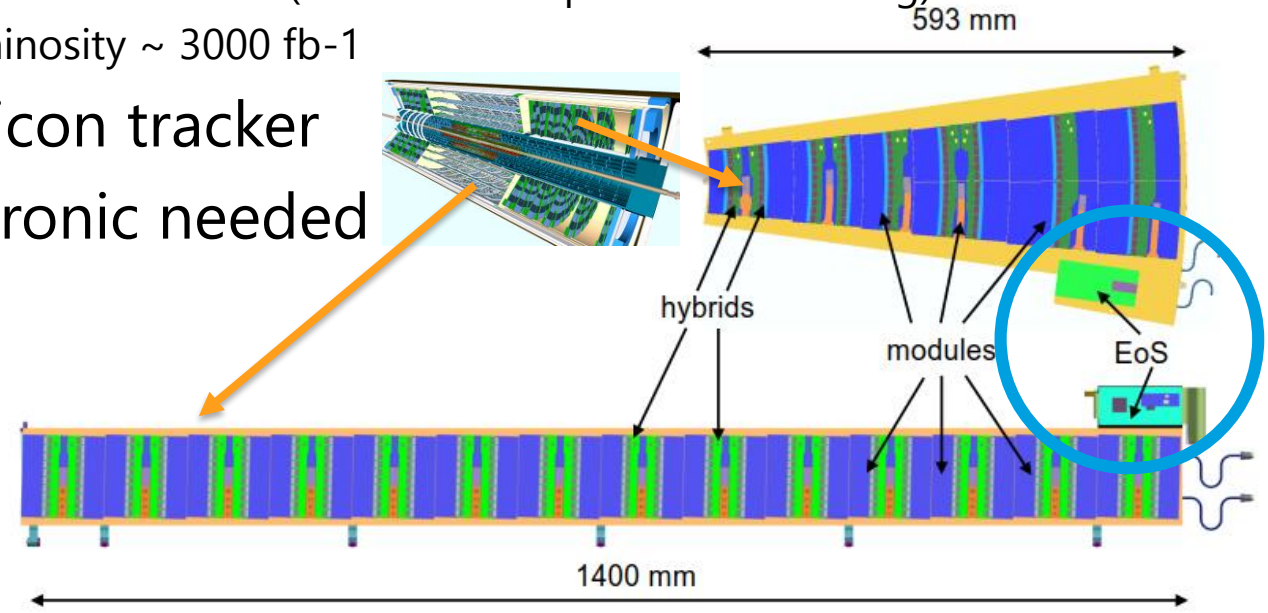
on behalf of DESY EoS Team

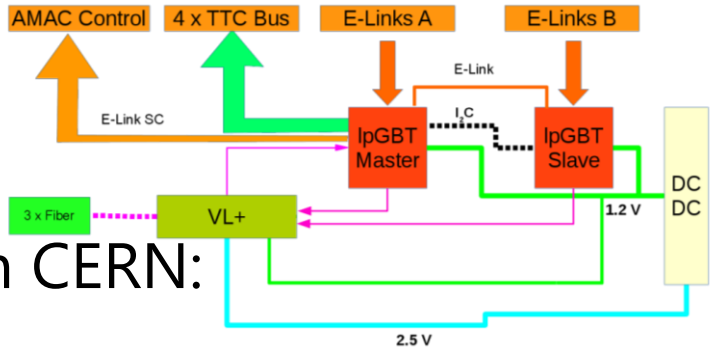
# ATLAS ITk Upgrade

- HL-LHC will be a very harsh environment for ATLAS inner tracker (ITk)
  - Peak luminosity ~ $7.5 \times 10^{34}\ cm^{-2}s^{-1}$ (200 collisions per bunch crossing)
  - Lifetime integrated luminosity ~ 3000 fb-1
- New, upgraded silicon tracker
- New readout electronic needed
  - Faster
  - Less materials
- Two geometries
  - Stave for barrel
  - Petal for endcap



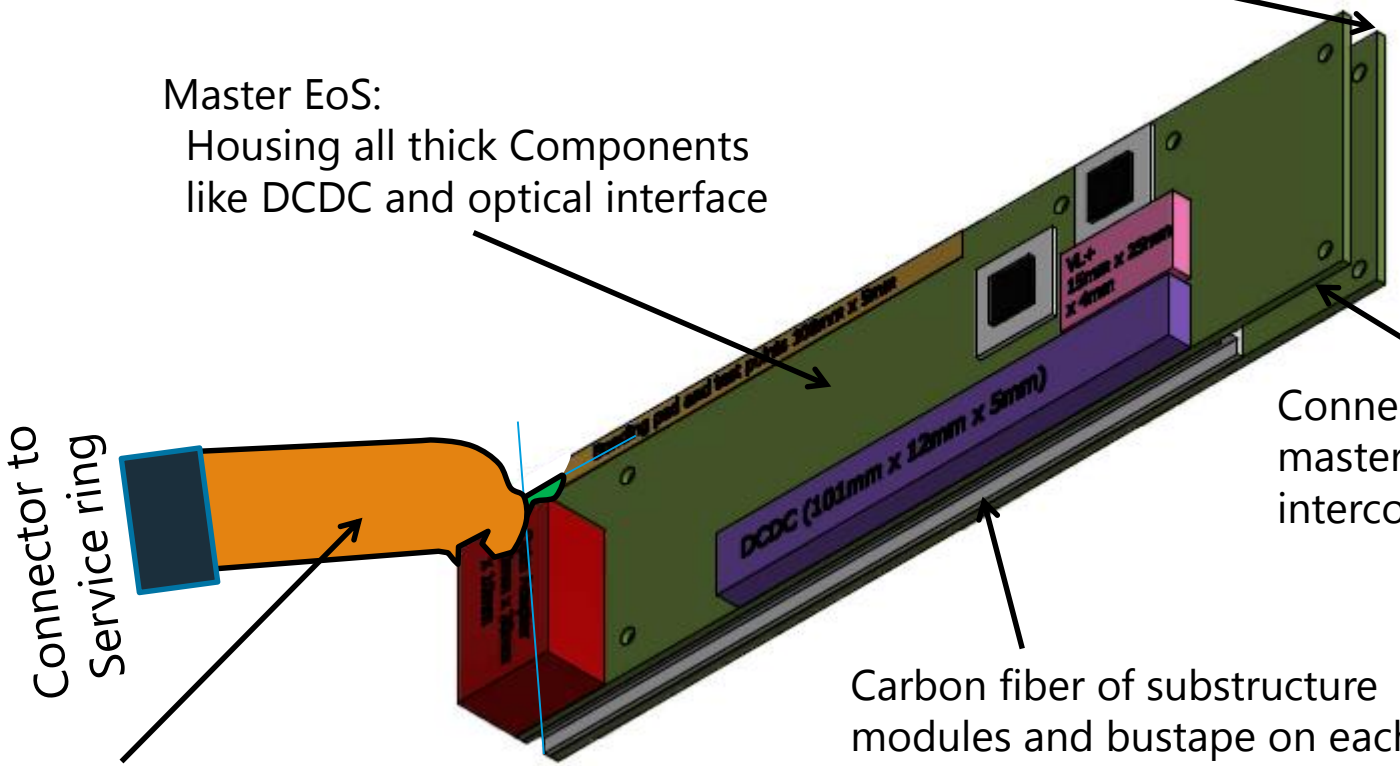

- End of Substructure (EoS) card
  - Sit on the "ear" of stave and petal
  - Act as the interface between on- and off-detector components
  - Handle data, command, and power delivery
    - Upstream: Up to 28 "Elinks" @ 640 Mbit/s
    - Downstream: Clock and control data stream for front-end ASIC
    - Both Low (LV) and High (HV) Voltage delivery

# EoS Card

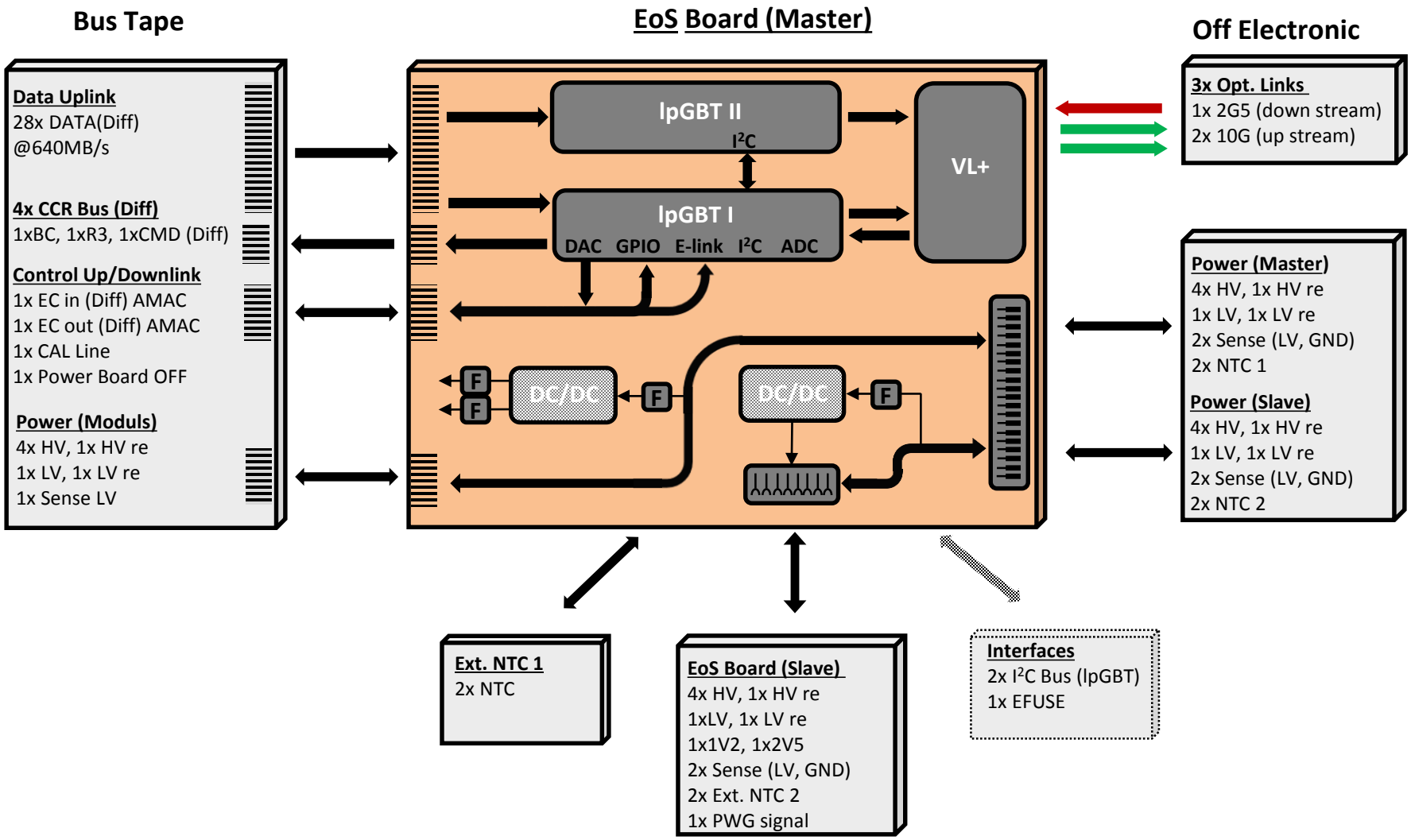



- Major radiation-hard components from CERN:
  - Low-power Gigabit Transceiver (lpGBT) ASIC
  - Bi-directional optical link (VL+)
  - DCDC convertor (BPOL12 and BPOL2.5)
- Multi-layer board using industry-standard PCB technology.
  - Nominal thickness 1.6 mm, maximum 1.8 mm
  - Total height < 5 mm (constrain from detector design/assembly)
- Two variants called the “Master” and the “Slave”
  - Glued to the each side of the mechanical structure (see next slide)
  - Connected at one end
  - 1 or 2 lpGBT each and a VL+ each
- Master will house the think components
  - Fiber interface
  - DCDC converters
- Flex cable for common power and external monitor connector
  - In the slave for barrel, master for petal

# EoS Card


Slave EoS with only
thin components
Master EoS:
Housing all thick Components
like DCDC and optical interface
Connector for
master-slave
interconnect
Connector to
Service ring
DCDC (101mm x 12mm x 5mm)
Carbon fiber of substructure
modules and bustape on each side
Flexible connection
to Service ring with
connector to PP0
either on master or slave

# Schematic


Bus Tape
Data Uplink
28x DATA(Diff)
@640MB/s
4x CCR Bus (Diff)
1xBC, 1xR3, 1xCMD (Diff)
Control Up/Downlink
1x EC in (Diff) AMAC
1x EC out (Diff) AMAC
1x CAL Line
1x Power Board OFF
Power (Moduls)
4x HV, 1x HV re
1x LV, 1x LV re
1x Sense LV
EoS Board (Master)
lpGBT II
I²C
lpGBT I
DAC GPIO E-link I²C ADC
VL+
F
DC/DC
Off Electronic
3x Opt. Links
1x 2G5 (down stream)
2x 10G (up stream)
Power (Master)
4x HV, 1x HV re
1x LV, 1x LV re
2x Sense (LV, GND)
2x NTC 1
Power (Slave)
4x HV, 1x HV re
1x LV, 1x LV re
2x Sense (LV, GND)
2x NTC 2
Ext. NTC 1
2x NTC
EoS Board (Slave)
4x HV, 1x HV re
1xLV, 1x LV re
1x1V2, 1x2V5
2x Sense (LV, GND)
2x Ext. NTC 2
1x PWG signal
Interfaces
2x I²C Bus (lpGBT)
1x EFUSE

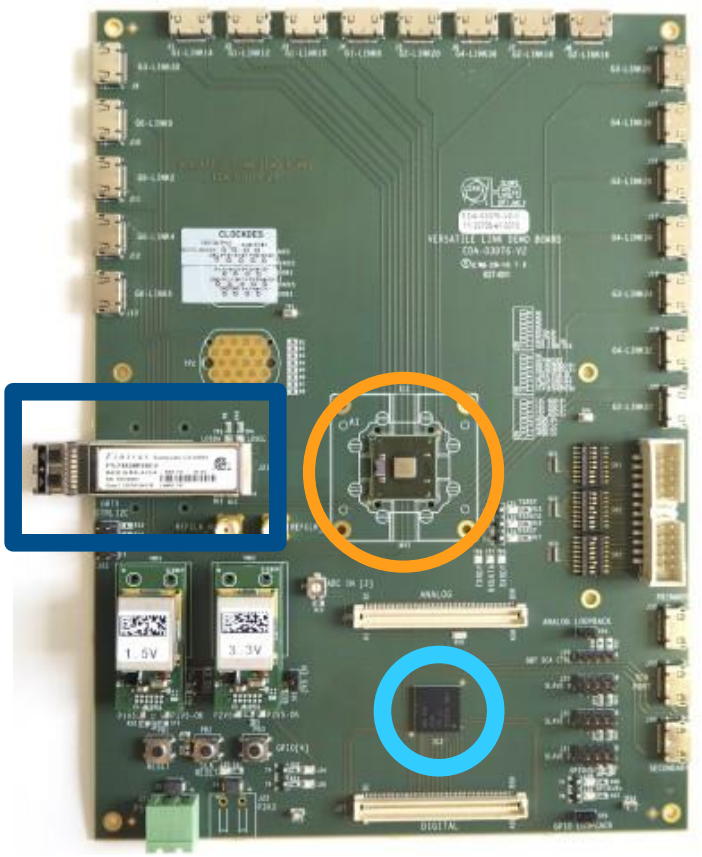
# GBTx-based Prototype

# EoS Prototype

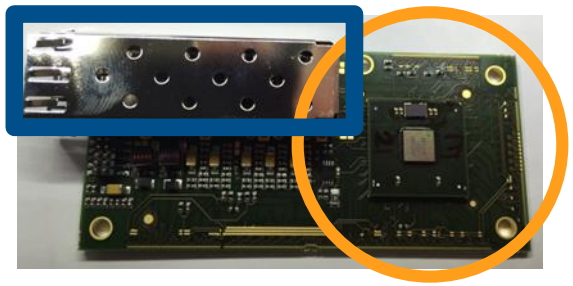
- The EoS will use lpGBT chip, but it is not yet available
- We built GBTx-based prototypes to learn about implementing the hardware and software
  - We won't learn everything since lpGBT is different
  - Unlike lpGBT, GBTx is accompanied by an ASIC decicated to slow control called GBT-SCA
  - Built both master and slave cards
- The laser component, VL+, is also not yet available
  - We use industry standard SFP+ for prototyping
  - The height of SFP+ is over the limit but can be ignored

# Evolution of the Prototypes

VLDB



Test daughterboard

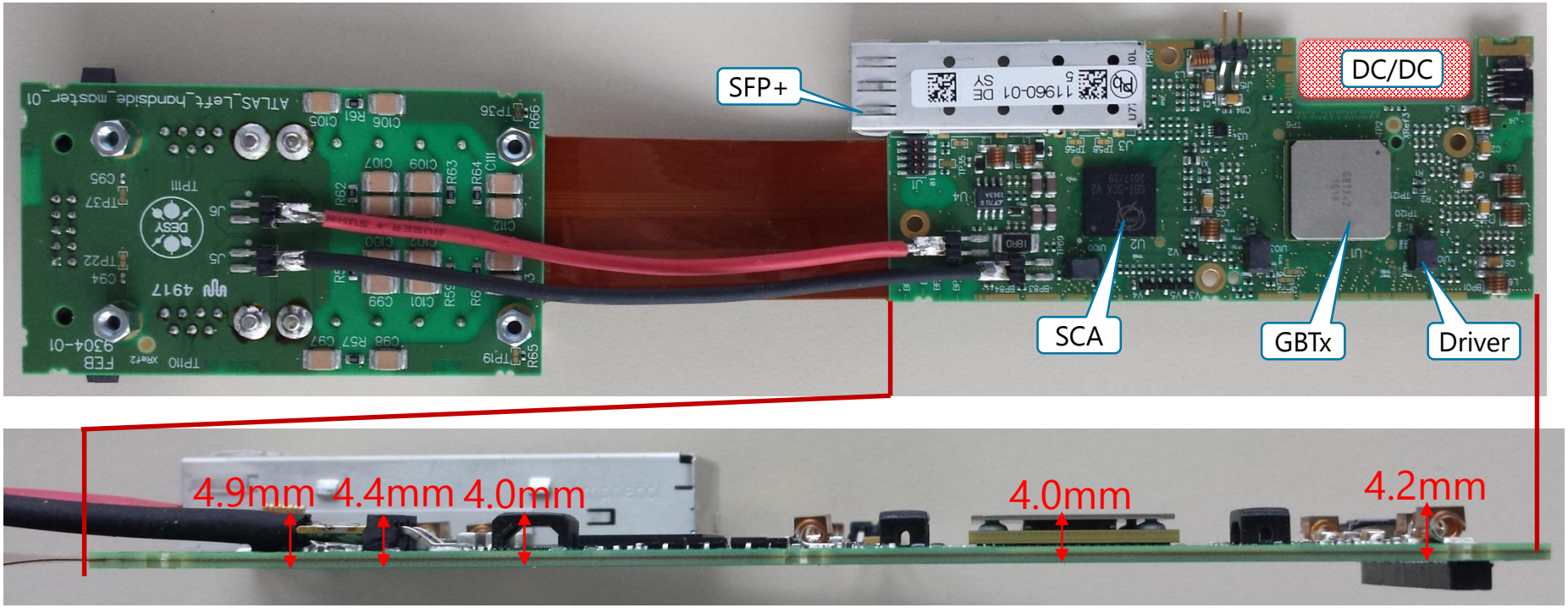


GBTx
GBT-SCA
SFP+

- We started from VLDB board, which is CERN reference design
  - Also hosted the GBT-SCA for slow control, whose functionalities will be integrated into lpGBT
  - VLDB is a fallback reference in case we run into a problem with our prototypes
- Next, we built a simple test daughterboard, hosting GBTx and SFP+
  - We no longer use it, but still make them for other teams to get started on the GBTx chip

Current Prototype

# Master Board




- So far, we built a total of 23 master boards
  - 3 of them are version 0
- We have 20 of the latest version 1
  - Current tallest component is at 4.9 mm, including the PCB
  - All I/O channel can run up to 320 Mbps

Current Prototype

# Slave Board


- For slave board, we built a total of 12 boards
- 2 are version 0
- We have 10 of the latest v.1

# Things We Learned

The current (v.1's) prototypes have no outstanding issues, but we've learned quite a lot while building them

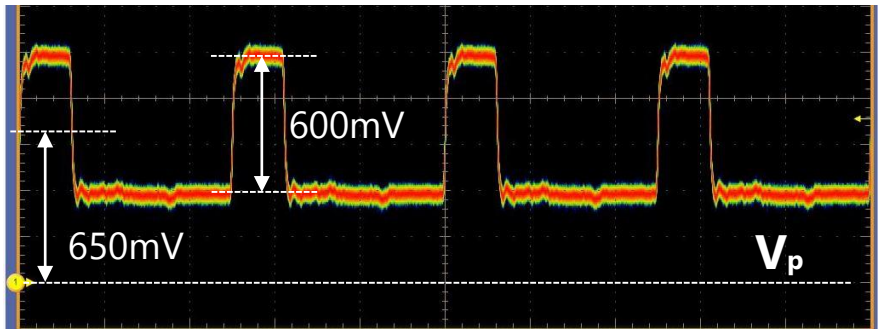
- Wrong pull-up for the SFP+
  - Passive (copper) cable is a good thing to check if optical one doesn't work
- Mistakes on connections between GBTx and SCA
- Wrong resistors
  - Stricker design rule will check and make sure these are correct in the future
- PCB manufacture can made bond pads with too small pad size, serious over-etching (!?)
  - We will perform visual inspection to catch this
- Elink channels have to be carefully selected
  - Some are not available at high speed mode

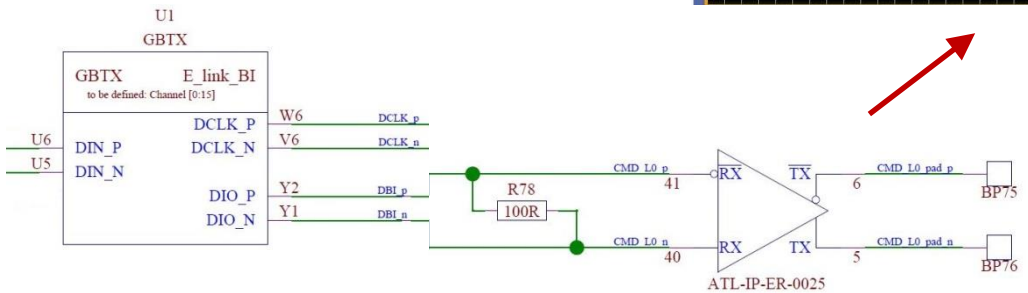
# Functionality Test

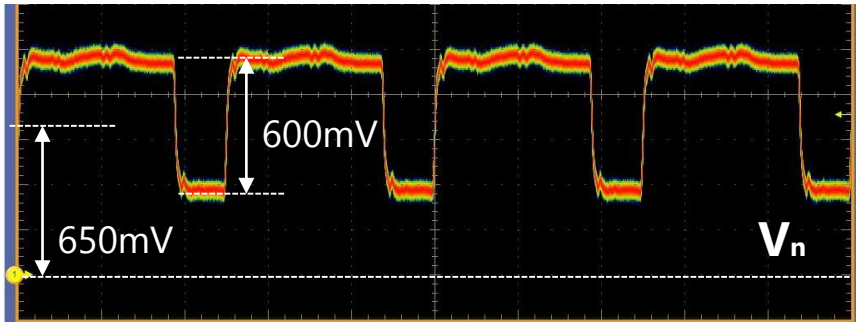
We developed both firmware (FPGA) and software (PC) for testing the boards

- Isolation resistor HV lines
- Line resistor HV, LV, NTC
- Electrical strength, residual current HV lines @ 1.5kV for 60 sec
- Current on LV and 1V5
- Common mode voltage at output driver
- Fast control Signals (CCR) and AMAC down ($V_{CM}$, $V_{DIFF}$, $I^2C$)
- Test of all data input ports
- GBT-SCA:
  - Read SCA's ID
  - SCA's built-in $I^2C$ Bus
  - GPIO
  - ADC and DAC channel

# CMD Signal (E-Link)

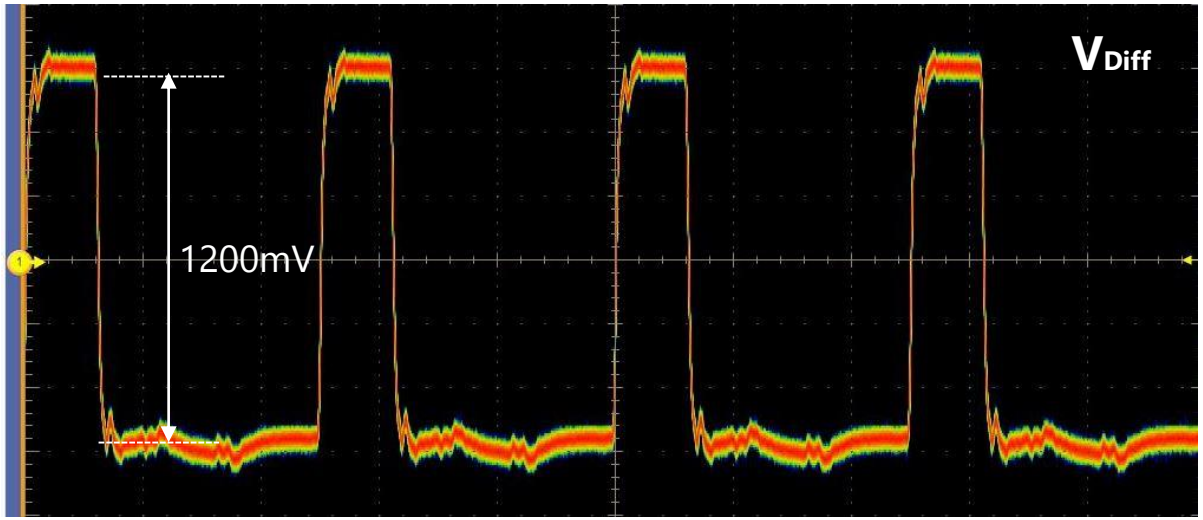


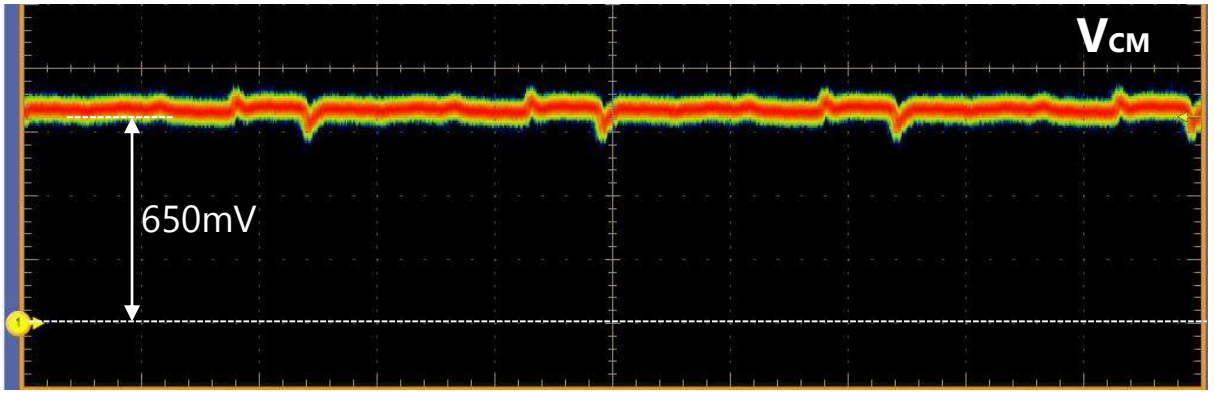




- Sending “0001” @ 40 MHz (160 Mbps)

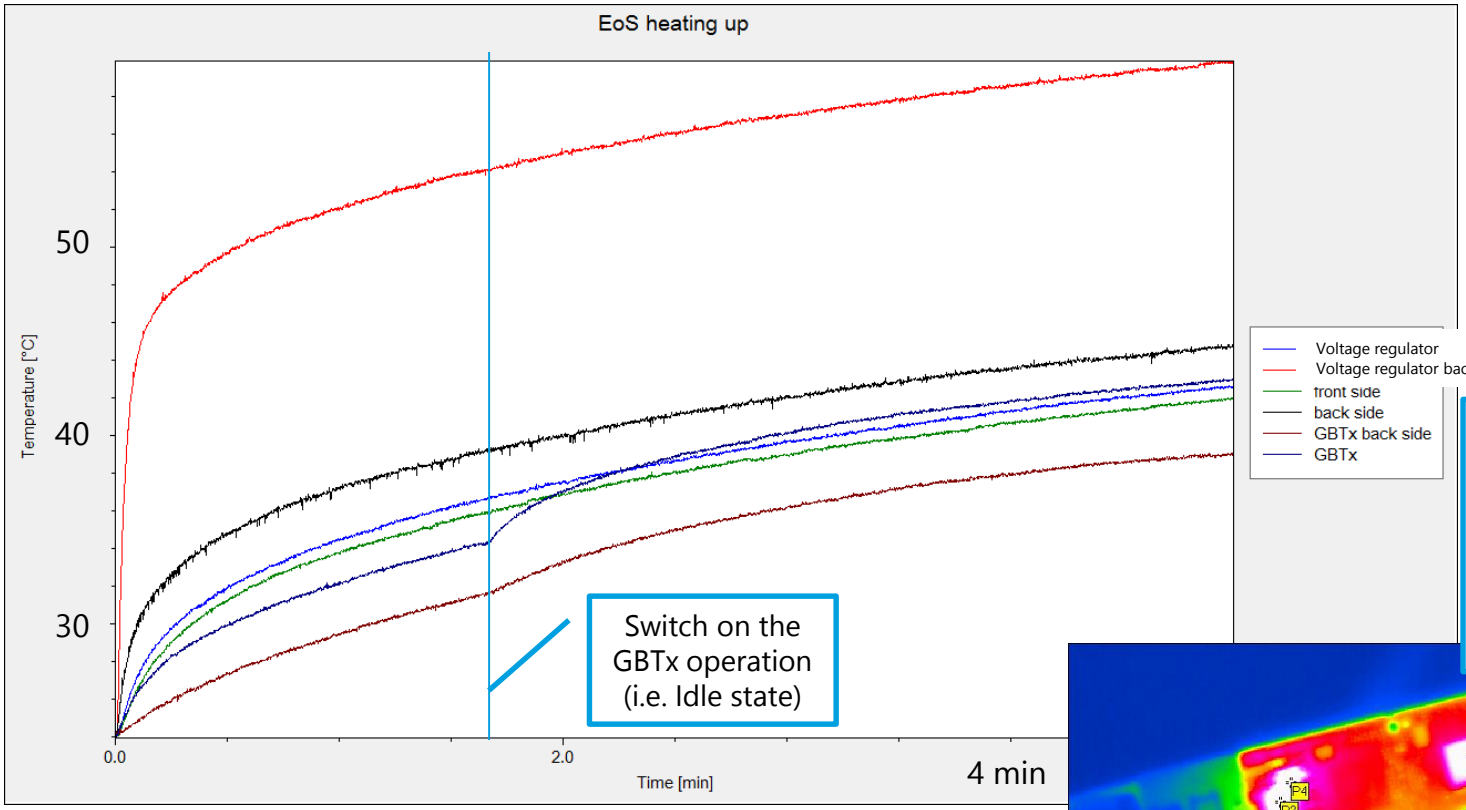
# CMD Signal (E-Link)



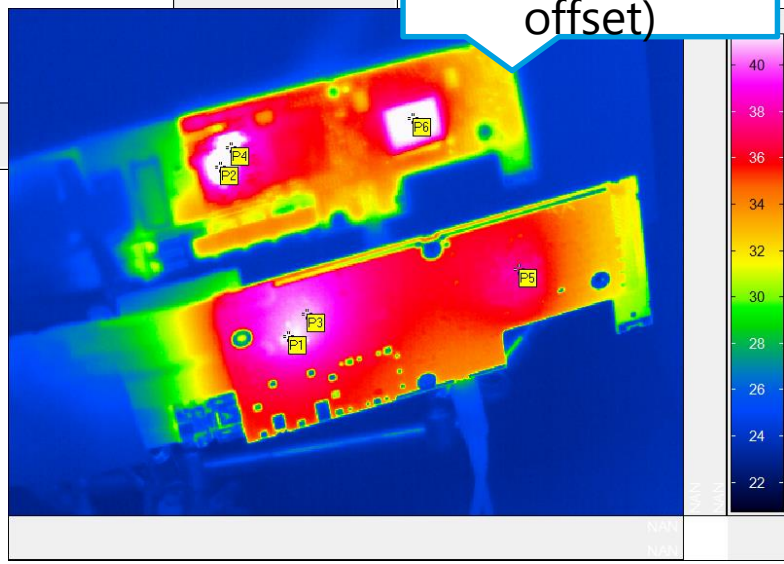




- Sending “0001” @ 40 MHz (160 Mbps)

# Thermal Test




The front side is measure from a mirror (need a temperature offset)

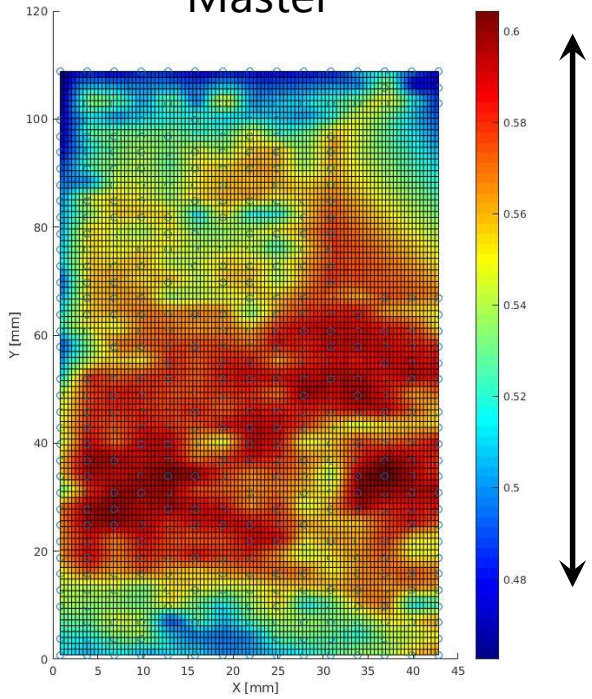



- No enforced cooling
- The PCB is a good heat spreader
- GBTx warm up pretty quickly after powered on, which is ok

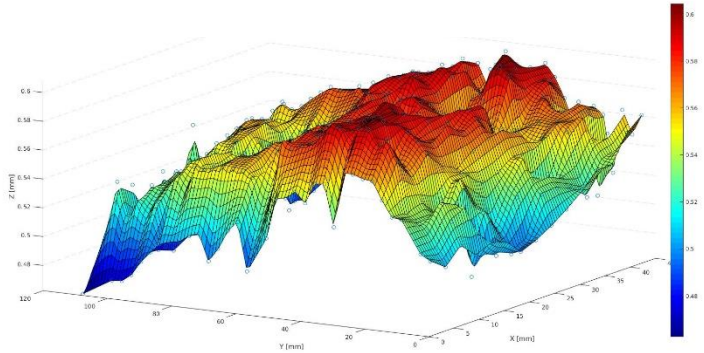
# Flatness Test

- Measure the flatness of fully populated master and slave board

Master

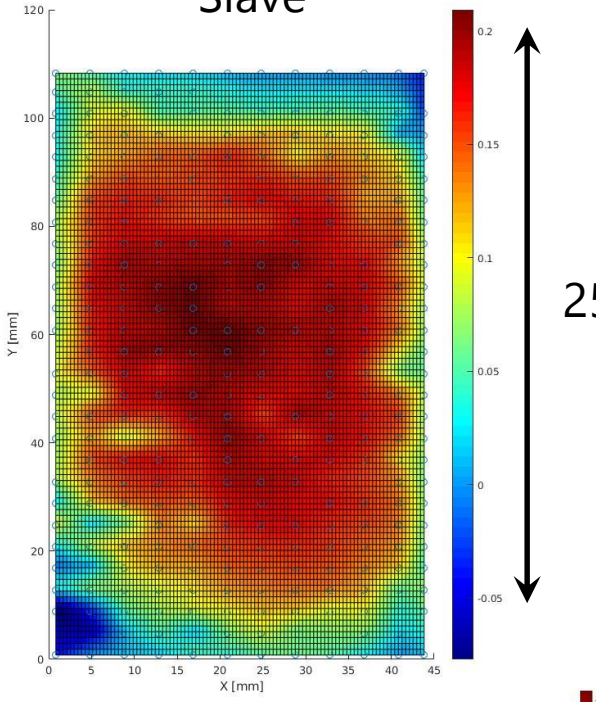



120μm

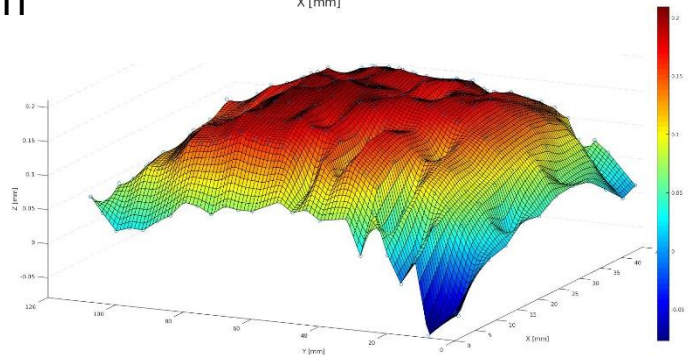


Corners are a bit thinner, not a problem for cooling

Slave

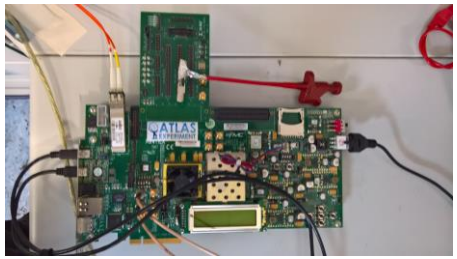


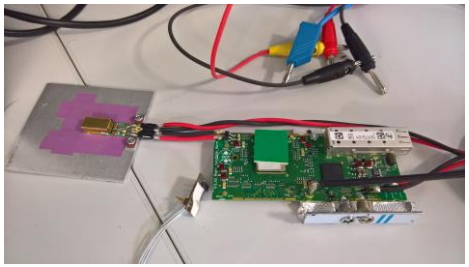

250μm



# Bit Error Rate Test

- We ran a preliminary bit error rate (BER) test
- The tests have the full data path
  - FPGA -> Optical link -> EoS (GBTx) -> Elink -> FPGA
- Ran with various configurations:
  - 160 and 320 Mbps
  - All Elinks on and only the used group on
  - With a metal case around the EoS and without
  - With twisted power cables(12v, 1.5v) and without
  - With a prototype DCDC converter (supply only 12v)

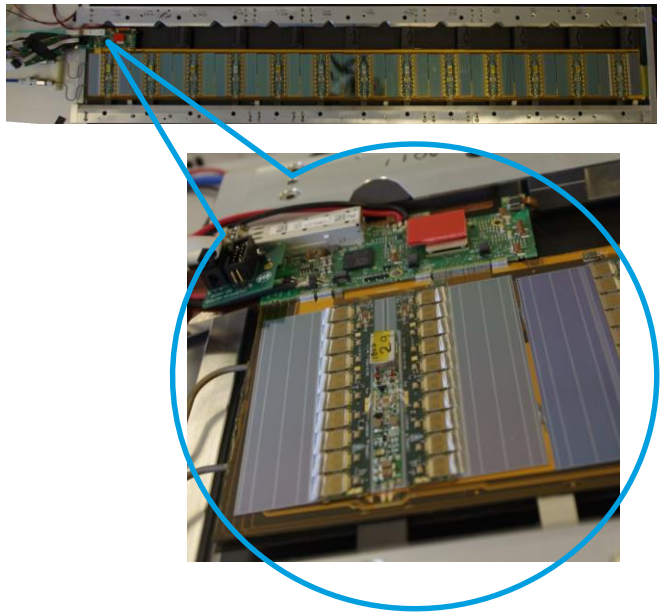


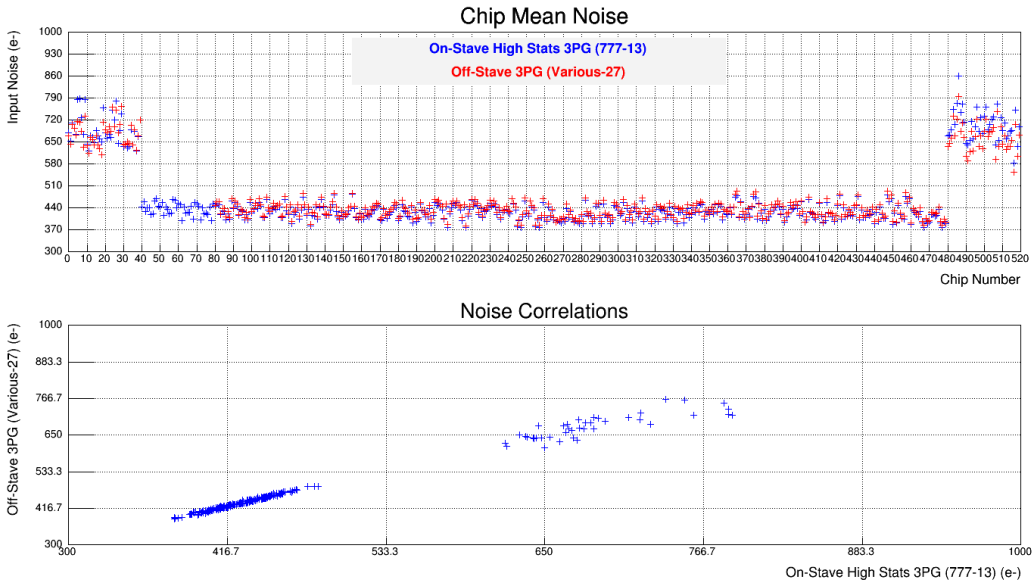


- All tests are more than 15h ($<10^{13}$) error-free
- Two tests were run for ~70h, both with only one Elink group turned on
  - 160 Mbps with metal case and twisted power cables
  - 320 Mbps without metal case and without twisted power cables
- Already better than the aimed $10^{12}$
  - Should be able to do even better with a proper setup

# EoS with Real Stave

- Our colleagues at Rutherford has put a master EoS prototype together with a real stave:
  - Bus tape
  - Full electrical modules at both ends
  - 11 modules with mechanical sensors
- Results:
  - LV, HV supply works
  - Connection to pipe NTC works
    - For temperature interlock
  - Configure and readout all modules correctly
  - Module results on stave consistent with those off stave
- The prototype works!





# Test Plan

- EoS sits on a single point of failure for a large part of the detector => need to be well-tested


- Connectivity
- Optical test of trace width, surface, etc.
- Measurement of test strips (resistivity/impedance)

- Resistivity, Impedance
- Optical Inspection:
  - Trace width
  - Missing pads

- X-ray
- Optical Inspection:
  - Assembly
  - Traces
  - Outer row of BGAs
- Impedance and current measurements

- Mechanics
- Current consumption
- Initialization
- Temperature test
- HV line test
  - 1.5 kV for 60s

- LV/HV line resistor
- Current consumption @ Boot/Init/Min/Typical/ Max of supply voltage
- Infrared imagine
- Reset procedure
- Clock/Control/Data signal
- $I^2C$ Bus/ADC/DAC/GPIO
- NTC
- Bit error rate
- Robustness/Variation
- Noise on power line

# Summary

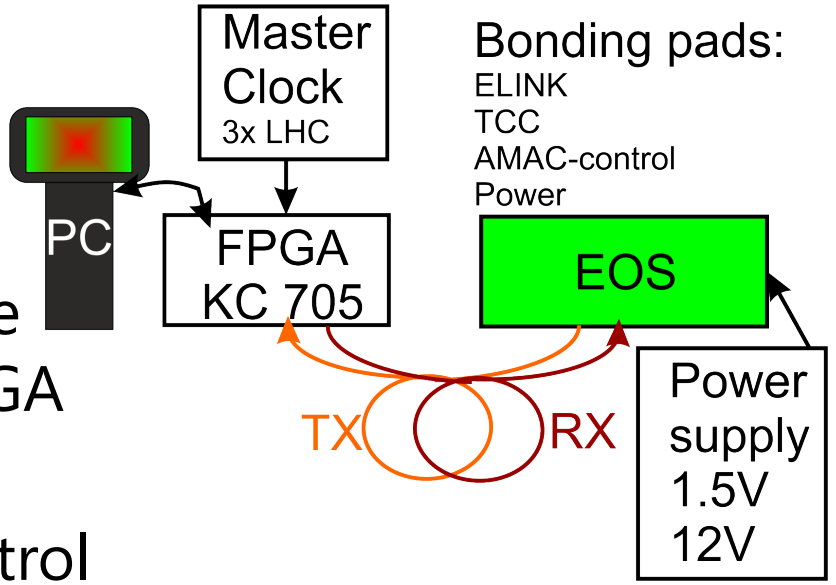
- We built EoS prototypes using available components
  - GBTx instead of lpGBT and SFP+ for VL+
- Learned how to connect and control the chips
- Perform functionality tests to make sure we build them correctly
- Check the thermal and flatness characteristic of our prototypes
- Master prototype has been used and tested with real stave
- Design concept for lpGBT/VL+ based prototypes are ready
- Vigorous tests are planned

Thank you

# Backup

# Test Setup

- The basic setup are:
  - EoS board (VLDB or the prototype)
  - FPGA board (currently Xilinx KC705)
  - PC
- We developed the firmware for the FPGA board based on the GBT-FPGA project from CERN
- We wrote a software on PC to control the testing on FPGA board
  - Currently connected by UART interface
  - Plan to move to faster link as we scale up
- Standalone instead of full ATLAS DAQ system
  - Good enough for our needs
  - Simpler to develop and debug.
  - Can be ready as soon as we have the boards and not rely on other developments

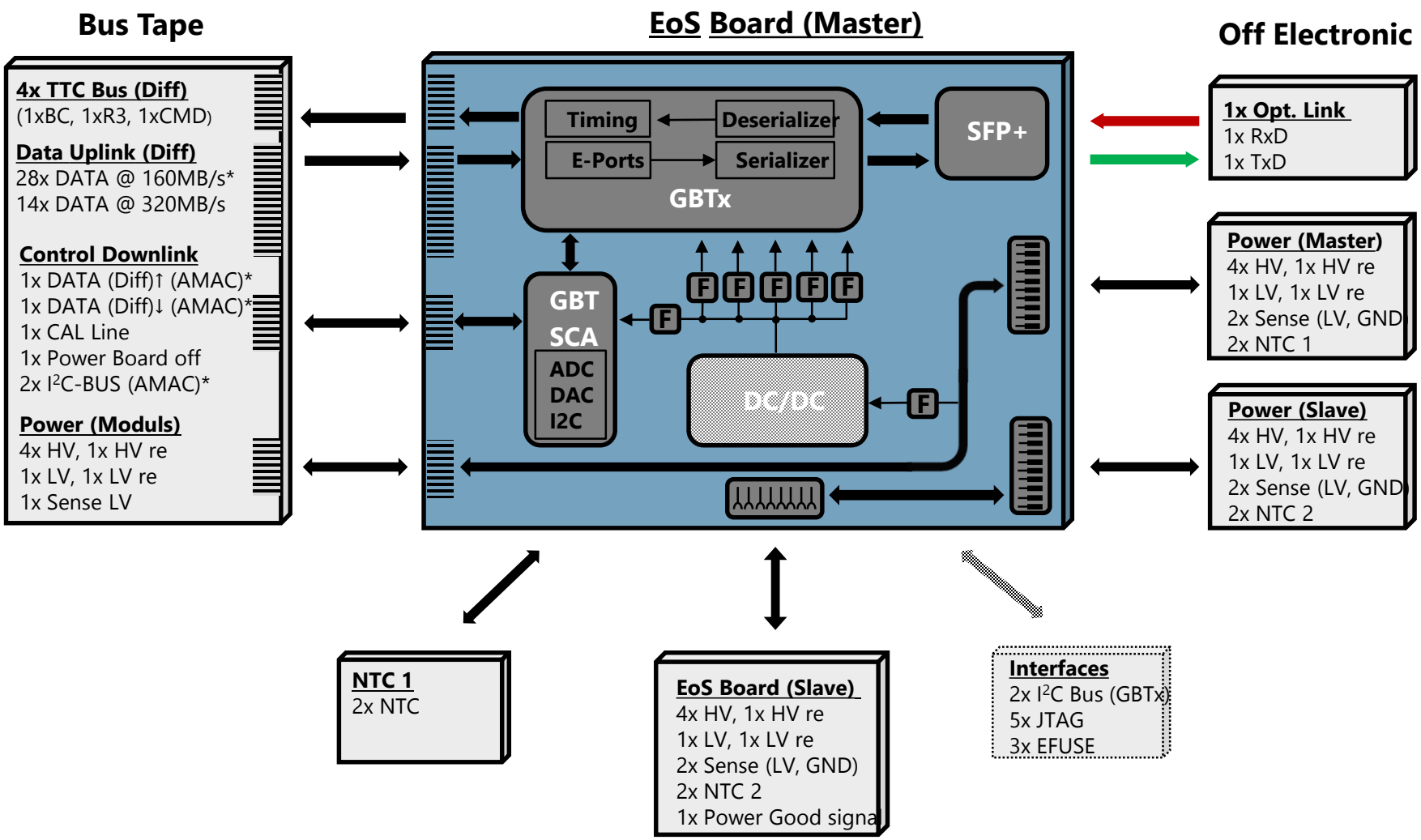



Setup schematic

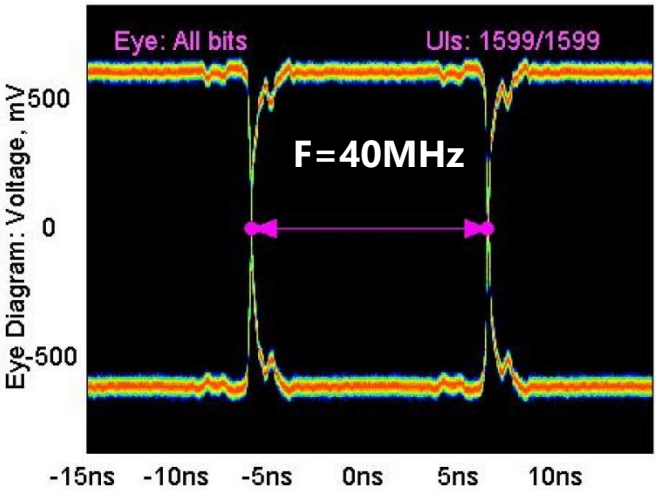
# Firmware and Software

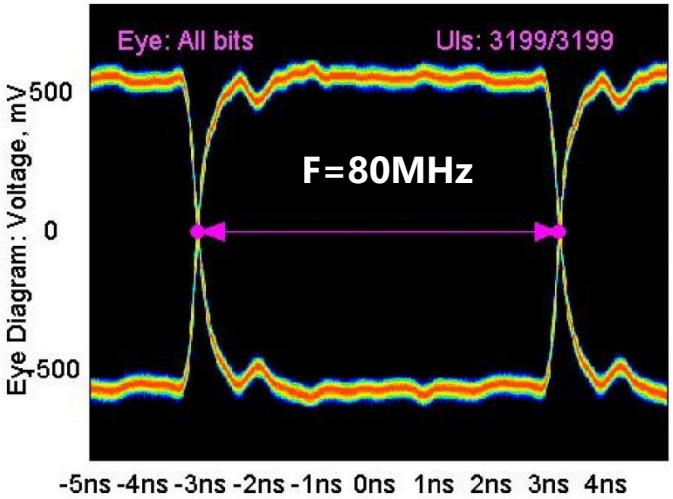
- We first integrated GBT-SC IP core to the main GBT-FPGA example designed
  - Include both external control (EC) to GBT-SCA and internal control (IC) of the GBTx itself
  - Test with VLDB, then try it on our prototypes
- Can do both IC and EC communication
  - Configure the GBTx via the optical link instead of I2C
  - Read the SCA's unique ID and control various functionalities
- Controlling of the FPGA and the SCA chip has been implemented on the PC software
  - Enable us to perform functionality test fairly quickly
  - In the future, automation will be build into the software so anyone can run the test
- Add bit error rate test

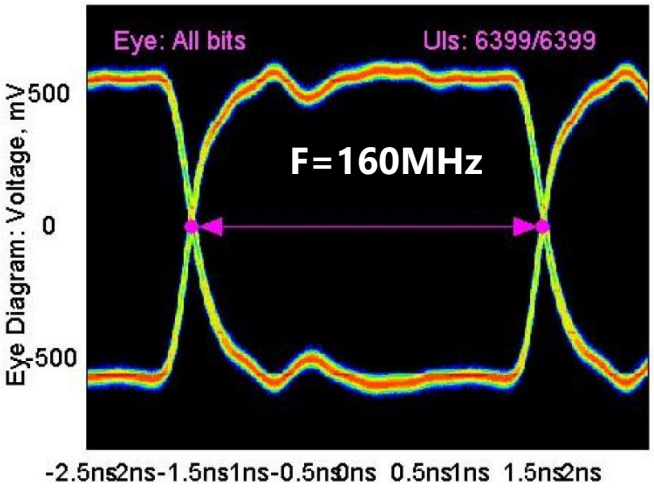
# Schematic Diagram

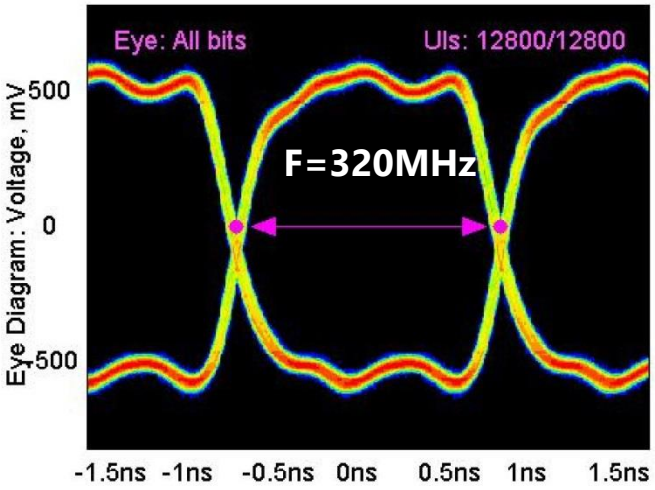


# Bunch Clock Signals ("TTC")

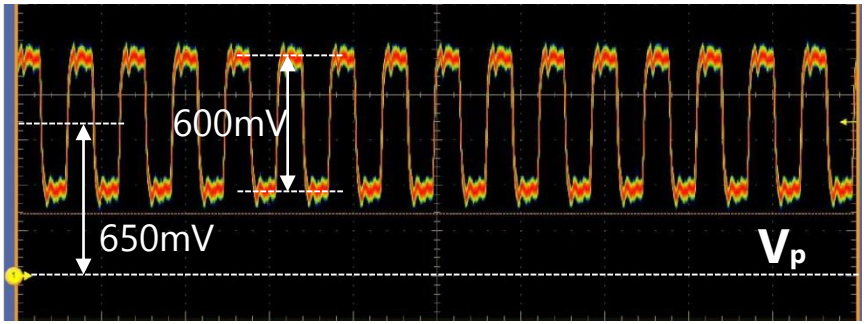


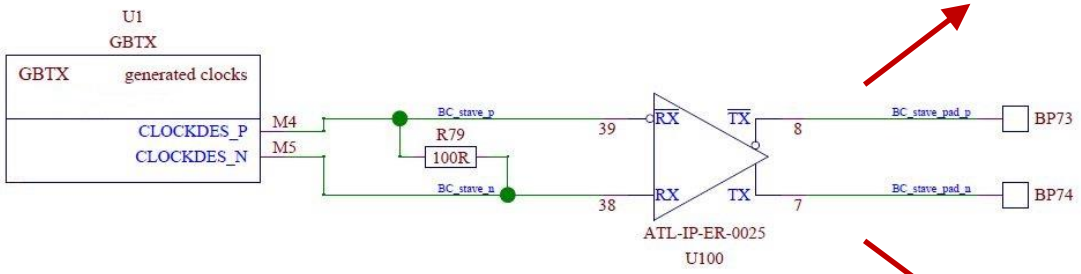



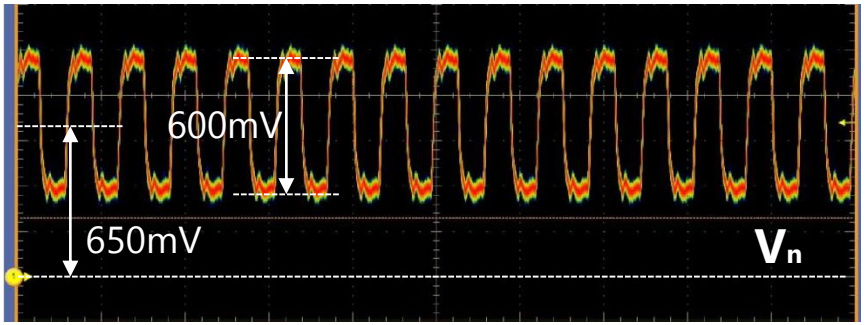



# Bunch Clock @ 160 Mbps



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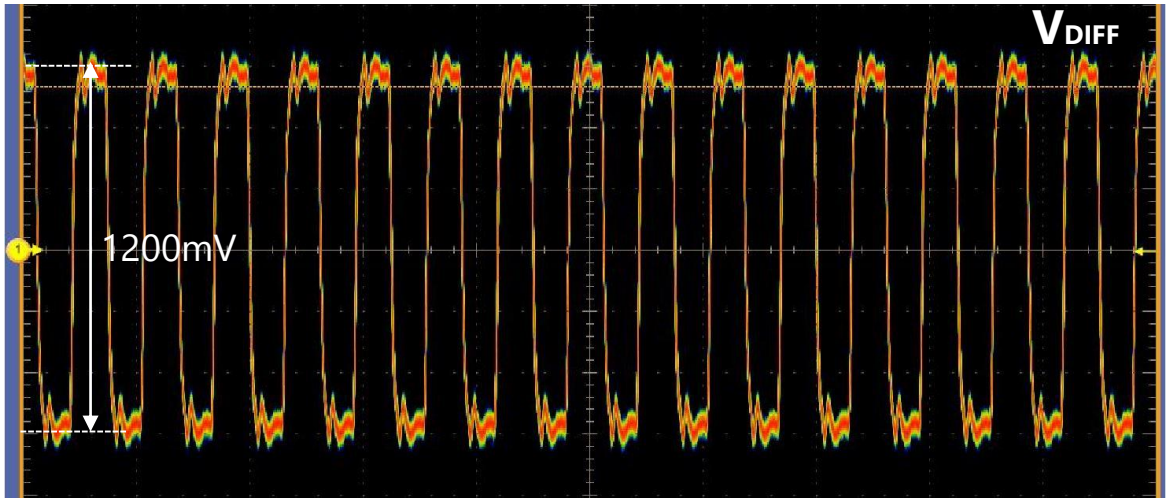
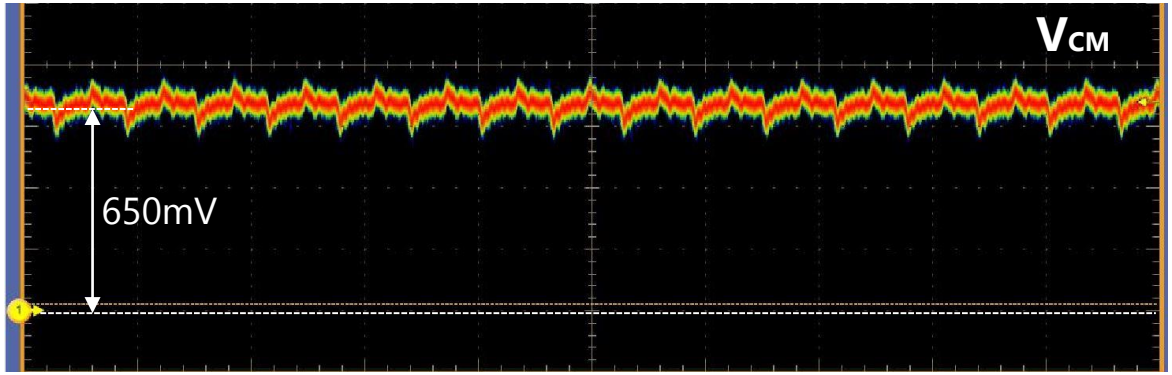
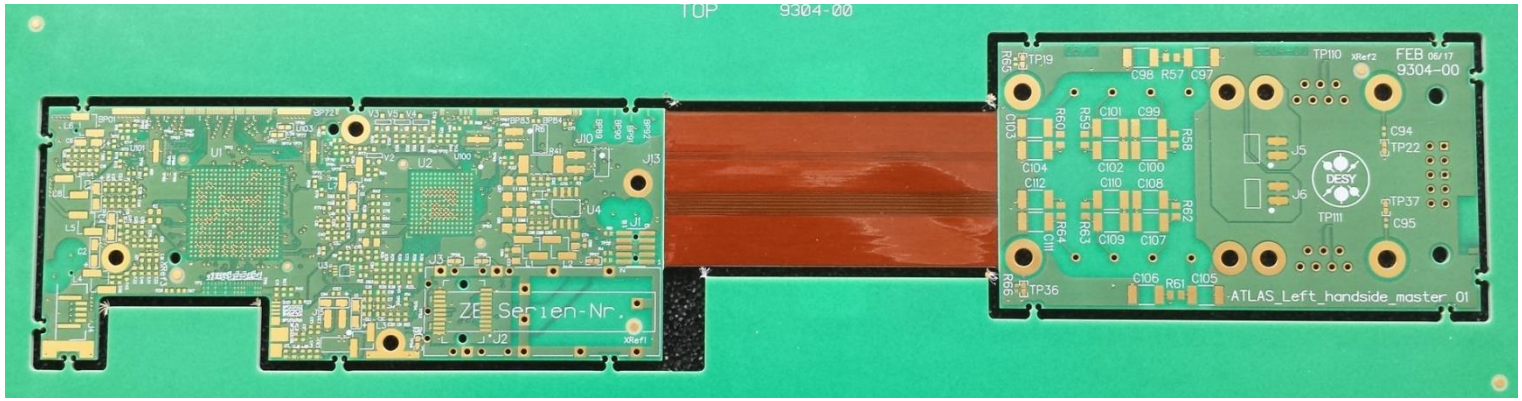


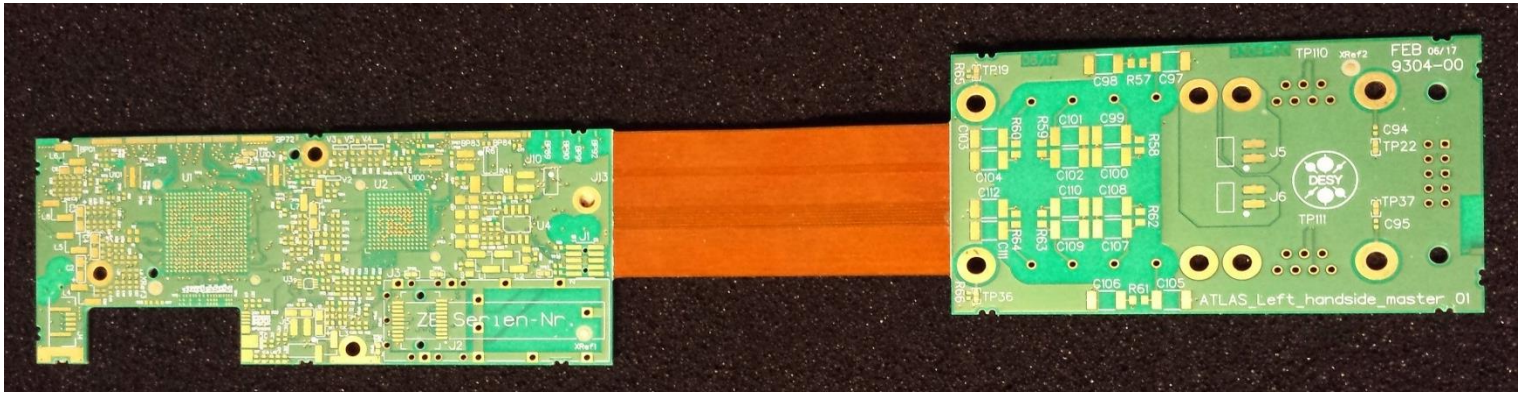



# 1. Manufacturer Tests for unpopulated EoS boards

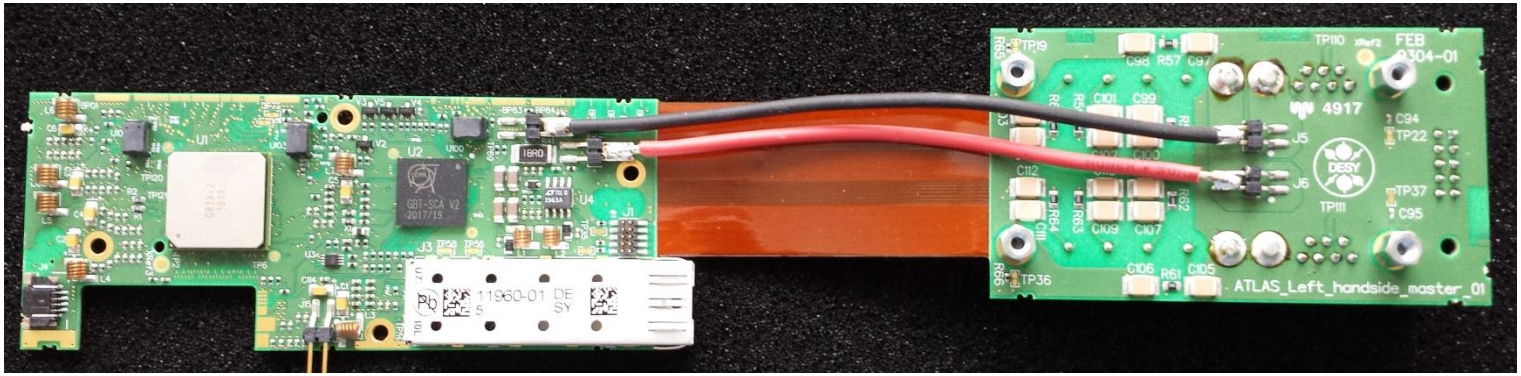
| PCB Manufacturer | | | |
|---|---|---|---|
| | **Parameter** | **TT** | **Resources** |
| 1.1 | Connectivity tests on board<br>(E-Test against Netlist) | - | - |
| 1.2 | Optical test of trace width, surface…. | - | - |
| 1.3 | Measurement of Test Strips (resistivity/impedance) | - | - |



| DESY Production I | | | |
|---|---|---|---|
| | **Parameter** | **TT** | **Resources** |
| 2.1 | Measurement of test strips on diff. layers:<br>• Resistivity<br>• Impedance | <br>0,1 min<br>1 min | <br>Quadrupole Tester<br>Reflectometer |
| 2.2 | AOI of the unpopulated PCB<br>- trace width, missing pads,<br>- Surface of bonding pads… | 2 min | AOI System |



| DESY Production II | | | |
|---|---|---|---|
| | **Parameter** | **TT** | **Resources** |
| 3.1 | X-Ray and destructive solder ball tests (1. board) | 3600 min | |
| 3.2 | Readability of the RF-ID Chip | 0,1 min | RF-ID Reader |
| 3.3 | Optical check:<br>• Correct assembly<br>• Check of none tested traces (TP<->BP)<br>• Outer row of BGAs | 5 min | AOI System |
| 3.4 | Impedance and U/I measurements:<br>• Signal connections from/to lpGBT<br>• Isolation between NTC lines/HV-return/LV-return and GND<br>• Line resistor of HV lines (CON<->BP)? | 3 min | Polartester |



| DESY ATLAS I | | | |
|---|---|---|---|
| | **Parameter** | **TT** | **Resources** |
| 4.1 | First check of EoS:<br>• Mechanical checks (dimensions, position of drill holes, flatness)<br>• Current consumption<br>• Correct initialisation | <br><br>5 min<br>0,1 min<br>0,1 min | <br><br>PS, TB, PC |
| 4.2 | Temperature test<br>• Long Term Test @ 40°C for 100 h<br>• Cycle Test @ +30°C…-30°C, 2x in 16 h | <br>6000 min<br>960 min | Environemental chamber ,<br>PS,TB, PC |
| 4.3 | Test of HV lines @ 1,5kV for 60 sec<br>• Electrical strength<br>• Residual current | <br>10 min | <br>HV-PS |

| DESY ATLAS II | | | |
|---|---|---|---|
| | **Parameter** | **TT** | **Resources** |
| 5.1 | Line resistor on HV line between:<br>• Connector and Bus Tape Bond Pads | 1 min | LV-PS, TB, PC |
| 5.2 | Line resistor on LV line between:<br>• Connector and Bus tape Bond Pads<br>• Connector and DC/DC-converter Bond Pads | 1 min | LV-PS, TB, PC |
| 5.3 | Current consumption for 1V8/2V5<br>- After boot process<br>- After initialisation<br>- At min/typ/max. values of supply voltages | <br>0,1 min<br>0,1 min<br>5 min | LV-PS, TB, PC |
| 5.4 | Check of PCB/ASIC temperature (infrared imaging) | 4 min | LV-PS, PC, Box, IR Camera |
| 5.5 | Reset signal:<br>• Function test<br>• Delay time of the reset signal (Ub/PWG) | <br>0,1 min<br>0,1 min | LV-PS, TB, PC |
| 5.6 | CCR- and AMAC down Signals:<br>• Function Test<br>• VCM, VDIFF, Timing | <br>1 min<br>5 min | LV-PS, TB, PC |

| DESY ATLAS II | | | |
|---|---|---|---|
| | **Parameter** | **TT** | **Resources** |
| 5.7 | Data Input Ports (E-Links) and AMAC up:<br>• Function Test | 1 min | LV-PS, TB, PC |
| 5.8 | $I^2C$ Bus signals:<br>• Function Test<br>• $V_{high}$, $V_{low}$, Timing | 0,1min<br>1 min | LV-PS, TB, PC |
| 5.9 | GPIOs:<br>• Function Test | 0,1min | LV-PS, TB, PC |
| 5.10 | Test of ADC/DAC | 0,1min | LV-PS, TB, PC |
| 5.11 | Test of NTC temperature measurement | 0,1min | LV-PS, TB, PC |
| 5.12 | BER Test for $10^{-13}$ @ 640Mbit/s and 14 E-Links | 20 min | LV-PS, TB, PC |
| 5.13 | Robustness and variation test with:<br>• DC/DC converter<br>• broken filter C | 5 min | LV-PS, TB, PC |
| 5.14 | Noise on power lines from board | 5 min | LV-PS, TB, PC |

DESY Stock

Agenda

HV-PS : High voltage power supply

LV-PS : Low voltage power supply

TB : Test bench (FPGA board and EoS Test Adapter)

PC : Personal Computer