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The End-of-Substructure (EoS) card for the Strip Tracker Upgrade of the ATLAS experiment

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The central building block of the Upgrade are staves and petals which host up to 14 modules per side. The incoming data is sent to the EoS and multiplexed by the lpGBT chips on 10 Gbit/s links and sent via optical transmitters (VL+) off-detector. Prototype boards have been designed, manufactured and used with the present chip versions of the GBTX /GBT-SCA chip family. This talk will summarize the experiences with the EoS prototype sitting at a single-point-of failure location. An outlook for an EoS with the faster and less power-consuming lpGBT chips and its integration will be provided.

Summary

For the ATLAS experiment an upgraded Silicon Tracker is required for the High-Luminosity Upgrade of the LHC. The main building block for the strip tracker is the module which consists of a silicon sensor and a hybrid PCB hosting the read-out ASICS. The modules are placed on so-called staves or petals which provide common services to all modules on a stave or petal. At the End of a Stave or petal, there is the End-of-Substructure (EoS) card, which connects the data, command and the power to the off-detector systems. For all that data transfers the front-end ASICs send their data on 640Mbit/s differential pairs to the End-of-Substructure (EoS) card. It will collect up to 28 data lines with one or two lpGBT chips and transmit them synchronized to the LHC operation clock with a versatile optical link (VL+) and optical fibers off-detector. From the downlink the LHC-clock is recovered by the lpGBT and the clocks and control data streams for the front end chips are generated.
Prototype electronics has been developed based on the GBTX/GBT-SCA chip family and SFP+ optical links to understand the design issues, the behavior of the EoS and the detector level integration. Presented will be the design of the electronics, the exercised tests for electrical behavior, mechanical deformation and thermal behavior. By the use of the EoS for substructure tests experience for detector level performance is gained.
For the final design the integration into the low-mass tracker with dedicated cooling severely constrains the design of the electronics. From these and the experience on the GBTX based prototypes a design-concept with lpGBT and VL+ will be presented. Since the EoS sits at a single-point-of-failure for almost a m2 of silicon strips a dedicated production control is planned and will be presented as well.

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