Contribution ID: **107**   Type: **Oral**

The Proton Timing System of the TOTEM experiment at LHC

Tuesday 18 September 2018 09:25 (25 minutes)

The new proton timing detectors of the Totem experiment, based on Ultrafast silicon detectors installed in Roman Pots at 220 meters from the interaction point 5 at LHC, will be read out through a fast sampler chip: the SAMPIC.
The best timing resolution can be obtained only by having the waveform of the detector signal.
The challenges to integrate the chip in the Totem-CMS DAQ and control systems will be discussed, and the adopted solutions reported. The system is under commissioning and will collect physics data during a special LHC run in late June. The latest results will be shown.

Summary

A special run of the LHC, expected in June, will allow the TOTEM and CMS experiments to perform high precision measurements on central diffractive processes.
With a moderate pileup we can resolve the ambiguity of the proton vertex using a timing detector with a resolution of ˜50ps. New detectors have been developed
using the Ultrafast Silicon Detector (UFSD), based on LGAD technology. To maintain the intrinsic timing performance of the sensors, in the range 30-80ps,
the collaboration will use the SAMPIC chip.
The SAMPIC is a 16 channel ASIC which can perform a fast sampling of the input signal, up to 8.4 GSa/s.
Each channel can collect 64 samples of the input signal, with an input range of 1 V and a selectable voltage resolution in the range 8-11 bits. The data frame of one channel is completed with a coarse timestamp that permits to synchronize different chips.
The Sampic will allow to collect and save the full detector waveforms, so that sophisticate offline algorithms will achieve the best timing performance.
Synchronization between our detectors is granted by an optical clock distribution system with a measured jitter ˜2ps and the possibility to monitor the clock drift.
A new board, called Digitizer Board (DB), has been designed to integrate the chip in the Totem and CMS DAQ and control systems.
The core component of the DB is a radiation hard FPGA (Microsemi SmartFusion2, SF2).
Digitized waveforms are sent from the SAMPIC to the FPGA. The SAMPIC has an internal self-triggering feature that is enabled to collect all the signals above a given threshold. However, no trigger matching is performed inside the chip, and each channel above threshold is converted independently and the relative data frame sent to the FPGA in random order.
The firmware developed for the SF2 collects the incoming frames, performs the chronological ordering and checks the frame integrity.
After the reception of the CMS trigger an internal timestamp is generated. Collected frames are scanned to retrieve the ones matching the trigger timestamp and build the event frames for the CMS DAQ.
Since the number of fired channels matching a given trigger is not constant, and the event size must be kept as low as possible, a strong data reduction and zero suppression is also implemented. In the final stage the event frame is serialized and sent through an optical link. The timing system has been installed in February 2018

and is actually under commissioning. Successful data taking has been done during the luminosity ramp-up fills of the LHC and during the special alignment run of the Roman Pot stations.

Detector and electronics performance will be reported, based on the latest results. The limitation in rate of the present setup will also investigated to understand the future developments needed. The results achieved by this project are of exceptional relevance also for the future upgrade of the experiment, exploring the possibility and testing the challenges of a full offline sensor signal reconstruction and analysis.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

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