Hardware Trigger Processor for the ATLAS New Small Wheel system

Thiago Costa de Paiva

For the ATLAS Muon Collaboration

1University of Massachusetts Amherst

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The ATLAS NSW Trigger Processor system
The New Small Wheel upgrade aims to reduce fake triggers from background hits.
- B and C are rejected with NSW trigger
- R-\(\phi\) pointing to Big Wheel regions of interest
- \(\Delta \theta\) between local segments and infinity momentum track.
Robust redundancy: both used for tracking or trigger
- sTGC wires/strips for tracking, strips/pads for trigger.
- MM strips for tracking, first hit above threshold for trigger.
NSW Trigger overview

- MM: 2 M strips (0.4 mm)
- sTGC: 280 K strips (3.2 mm), 45 K pads, 28 K wires
- MM and sTGC trigger algorithms run independently
  - sTGC: 4 candidates/BC
  - MM: 8 candidates/BC
- Single candidate must be sent to Sector Logic (SL), which will combine information from NSW with the Big Wheel
- Track candidates computed on FPGAs in the trigger processor (TP), which receives trigger hits from upstream electronics
- Total latency budget for full NSW trigger processing chain is 43 LHC bunch crossings (1075 ns)
- Latency budget: 120 ns from deserialization of the last input bit until the first output bit from the output serializer is sent to the Sector Logic

Output to Sector Logic

<table>
<thead>
<tr>
<th>Num of bits</th>
<th>Spare</th>
<th>Low res.</th>
<th>(\phi) resol.</th>
<th>(\Delta\theta) (mrad)</th>
<th>(\phi) index</th>
<th>R index</th>
<th>Monitor</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>5</td>
<td>6</td>
<td>8</td>
<td>1</td>
</tr>
</tbody>
</table>
- Router forwards the data pre-selected by the Pad Trigger from TDS to the TP
- Each VMM takes hits from 64 strips; address of the first strip to cross threshold is used as trigger ART (Address in Real Time) hit
- The ART Data Drivers Cards aggregate trigger hits from multiple front end boards and send to the TP.
- See “Frontend and backend electronics for the New Small Wheel Upgrade of the ATLAS muon spectrometer” by Xu Wang (TWEPP 2018)
NSW Trigger Processor context

Detector interface
- 2 fibers from Pad Trigger
- 32 fibers (4 fibers per layer, 8 layers)
- MM: 4.8G
- sTGC: 4.8G
- data tagged by BCID at source

Trigger Processor FPGA
- Algorithm on ATCA mezzanine card
- 64 LVDS lines to/from other detector’s T.P.
- FPGA config

Trigger Processor Algorithm

Interface to Sector Logic
- Busy
- (2 streams of candidates)
- 6.4Gb/s each
- TTC
- BC clock

Ancillary Functions

FELIX
- E-links (statistics, sampled BCIDs)
- Level-1 Accepted events
- algorithm params
- TTC
- BC clock

Monitor processor

swROD

Configuration processor

DCS

Hardware Services
- Ethernet
temps
voltages
ATCA shelf mgr

Note:
- 7 copies of each stream are produced
NSW Trigger Processor algorithms
Algorithm implemented in a trigger processor FPGA

- Calculate charge centroid per plane (0.1mm)
- Average centroids in each quadruplet
- Compute \( \Delta \theta \) using LUTs
  - \( \Delta \theta = \theta_{IP} - \theta_{Pivot} \)
- R-index is the centroid average of pivot and confirmation quadruplets
- \( \phi \)-index determined from the pad trigger tower phi-ID

The sTGC trigger algorithm can process up to 4 candidates in parallel per 1/16\textsuperscript{th} sector.
sTGC trigger algorithm (2/2)

sTGC

**sTGC**

- **deserialization**
  - 4.8G, 4x8 links
  - 104 bits/link/BC

**TDS data merger and distributor**

- 4x8 links

**Centroid finder**

- band-ID to seg finder

4 band-IDs

**band-ID to seg finder**

- 0..3
- 4..7
- 28..31

**segment finder**

- 7 copies

**format segments**

- ≤4

**merge segments**

- ≤8

**8 candidates in 2 packets**

- 7 copies each

**8b/10b 6.4G serializer**

- to Sector Logic 7 copies

**8b/10b 6.4G serializer**

- to Sector Logic 7 copies

**from MM**

- φ-ID

**≤8**

**segment finder**

- 7 copies
MM trigger algorithm (1/2)

- Find the slope of each hit strip with respect to the interaction point
- Collect hits that are in the same slope roads and produce a multi-plane coincidence trigger “Finder”.
- $\Delta \theta$ calculated from X slopes
- $\phi$ calculated using U and V slopes.

![Display of Slope Roads (all "roads" are not shown)](image)

- Each hit is first binned into one slope road
- X-plane hits are also binned into one nearest neighbor (tolerance $\sim 0.5$ bin)
- UV-plane hits are binned into several nearest neighbors

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**Diagram:**

32 x 4.8G ADDC ART GBT Format → GBT Packet Deserializer and Alignment → GBT Packet Decoder and Distributor → 16 Finders → 16 Fitters → Track Candidate Selection and Formatting → Output to sTGC for Segment Merging and TX to Sector Logic
MM trigger algorithm (2/2)

Look for a hit in the horizontal roads.

Determine roads under interest for U and V planes

Using pipeline, look for coincidences between U and V roads using the X road as reference (diamond area)

Coincidence of 3 of 4 strips (at least one of the horizontal roads is active)
NSW Trigger Processor Electronics
NSW TP Carrier and Mezzanine boards

Carrier board
- 2 mezzanines
- 2 Virtex 6 FPGAs
- 2 DDR3 memories
- 1 Spartan 6 FPGA

Mezzanine
- 2 Virtex 7 FPGAs
- 6 RX/TX µPod pairs
- 72 optical ports (10Gbps)

Rear Transition Module
- 14 SFP+ ports
- 2 RJ45 (DTCC)
- 2 NIM (SMA)
New carrier board motivation

Limitations in the current design:

- Outdated FPGAs with no support by current Xilinx tools
- Insufficient clock resources and flexibility
- Unsuitable Xilinx Virtual Cable protocol support for remote debug
- Non-existing ATCA support for the controller in the mezzanine

New design:

- Similar architecture
- Xilinx Ultrascale family
- Improved clock resources and flexibility
- Multiple ethernet access through backplane or RTM
- Zynq 7000 for extended control and hardware services
NSW Trigger Processor Testing
Trigger Processor algorithm testing

Pattern generators: main testing tool
- Inserted direct in FPGA memory
- FPGAs in the same mezzanine
- FPGAs in different mezzanines

CERN Vertical Slice ART Data Chain

Cosmic ray test stands also available for further analysis of the algorithms
Tests performed in realistic conditions (ATLAS infrastructure, load boards)

Mezzanine optical transceivers and FPGAs are the critical components

Multiple profiles verified with similar results

Exercised up to 26 W per FPGA (estimated around 20 W) always well under 85°C

Clear influence of the power dissipated in the surrounding boards

Clear influence of the chiller cooling cycles
Bonus
MM algorithm – Utilization and placement

- Full edge implementation of the current algorithm
- Working on the algorithm to meet timing
- Algorithm divided into 16 regions. Each region share signals with 2 neighbors. Placement constrained to avoid long signal paths (gray)
- Still some functionality to be added
MM algorithm – Latency

- Estimated latency within specifications
Closing remarks
Future Outlook

- NSW upgrade will greatly improve tracking efficiency and reduce fake trigger rates from background hits in the high rate end-cap forward region.
- Trigger algorithms for both the MM and sTGC technologies have been developed and are currently being commissioned in hardware.
- Use of dedicated FPGA resources and well planned approaches allows the algorithms to stay within their demanding latency budgets.
- The ATCA based trigger processor platform will allow for fast communication of trigger data and transmission of track candidates to the new Sector Logic system for triggering.
- Thermal tests ensured that no temperature problems are foreseen in the NSW TP design.
- Algorithm testing is moving to CERN for permanent setups allowing long term tests.
Backup
Matching to Sector Logic Boards

Track vector information from the NSW is combined with results from the current Level-1 muon trigger system (TGC-BW)

Big Wheel Regions-of-Interest to be confirmed by NSW

**Red lines** are NSW sector boundaries.

The partitioning of the Trigger Sectors and granularities of the RoI remain the same as in the present scheme.

Mismatch of NSW and BW detector boundaries

⇒ fan-out up to 7 SL boards

2 BW trigger sectors ==> 1 SL Board

7 x 2 optical links
NSW TP mezzanine

HORX Mezzanine Card - Connectivity

Specifications - FPGA

- High Density Optical Mezzanine for ATCA
- Dimensions: 145mm x 146 mm
- FPGA: 2 x Virtex-7 (415T, 485T, 550T, 690T)
- Front-end:
  - 72 RX + 72 TX Optical Fibers (36/36 each FPGA)
  - 12 x Avago MicroPod modules (up to 12.5 Gbps)
- Inter-FPGA interface:
  - 64 LVDS inter-FPGA
  - 8 GTH inter-FPGA
- Carrier interface:
  - 50 LVDS to blade
  - 8 GTH to blade
  - Separate System & GTH clocks
  - Power (12V) and management (IPMI, JTAG)
- Inter-FPGA interface:
  - 64 LVDS inter-FPGA
  - 8 GTH inter-FPGA

Satisfies key connectivity requirements required
→ lateral bandwidth of 7.0 Gbps to transmit candidates from MM to sTGC processors with minimal latency