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Hardware Trigger Processor for the ATLAS NSW System

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The main goals of the ATLAS New Small Wheel (NSW) upgrade are to reduce fake triggers from backgrounds hits and improve the tracking efficiency in the high rate environment at the LHC. A low-latency hardware trigger processor is being developed for the NSW in the muon spectrometer. The processor will fit candidate muon segments in the small-strip Thin Gap (sTGC) and MicroMegas (MM) chambers in real time, improving significantly the background rejection. We present the overall electronics design and implementation of two pure-FPGA algorithms in an ATCA architecture for finding track segments using trigger data from the sTGC and MM.

Summary

The ATLAS New Small Wheel (NSW) trigger processor will be implemented as a set of 16 ATCA blades that each includes two mezzanine cards. The main goal of this system is to provide segments for the first-level trigger. Each mezzanine card provides up to 72 multi-gigabit links to handle the signals from a sector of small-strip Thin Gap (sTGC) and MicroMegas (MM) chambers.

Hits from sTGC and MM chambers are received in real time over optical links from the detector with minimum latency. Segment finding is implemented on the mezzanine card on separate FPGAs for sTGC and MM. Each mezzanine card covers one 16th of the wheel. The segments using sTGC and MM information are subsequently combined to derive NSW trigger segments. An important requirement is fast interconnects between the two FPGAs to be able to perform the candidate merging with minimal latency.

The NSW trigger segments are then sent to the ATLAS muon sector logic that combines the NSW trigger information with the trigger signals from the Thin Gap Chambers (TGC) in the Big Wheels (BW) to provide the full muon trigger decision. The NSW trigger processor provides coordinates for the NSW trigger segments to derive a coincidence between the NSW and the regions of interest identified by the BW. In addition, the difference in polar angle between the NSW segment and the line connecting the segment with the interaction point is calculated. This difference is used to reject backgrounds from particles that do not come from the collisions.

In addition to implementing the trigger algorithms for the MM and sTGC systems, the NSW trigger processor has to perform several ancillary functions. These include time synchronization, configuration, monitoring and debugging mode, among others. Several of these functionalities rely on the ATCA blade and Rear Transition Module (RTM). A new ATCA blade has been specified and will be built. Algorithms in firmware running on prototype ATCA hardware (blade, mezzanines and RTM) are currently being tested, with a full system ready for installation during LHC Long Shutdown 2 in 2019-2020. The implementation of the segment finding logic and the ancillary functions, the ATCA hardware, and the performance of the NSW trigger system will be described.

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