Contribution ID: **85** Type: **Oral**

The Muon to Central Trigger Processor Interface for the Upgrade of the ATLAS Muon Trigger for Run-3

Wednesday, 19 September 2018 12:00 (25 minutes)

The Muon-to-Central Trigger Processor Interface(MUCTPI) of the Level-1 muon trigger of the ATLAS experiment is being replaced for the LHC Run-3. The upgraded MUCTPI is implemented as an ATCA module using high-end FPGAs and high-density ribbon fibre-optic modules to integrate over 270 multi-gigabit optical inputs and outputs on a single board.
The MUCTPI also features a System-on-Chip(SoC) with an ARM processor running an embedded Linux OS to control the module. We present results from the hardware and firmware validation of the second prototype based on Xilinx/Ultrascale+ FPGAs, and about the SoC used to interface to the experiment run control system.

Summary

The Muon-to-Central Trigger Processor Interface (MUCTPI) is part of the Level-1 trigger system of the ATLAS experiment at CERN. It receives and combines information on muon candidates from the 208 trigger sector logic modules of the detector and calculates the candidate multiplicity, taking into account the possible double counting between trigger sectors due to the geometrical overlap of the muon chambers and the trajectory of the muons in the magnetic field, and sends the result to the Central Trigger Processor (CTP). The existing MUCTPI is being upgraded for Run-3 of the Large Hadron Collider, in order to interface with the new muon endcap trigger sector logic modules which will be deployed as part of the muon new small wheel upgrade. The upgraded MUCTPI will also be able to send full precision information on the muon candidates identified by the muon trigger processors at the bunch crossing rate to the topological trigger processor (L1Topo) of the Level-1 trigger system, which will allow combined calorimeter/muon topological trigger algorithms to be implemented. The MUCTPI for Run-3 is implemented as a single AdvancedTCA (ATCA) blade, replacing a full 9U VME shelf with 18 boards of the existing system. This high level of integration is enabled by the use of state-of-the-art FPGA devices, featuring a large number of on-chip high-speed serial transceivers, and high-density ribbon fibre-optics receiver and transmitter modules. The module features over 270 multi-gigabit optical inputs/outputs operating at line rates between 6.4 and 11.2 Gb/s, resulting in an aggregate bandwidth of 2 Tb/s. Two large Xilinx Virtex UltraScale(+) FPGAs (sector processors), each covering one side of the detector, are used to receive and process the muon trigger information from the 208 sector logic modules and forward lists of muon candidates to L1Topo through up to 48 serial

optical links. A third FPGA, a Xilinx Kintex UltraScale device, is used to merge the information from the two sides of the detector, to perform the required trigger calculations and to send the resulting object multiplicities and trigger flags to the CTP. For events accepted by the CTP, it also outputs a list of muon candidates to the DAQ and high-level trigger systems. Finally, a Xilinx Zynq System-on-Chip (SoC) FPGA is used to interface the MUCTPI to the ATLAS run control system through a Gigabit Ethernet connection. It is used to configure and control the MUCTPI and to read state and monitoring information. The SoC device runs an embedded Linux with application-specific software using a remote-procedure-call approach. In addition, we have ported a simple run control application from the ATLAS TDAQ software which can control and configure the MUCTPI, provide monitoring data (including ROOT histograms). A first fully functional prototype of the MUCTPI exists and has been extensively tested. We present results from the validation of second prototype, which uses 16 nm Ultrascale+ FPGAs for the sector processors. We also give an overview of the firmware as well as the software environment running on the SoC and show results from first integration tests.

Primary author: SILVA OLIVEIRA, Marcos Vinicius (Federal University of Juiz de Fora (BR))

Presenter: SILVA OLIVEIRA, Marcos Vinicius (Federal University of Juiz de Fora (BR))

Session Classification: Trigger

Track Classification: Trigger