WHAT IS SERENITY?

• ATCA Development Platform

• Carrier Card
  • Services - Power, Clocks, Optics, Interconnects, IPMC & CPU

• Daughter Cards
  • Data Processing FPGAs

• Firmware & Software
  • Generic, Flexible Infrastructure
AN ASIDE: COTS COMPONENTS

ATCA low level control – IPMC
- Available from CERN
- Runs the commercial standard software

Standard Intel x86 COM-Express Type 10 CPU
- Running standard Centos Linux
- What sysadmins want, not necessarily what hardware engineers want!
- PCIe interface to FPGAs
- Clean separation of hardware, firmware and software

Ethernet
- Switch with integrated Gigabit Ethernet Phys
- AC coupled via capacitors
- Small form factor 1cm²
- VLAN capable
WHICH PROBLEMS IS SERENITY MEANT TO SOLVE?

• Different projects want different FPGAs, different optical and electrical connectivity
  • Can one board make everyone happy?
  • If not, can we at least provide a rapid-prototyping platform for ATCA?
• Bulk of cost concentrated in FPGAs, bulk of potential failure modes in carrier
  • Can we decouple financial risk from production risk?
HOW?

• FPGAs on Daughter-cards:
  • Freedom to choose your preferred family, package, generation, (vendor?)
  • Freedom to choose your balance of optical and electrical connectivity
  • Carrier testing done with FPGAs safely in their static-bags

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Samtec Z-RAY produced to custom specification
WHAT WERE THE CONCERNS?

• We started the project with serious concerns over choice of ATCA, particularly:
  • Thermal management
    • Optics must be kept below 50C or longevity drops at shocking rate
  • Acoustic noise

• Others expressed concern over
  • Interposer signal integrity
  • Supplying power to FPGAs
  • Cooling FPGAs on daughter-cards
  • Limited prior experience with 16 or 25G links
  • Whether different institutes could really produce their own daughter-cards?
Can different groups produce daughter cards?

- IC - Xilinx KU115: Symmetric & Daisy Chained
- KIT - Xilinx KU15P
- TIFR - Xilinx VU9P
- Saclay – a clock-network analysis daughter card

All optical KU115, Imperial
Mixed optical/electrical KU15P, KIT
Clock-performance analyzer CEA Saclay
In progress, All optical VU9P, TIFR

Daisy-chain, optical in
Daisy-chain, optical out
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FEATURE TESTING

- All features tested except
  - TTC/TTS distribution
  - No DTH
  - SPI control of Ethernet switch
  - Switch works in default config.
  - RGMII to FPGAs
    - Using PCIe instead
- All tested features working
LINKS - INTERNAL LOOP

- 120 simultaneous IBERTs
  - 16Gbps, Near-end PMA loopback. Default settings
- Each link passed 1e15 bits - No errors
- 120Pb of data through silicon
- Indicated good clock and power stability
• Inter-interposer bus
• Two independent FPGAs
• 16Gbps, DFE disabled, No Pre-or Post-Cursor
• Each link passed 8e14 bits – No errors
• Firefly optics
• Two independent FPGAs
• 16Gbps, DFE disabled, No Pre- or Post-Cursor
• Default optical module settings
• 10m optical fibre
• Each link passed 8e14 bits – No errors

FPGA 1 → daughter-card → interposer → motherboard → firefly → MTP → 10M optical cable → MTP → firefly → motherboard → interposer → daughter-card → FPGA 2

No optical module present

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25GBPS INITIAL RESULTS

Firefly over copper 25Gbps PRBS31

Inter-interposer bus 25Gbps PRBS31

Using the deprecated 14Gbps-rated Firefly connector
THERMAL & MECHANICAL TESTS

• Thermal simulations
• Physical thermal studies at CERN
• Mechanical component design, studies into stress on FPGA solder balls and stress on PCBs under way at IC

Max temperatures reported

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• Kapton heaters
• Comtel Crate
  • Front-Back Airflow
# THERMAL TEST RESULTS

## Measurement, Fan Speed 15

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>35°C</td>
<td>35</td>
</tr>
<tr>
<td>42°C</td>
<td>42</td>
</tr>
<tr>
<td>33°C</td>
<td>33</td>
</tr>
<tr>
<td>37°C</td>
<td>37</td>
</tr>
<tr>
<td>73°C</td>
<td>73</td>
</tr>
</tbody>
</table>

## Simulation, Fan Speed 15

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>40°C</td>
<td>40</td>
</tr>
<tr>
<td>38°C</td>
<td>38</td>
</tr>
<tr>
<td>36°C</td>
<td>36</td>
</tr>
<tr>
<td>42°C</td>
<td>42</td>
</tr>
<tr>
<td>67°C</td>
<td>67</td>
</tr>
</tbody>
</table>

- Standard CERN crate made by Schroff, Vertical Airflow
  - FPGAs @ 90W each
  - Max temperature 100 °C
  - Optics @ 10W each
  - Max temperature 50 °C
  - May increase to 20W so need margin
- Simulation by Ansys
- KIT also running simulations with Mentor FloTHERM for comparison

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Measurement, Fan **Speed 10**

- 39°C
- 47°C
- 34°C
- 39°C
- 78°C

Measurement, Fan **Speed 13**

- 36°C
- 44°C
- 34°C
- 37°C
- 75°C

Measurement, Fan **Speed 15**

- 35°C
- 42°C
- 33°C
- 37°C
- 73°C

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• Simulations suggest significant improvement with custom heatsink.

• Validation of simulation with measurement under way.
• Measurements of the running ATCA system still a cause for concern regarding
  • Aural (acoustic) health and safety
  • Power-consumption required to cool system
CLOCK-DISTRIBUTION TESTS

• Serenity is TDR proposal for CMS HGC DAQ, trigger, clocking and control board.
• HGC requires precision timing distribution
• CEA Saclay have been testing whether Serenity’s clocking performance meets HGC requirements
CLOCK-DISTRIBUTION TESTS

• 320.624MHz test clock (HGC precision-timing frequency)
• External clock-source, RMS = 1.3ps
• Serenity tested at 20GS/s (Eval board at 40GS/s)

<table>
<thead>
<tr>
<th>Measurements by CEA Saclay</th>
<th>SI5444 Eval board for comparison (4 outputs)</th>
<th>Serenity North LHC clock (9 outputs)</th>
<th>Serenity South LHC clock (9 outputs)</th>
<th>Serenity Overall</th>
</tr>
</thead>
<tbody>
<tr>
<td>Random Jitter</td>
<td>0.9ps</td>
<td>1.6ps</td>
<td>1.4ps</td>
<td>1.8ps</td>
</tr>
<tr>
<td>Deterministic Jitter</td>
<td>1.9ps</td>
<td>3.2ps</td>
<td>3.1ps</td>
<td>4.2ps</td>
</tr>
<tr>
<td>RMS</td>
<td>1.3ps</td>
<td>2.3ps</td>
<td>2.1ps</td>
<td>2.8ps</td>
</tr>
</tbody>
</table>

• Based on these results, Serenity’s contribution to system jitter is minimal and it can be considered a “pure clock distribution” node
• Ipbus-over-PCIe worked out of-the-box

• Have built upon the success we had with MP7 model in Phase-1 upgrades
  • Infrastructure firmware – EMP
  • Build Tool - IPBB

FIRMWARE

• Infrastructure separated from payload for algorithms
• Different boards

• Different configurations

EMP FIRMWARE
CONCLUSIONS

• Serenity has succeeded in its initial aims of allowing multiple types of FPGA and user-specified connectivity, and also in mitigating risk
  • Different institutes have successfully produced their own daughter-cards, each with different generations & models of FPGAs

• Concerns over interposer signal integrity and supplying power to FPGAs seem unfounded

• Performance at both 16G and 25G looks good

• Cooling of both optics and FPGAs on daughter-cards looks manageable
  • General concerns over power and noise of LHC-scale systems built using ATCA remain
WHAT NEXT?

• 20 Revision 1.1 cards in assembly now
• A number of cards destined for “time-share test-stands” at CERN
  • Allow systems to test “full-stack” algorithms from source to sink
  • Also, horizontal integration with CERN DTH & online software when they become available
• Remaining cards destined for collaborating institutes
THANKS FOR LISTENING!
ANY QUESTIONS?

CEA Saclay: Ozgur Sahin, Pierre-Anne Bausson
IC: Andrew Rose, Duncan Parker, Greg Iles
INFN Pisa: Giacomo Fedi, Piero Giorgio Verdini, Andromachi Tsirou
KIT: Luis Ardila, Matthias Balzer, Thomas Schuh
RAL: Tom Williams, Alessandro Thea, Kristian Harder
TIFR: Shashi Dugad, Raghu Shukla, Irfan Mirza
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I do not own, nor do I assert any right of ownership over, the Serenity logo. It is just a cool logo from a cool TV series (Firefly) and subsequent film (Serenity). I urge you to go and buy them both: They’re a lot of fun.
HARDWARE IN HAND
MICRO-BACKPLANE

Dual RJ45 (2×GbE)

LHC + precision LHC clock - SMB connectors

ATCA zone-2

I2C and address pins

ATCA zone-1

Banana-plug: -48V and GND

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OFF-CHIP LINK IBERTS

- 120 simultaneous IBERTs
  - 16Gbps
  - 60 through fireflys, 60 over copper
  - Default settings
- With highlighted caveats, each link passed 8e14 bits
  - No errors
- 1 board, 85Pb between FPGAs

Polarity configuration error

X1 to X0 over copper

X0 to X1 over fibre

No optical modules plugged

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CARRIER TESTING

• Com-express & GBE
  • HD display-port, USB, SSD, Centos-7, GBE† all working
• Artix-7 Service FPGA
  • JTAG, Flash, Heartbeat LED, Clocks, PCIe to Com-express all working
• IPbus-over-PCIe
• The existing MP7 I2C-over-Ipbus and JSM JTAG-over-Ipbus infrastructure also work unchanged

†Com-express→On-board GbE switch→ATCA zone-2 connector→Micro-backplane→RJ45→Outside world
COMMUNICATION VIA PCIe

- JTAG to both KU115s via the Artix
  - Digilent USB-debugger via Artix GPIO
  - XVC-over-Ipbus-over-PCIe
  - Directly over Ipbus
- Heartbeat LEDs
- Debug LED arrays
- Programming Flash
- PCIe & system clock

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00:1f.3 SMBus: Intel Corporation Atom Processor E3800 Series SMBus Controller (rev 11)
01:00.0 Serial controller: Xilinx Corporation Device 7021
02:00.0 Serial controller: Xilinx Corporation Device 8031
03:00.0 Serial controller: Xilinx Corporation Device 8031
04:00.0 Ethernet controller: Intel Corporation I210 Gigabit Network Connection (rev 03)

Off-the-shelf CPU coolers for benchtop testing
EMP FIRMWARE: EXAMPLE

• Many large Xilinx parts are now multi-die
  • Super Logic Region
  • How do algorithms developed in MP7 port to UltraScale?

• HT Track Trigger
  • Geometric Processor Component
  • Concern over inter SLR routes
  • Quickly port to KU115
  • VU9P or KU15P also available.
  • Only 20% of inter-die routes used.