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Serenity - An ATCA prototyping platform for CMS Phase-2

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Serenity is an ATCA prototyping platform designed to explore alternative, novel design choices for CMS Phase-2. It uses a newly available interconnect technology from Samtec (z-ray) to mount a removable processing unit (FPGA) that should mitigate risk and provides significant flexibility in processing unit choice and connectivity. The presentation will explore the pros and cons of using an industry standard Computer-On-Module, running x86 Centos and a small service FPGA for low level control. Specially designed Kapton heaters will be used to validate the thermal design, while structural test results will be presented for the heatsink design.

Summary

Serenity is an ATCA prototyping platform designed to explore alternative, novel design choices for CMS Phase-2 off-detector electronics, as well as providing a development platform for system firmware and software designers. It uses a newly available interconnect technology from Samtec (z-ray) to mount one or more removable processing units (FPGAs in our case) onto the card. The objective is to add flexibility and mitigate risk. The flexibility is achieved it two ways. The small PCB on which the processing unit resides permits may different processing units to be used. The additional routing capability of the processing unit daughter cards allows a single base board with two processing sites to support a daisy chained, parallel, or parallel with shared bus configuration. Risk is mitigated because a fault on the relatively low cost base board does not require the expensive processing units to be discarded. In many ways it therefore mirrors a PC design, in which the CPU, GPU and memory are pluggable. The high density of the interconnect enables it to be used to bring in power, while the excellent high-speed performance (28 Gb/s in the current case, with newer versions available up to 56Gb/s NRZ) make it also suitable for SerDes connections. The board takes a novel approach to on board control. Instead of using an FPGA with embedded CPU (e.g. Zynq) it allows the exploration of the pros and cons of using an industry standard Computer-On-Module, running x86 Centos and a small service FPGA for low level control (e.g. I2C, JTAG). Access to processing units (FPGAs) is via PCIe with an IPBus interface in the FPGA and the matching uHAL software library. A benefit of this approach is that users have been able to use off-the-shelf PCIe development cards for algorithm development while final the final hardware is debugged. The ubiquitous nature of PCIe also allows the firmware and software stack to be re-used for other applications. Serenity has recently returned from manufacture. In addition to the standard testing procedure there will also be a dedicated thermal and structural test. The former will use specially designed Kapton heaters to simulate a total processing load of up to 130W (either single site or split over the two processing sites) and optical module load of up to 120W. This is essential given the significant increase in power over Phase-1 designs that used MicroTCA (35W per FPGA) and the requirement to maintain optical module temperatures below 50 ℃ to increase their longevity. There will also be a structural test to assess heatsink load distribution on the part, which is necessary to ensure that sufficient pressure can be applied to ensure a good thermal contact without damaging the part itself, such as the solder balls.

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