UNIVERSITY OF BIRMINGHAM | SCHOOL OF PHYSICS AND ASTRONOMY

ALICE

ALICE trigger system for LHC Run 3

M. Krivda for ALICE CTP

TWEPP

18.09.2018

UNIVERSITY OF BIRMINGHAM | SCHOOL OF PHYSICS AND ASTRONOMY

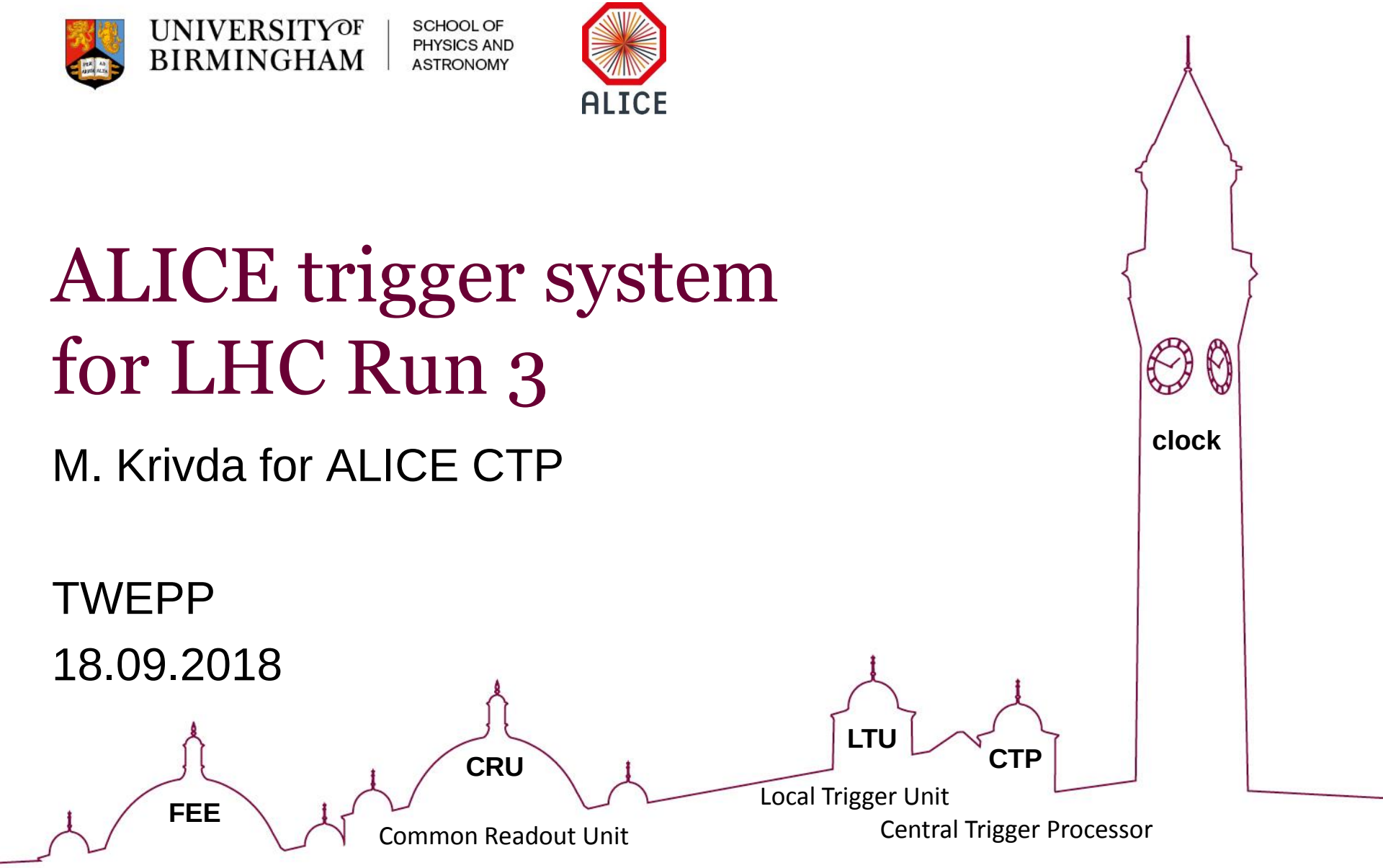
ALICE

ALICE trigger system for LHC Run 3

M. Krivda for ALICE CTP

TWEPP

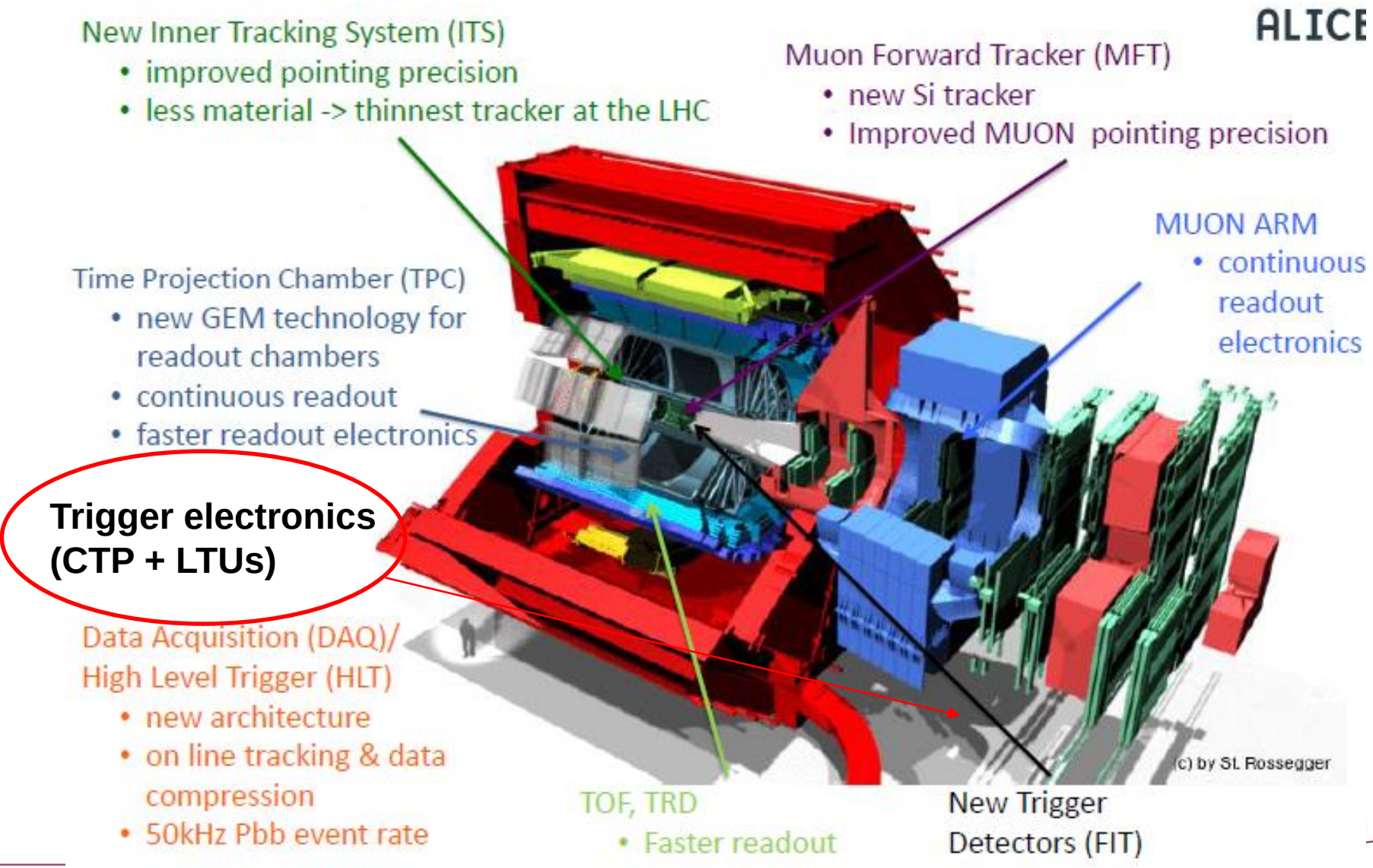
18.09.2018



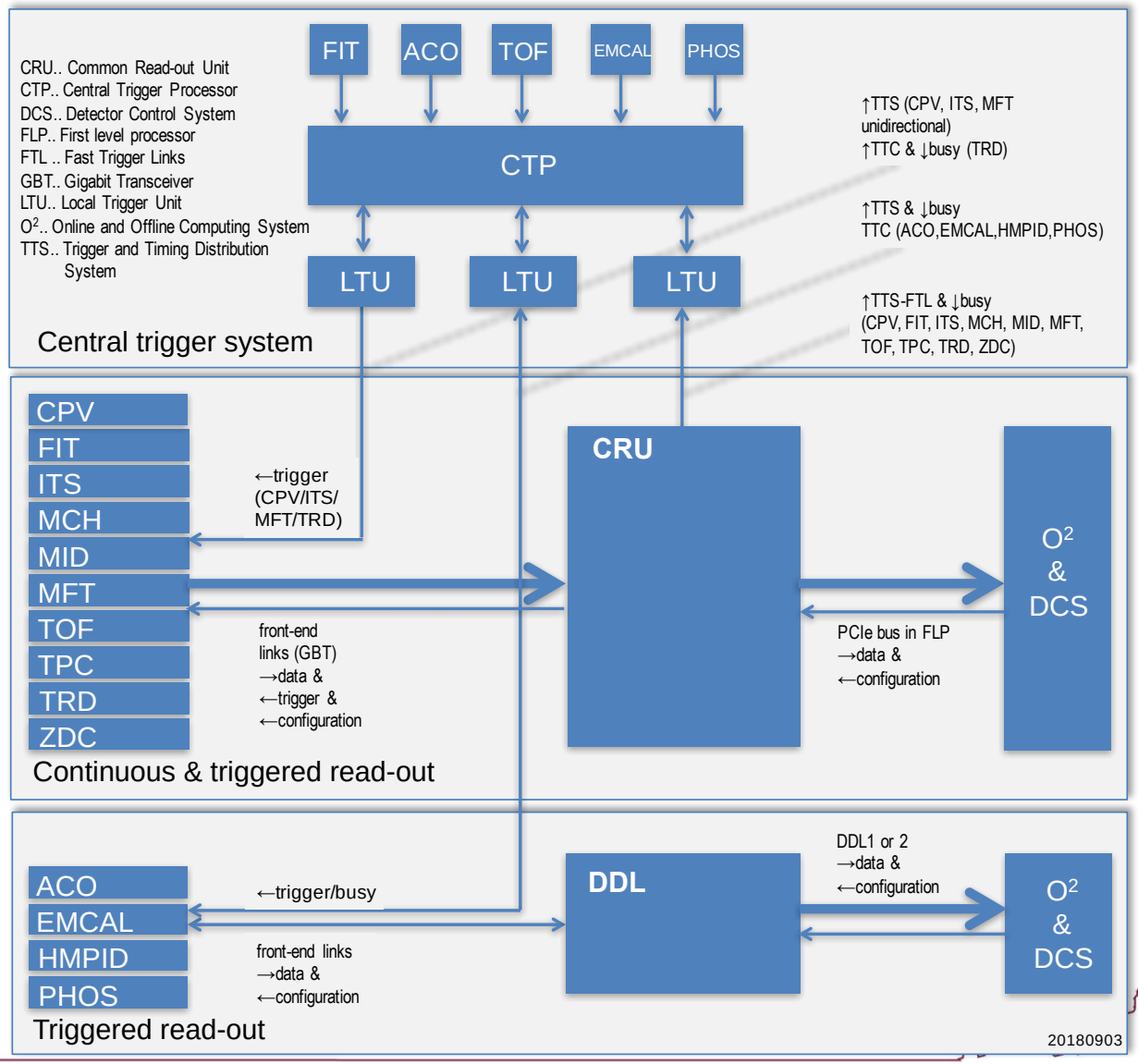
Content

- ALICE experiment in LHC Run3
- New trigger system overview
- CTP/LTU board description
- Test results for 1st production batch (23 boards)
- Implementation and test of TTC-PON for ALICE trigger system (CTP, LTU, CRU and VLDB boards)
- Summary

ALICE experiment in LHC Run3



ALICE system block diagram



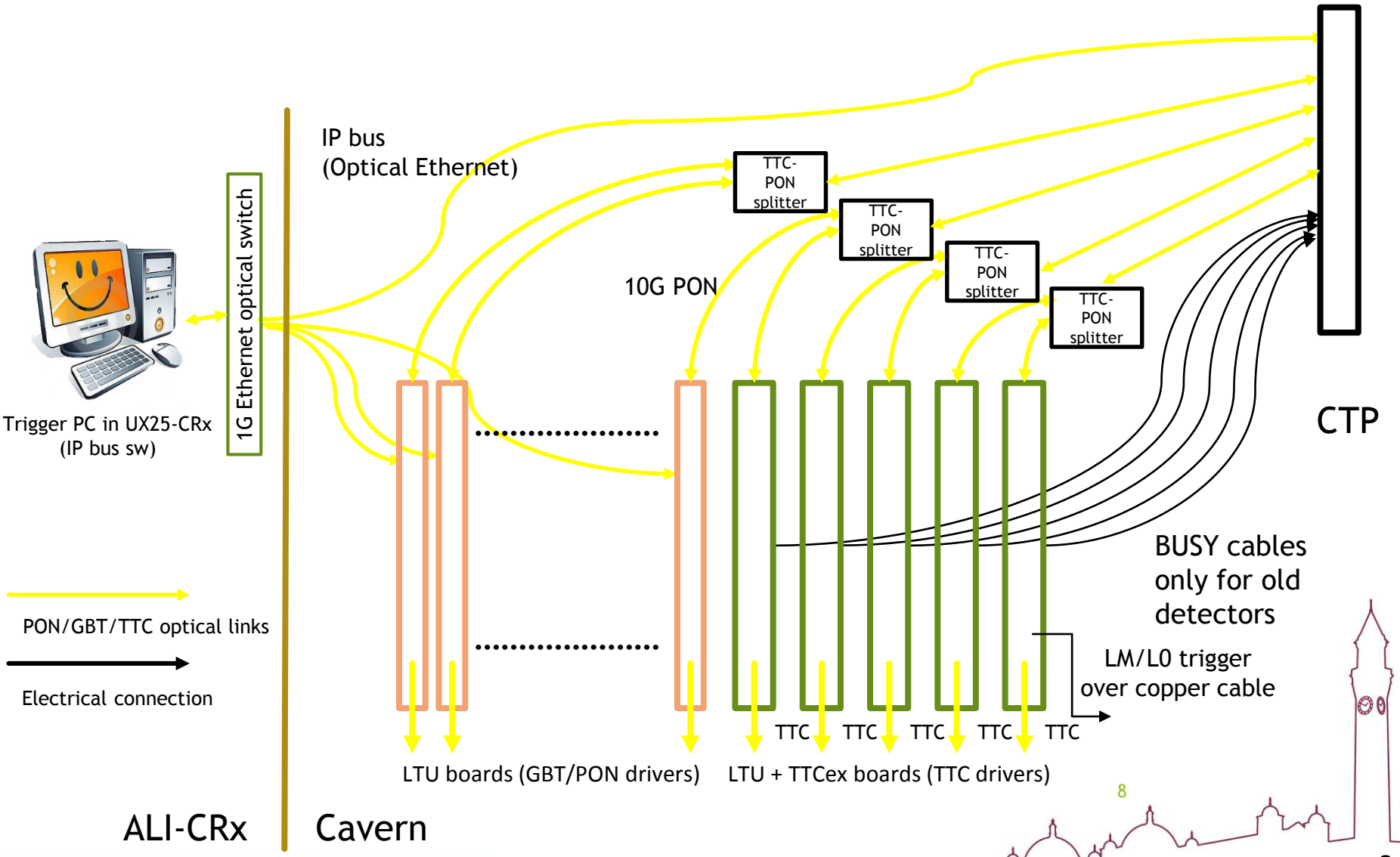
Trigger system requirements I.

- Interaction Rates:
  50 kHz for Pb-Pb, and up to 200 kHz for pp and p-Pb
- 2 modes of detector operation:
  - continuous and triggered
- Main ALICE trigger sensitive to interactions (LM)
  - LM - interactions, L0, L1 – specialized triggers
- All detectors able to receive triggers, triggers can be sent every BC
- Continuously monitoring status of ~500 CRUs and control data flow
- Backward compatible with detectors not upgrading
- No CTP dead time
- 3 types of trigger data distribution
  - Directly on detector (ITS and MFT detectors) via GBT
  - Via Common Readout Unit (CRU) using TTC-PON for upgraded detectors
  - Via existing TTC system for old detectors

Trigger system requirements II.

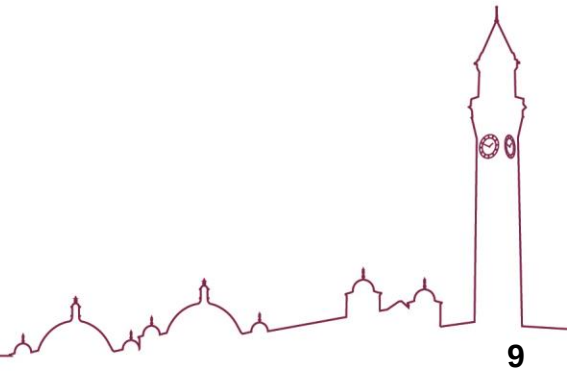
- 14 detectors (9 with TTC-PON system, 4 with TTC system, TRD (TTC+PON))
- 6 Triggering detectors (FIT, ACO, EMC, PHO, TOF, ZDC; 34 trigger inputs)
- Trigger Input latencies (time from interaction to signal input at CTP)
  - 425 ns (contributing detector – FIT) → Interaction (Minimum Bias) trigger
  - 1.2 μs (contributing det. – ACO, EMC, PHO, TOF, ZDC)
  - 6.1 μs (EMC, ZDC)
- Each detector sees only ONE trigger (LM, L0 or L1)
  - Except special cases (PHOS and HMPID)
- Electronics must survive in magnetic field of ~11 mT (rack location near/below the dipole magnet)
- Random jitter on the clock <10 ps at FEE (TOF requirement)

The trigger-system overview



8

CTP/LTU board description



Design of CTP/LTU

- Single universal trigger board (CTP/LTU board)
  - FW configures board either in CTP or LTU configuration
- Kintex-Ultrascale FPGA (XCKU040-2FFVA1156E) for LTU board
- Kintex-Ultrascale FPGA (XCKU095-2FFVA1156E) for CTP board

- Interface between CTP and LTUs is via TTC-PON system
  - allows two-way data traffic between CTP and LTUs
- IPbus “basex” version of firmware, electrical SFP or optical SFP plug in module for Ethernet
- CTP/LTU board has FMC mezzanine card and triple-width front panel
  - VME-type 6U board (VME for power only)

CTP/LTU board

Power Good LED

JTAG connector

Power Management bus connector

FMC board

LTU mode: FMC S-18 card (optional, GBT, Ethernet)

CTP mode: (70 LVDS I/O) – Trigger inputs etc.

FPGA Kintex Ultrascale (A1156 package)

Clock out (LVDS or LVECL or HSCL or CMOS or custom differential)

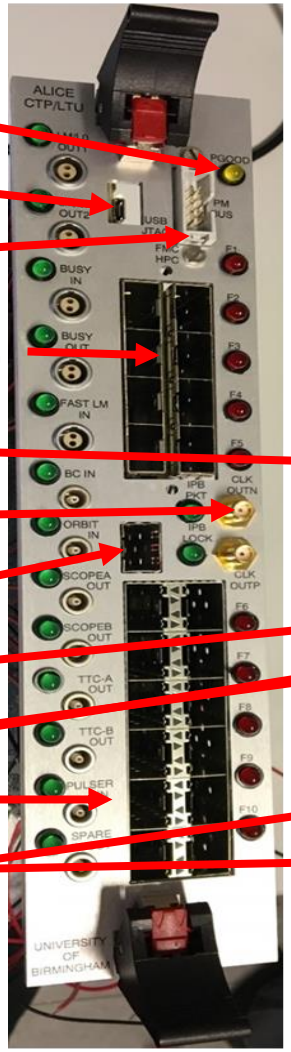
SFP+ for IPbus

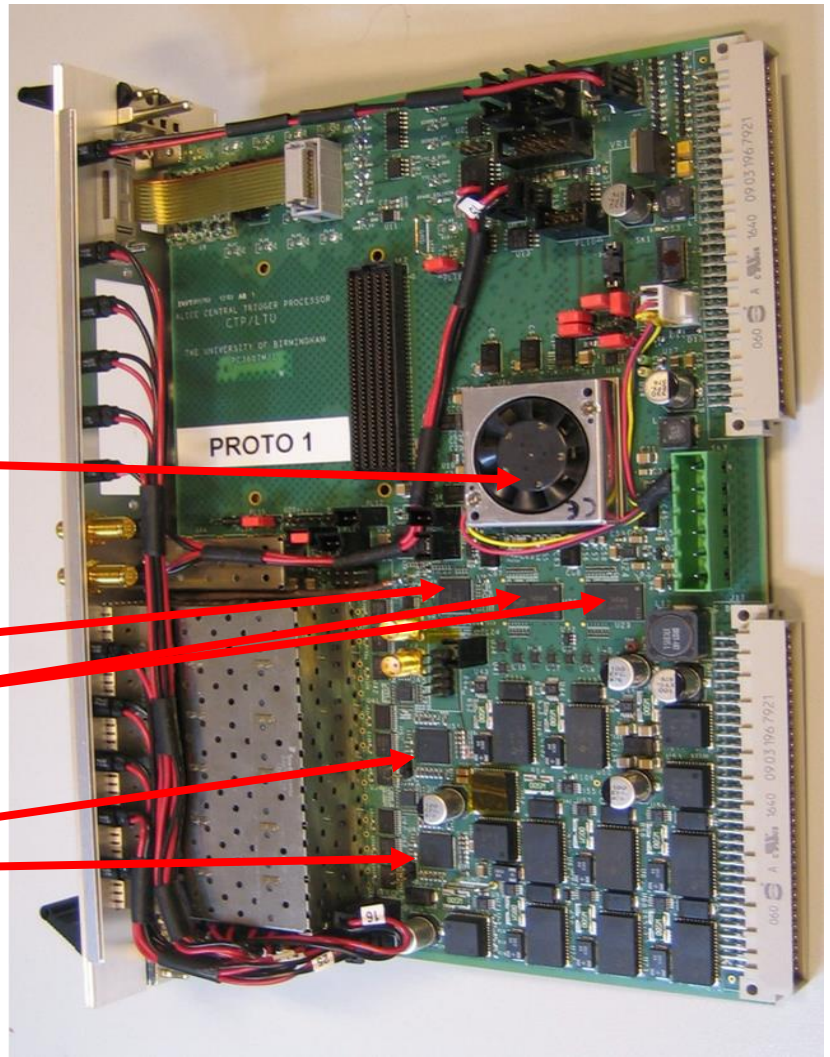
2 x PLL Si5345

2 x DDR4 memory

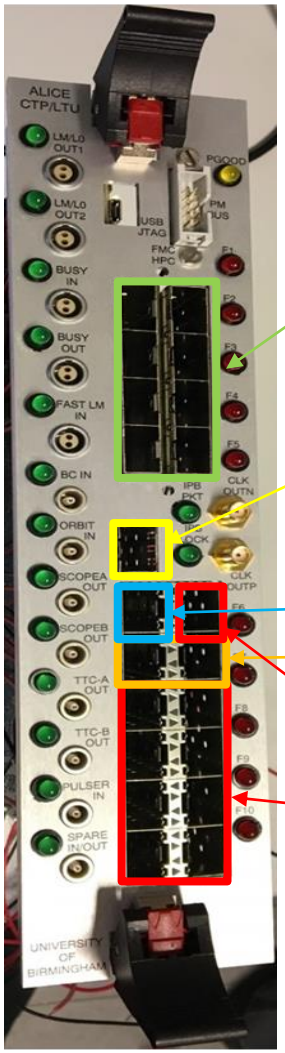
12 SFP+ for OLT/ONU/GBT

2 x UCD90120A





CTP/LTU board interfaces



Optional FMC card:

- FMC CTP card (trigger inputs)
- Commercial FMC S-18 card with 7 x SFP+ (GBT)

IPbus interface:

- ABCU-5740ARZ for 1G copper Ethernet
- AFBR-709DMZ for 1G optical Ethernet

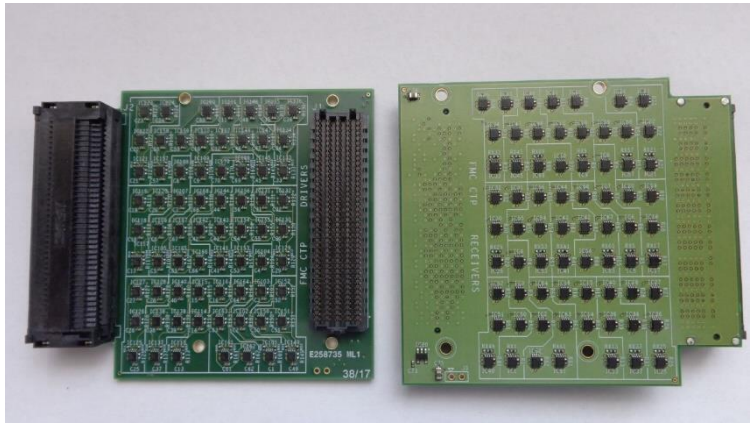
TTC-PON ONU (link to CTP)

GBT (trigger distribution + link to DAQ)

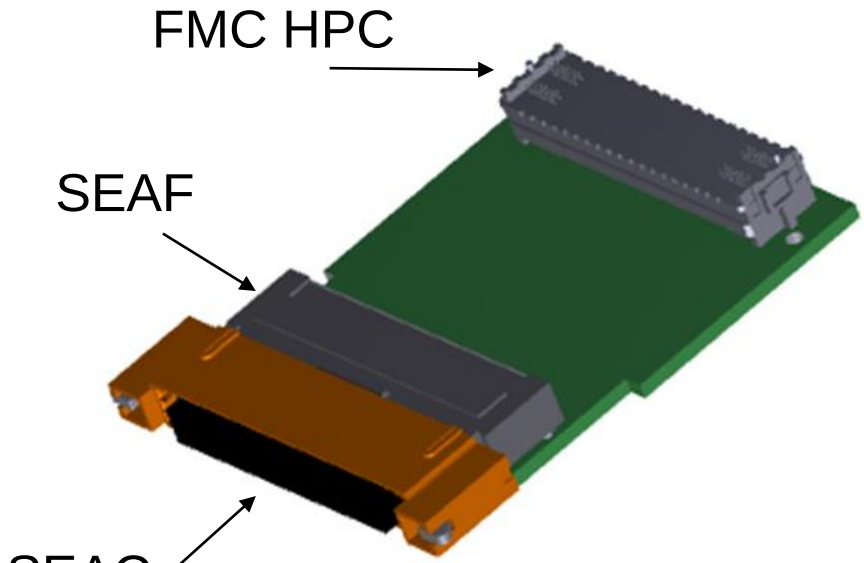
9 x OLT (links for CTP-CRU connection)

FMC CTP card

- FIN1101K8X, LVDS Single Channel Repeater
- 0-ohm resistors for input or output configuration
- M24C02-WDW6TP Serial EEPROM -> stored configuration of FMC card
- 70 diff. links for data
- 2 diff. links for clocks

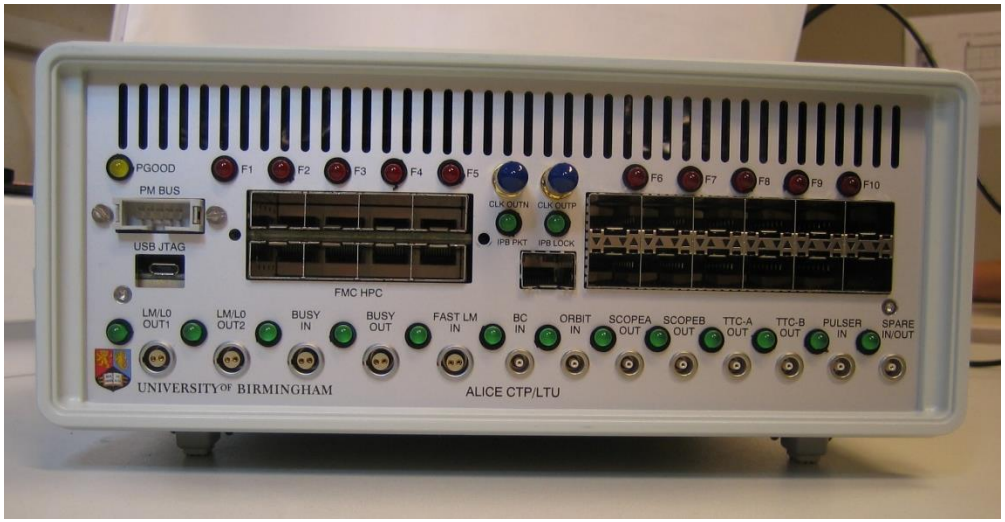


FMC CTP prototype



Samtec SEAC with 72 diff. pairs

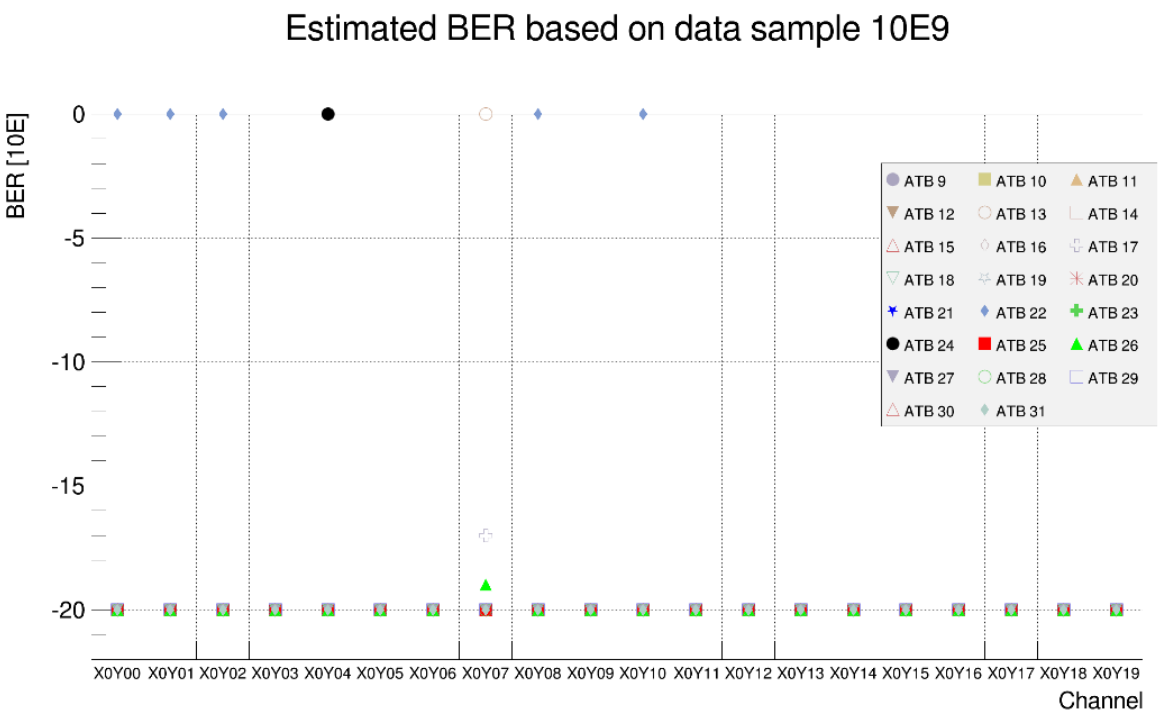
ELMA box for CTP/LTU board

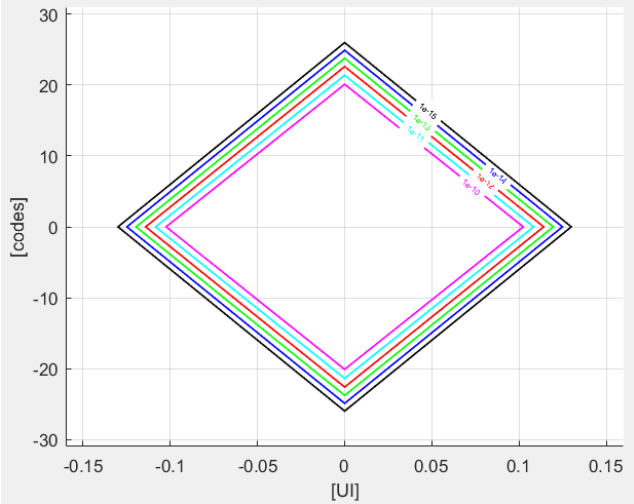


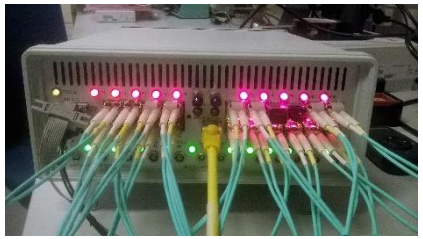
- Standalone unit for laboratory usage
- 2 internal AC-DC power supplies
- 2 fans for cooling
- Power switch + fuse

Test results for 1st production batch (23 boards)

IBERT+ (In-system BER Test)

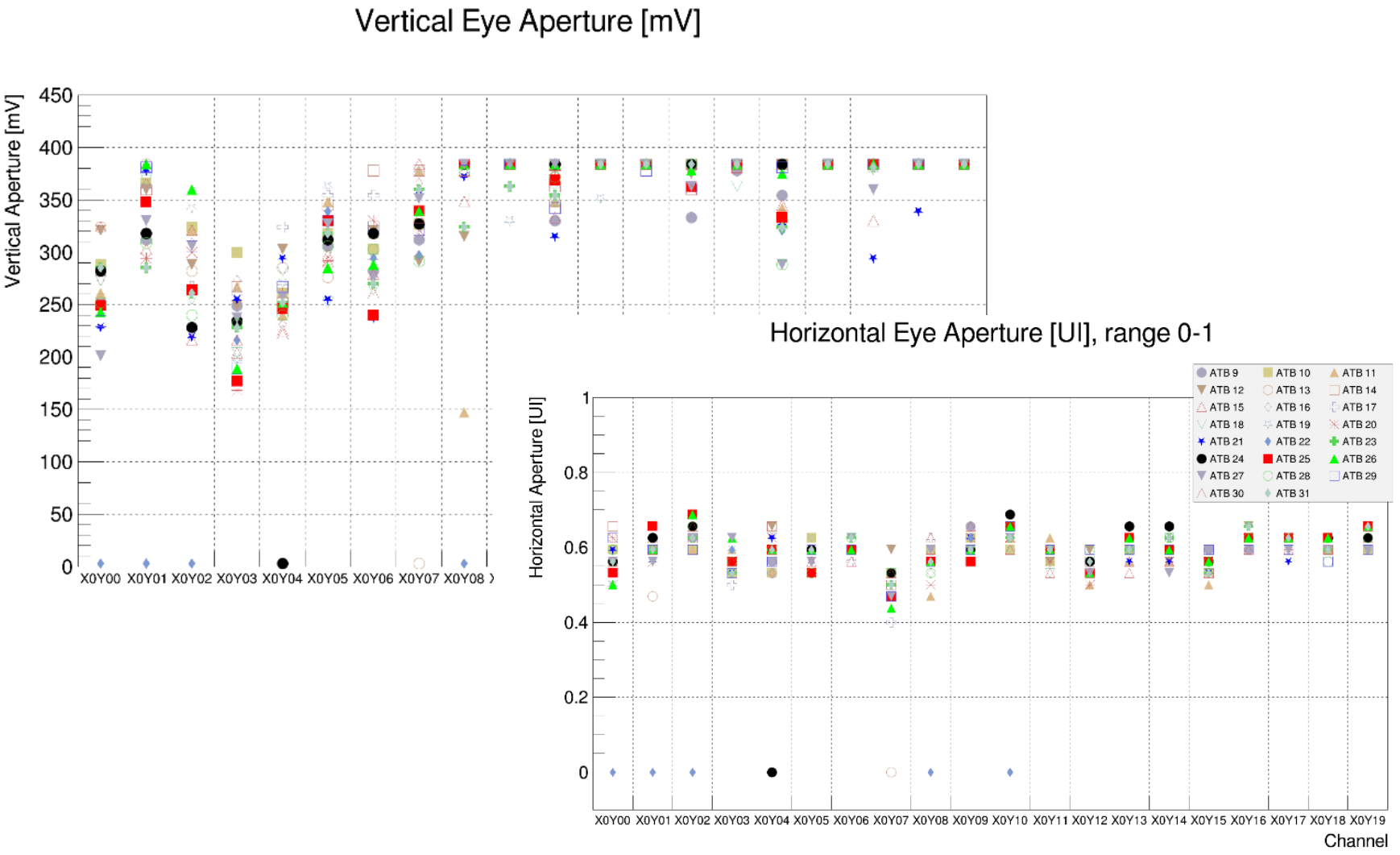




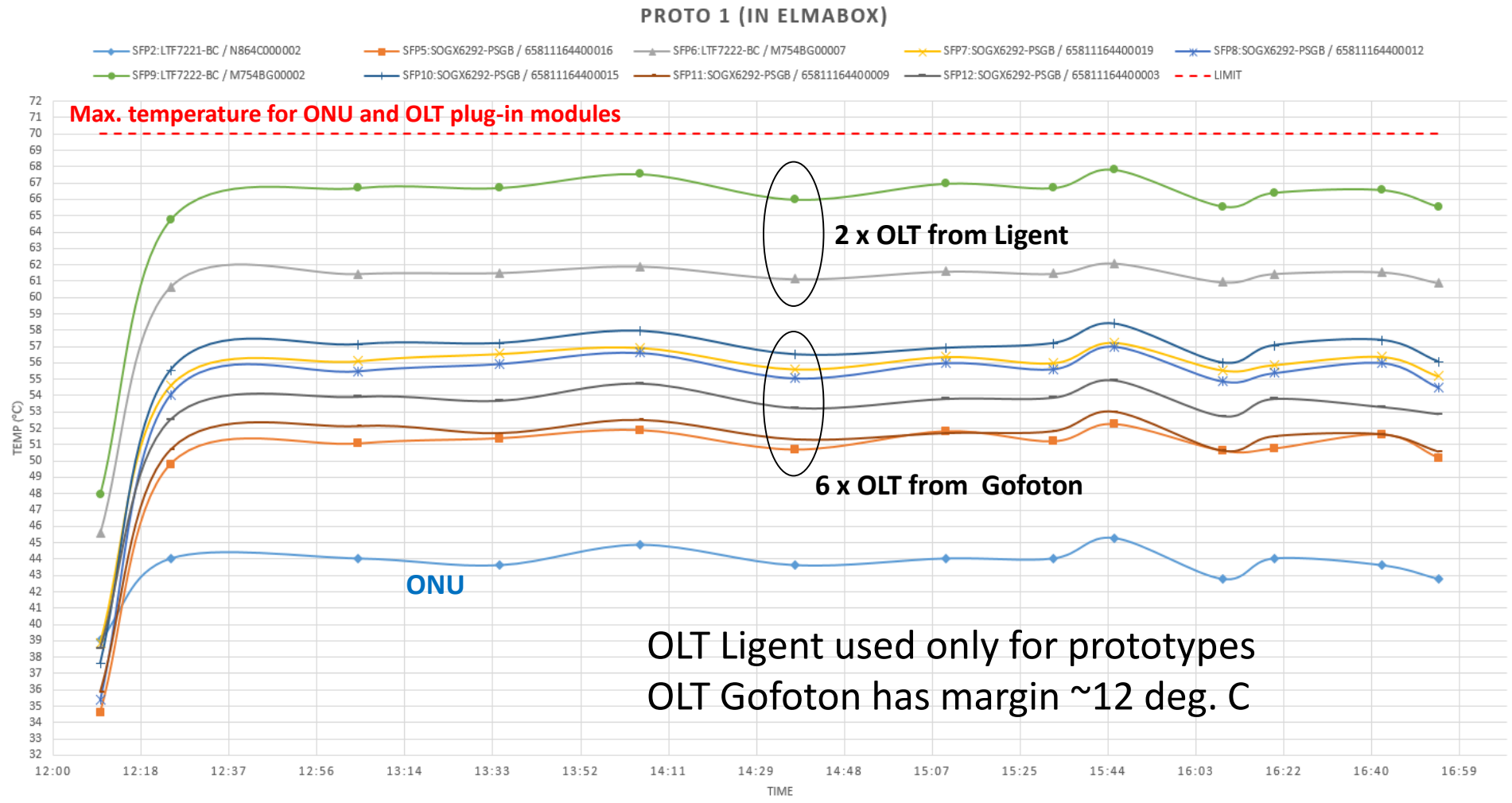


- Xilinx IBERT design improved by using GT debugger and TCL script for automation of BER measurement
- TCL script uses the mask for Xilinx GTH + additional values for SFP+ module
- 3 out of 23 boards from 1st batch were sent back to assembly company for repairs

IBERT+ (In-system BER Test)



Temperature test for OLTs and ONU (ELMA box, room temperature ~20 deg. C)

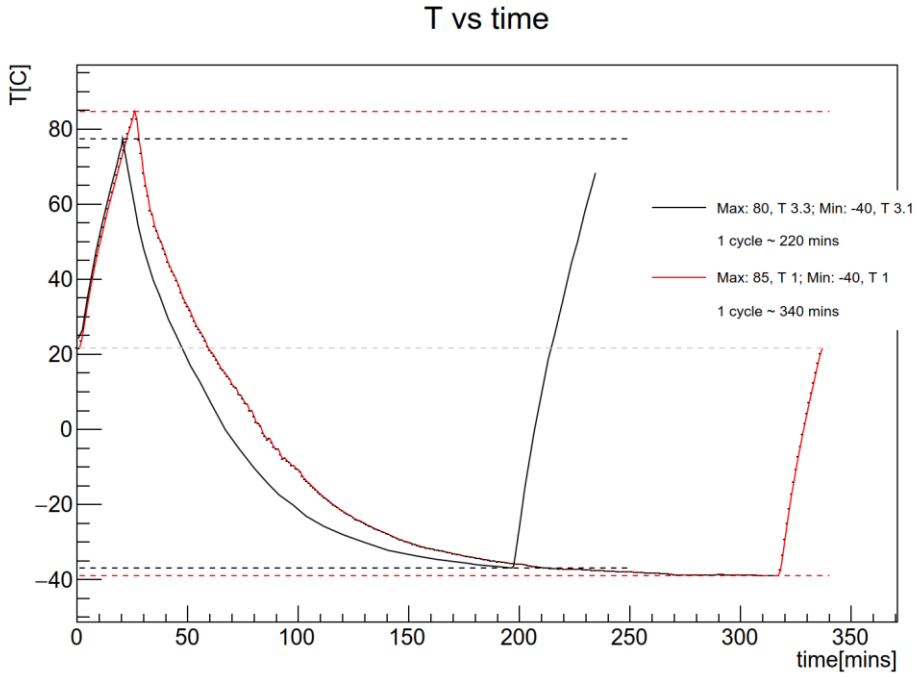


OLT Ligent used only for prototypes

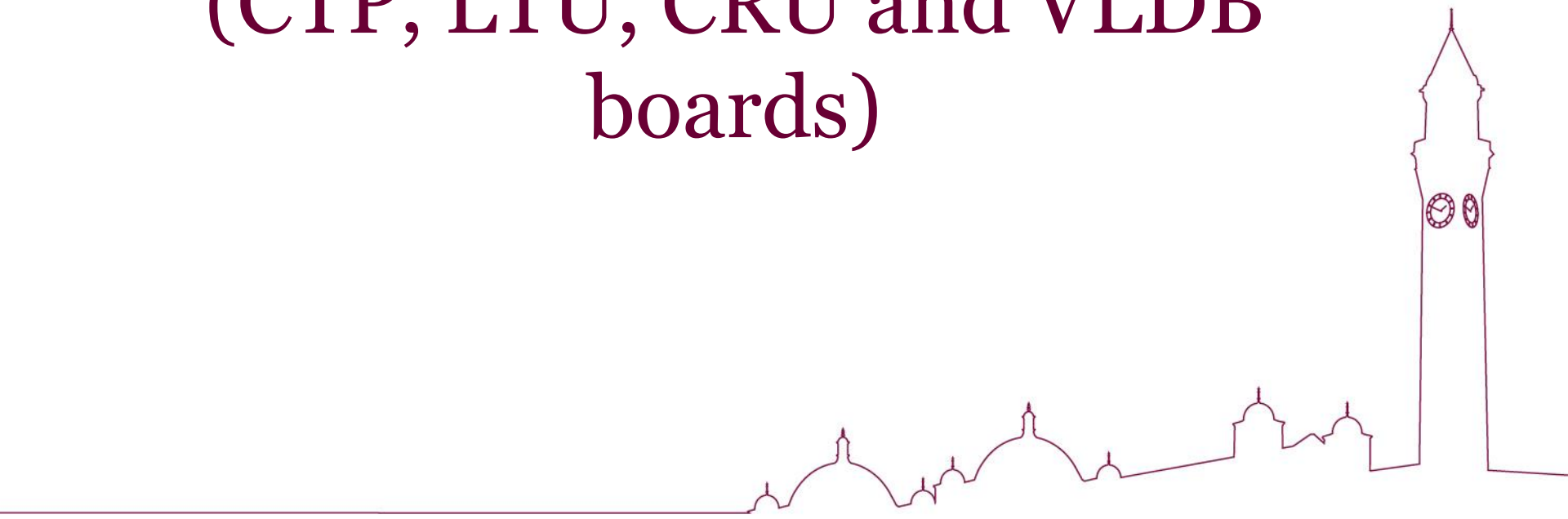
OLT Gofoton has margin ~12 deg. C

The stress test for CTP/LTU boards

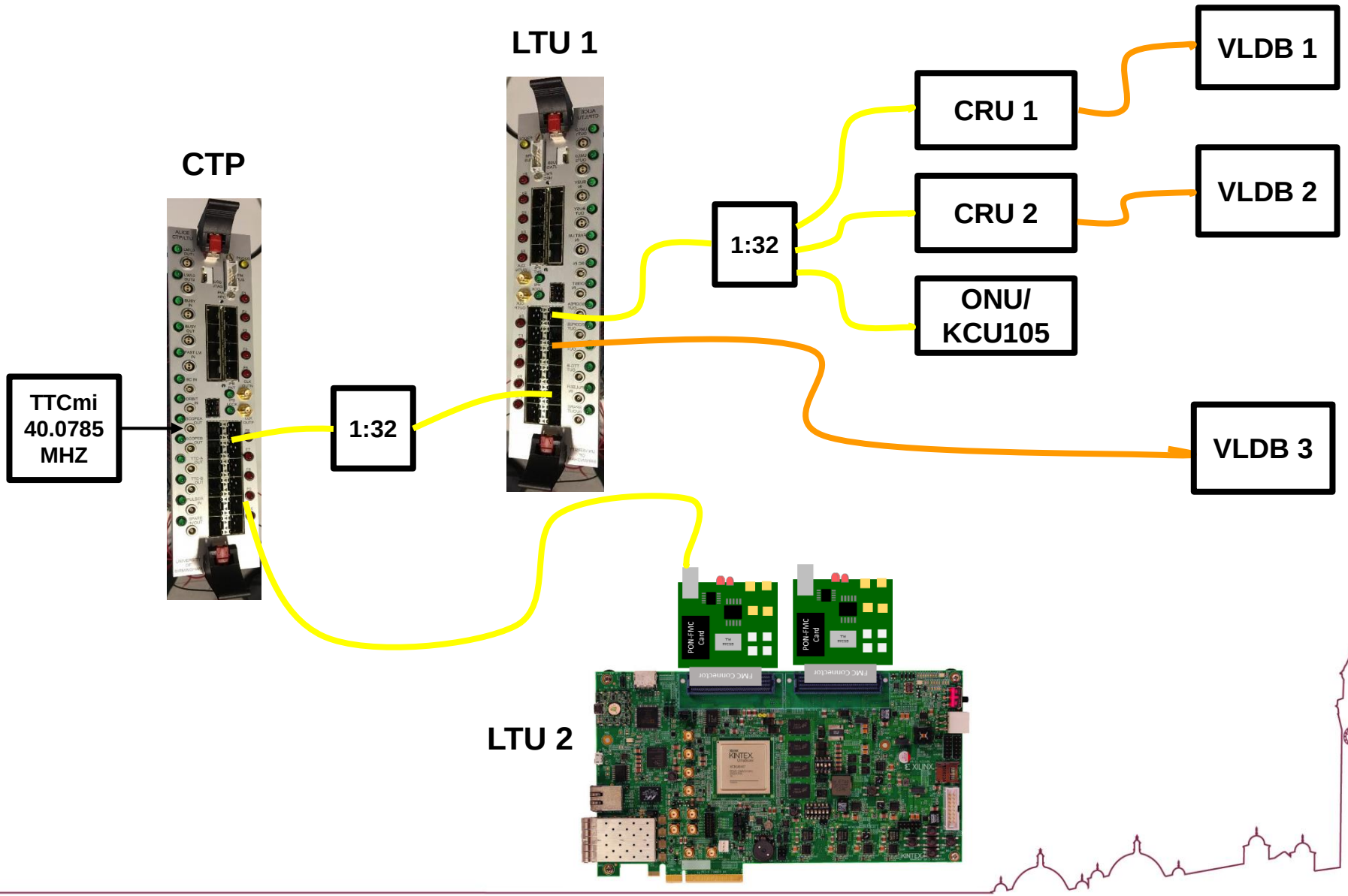
- 4 CTP/LTU boards inside the climate chamber at CERN el. pool
- 100 + 25 temperature cycles from -40 to 85 deg. C
- Each cycle is 340 min.
- 1 out of 4 boards has broken high-speed channel



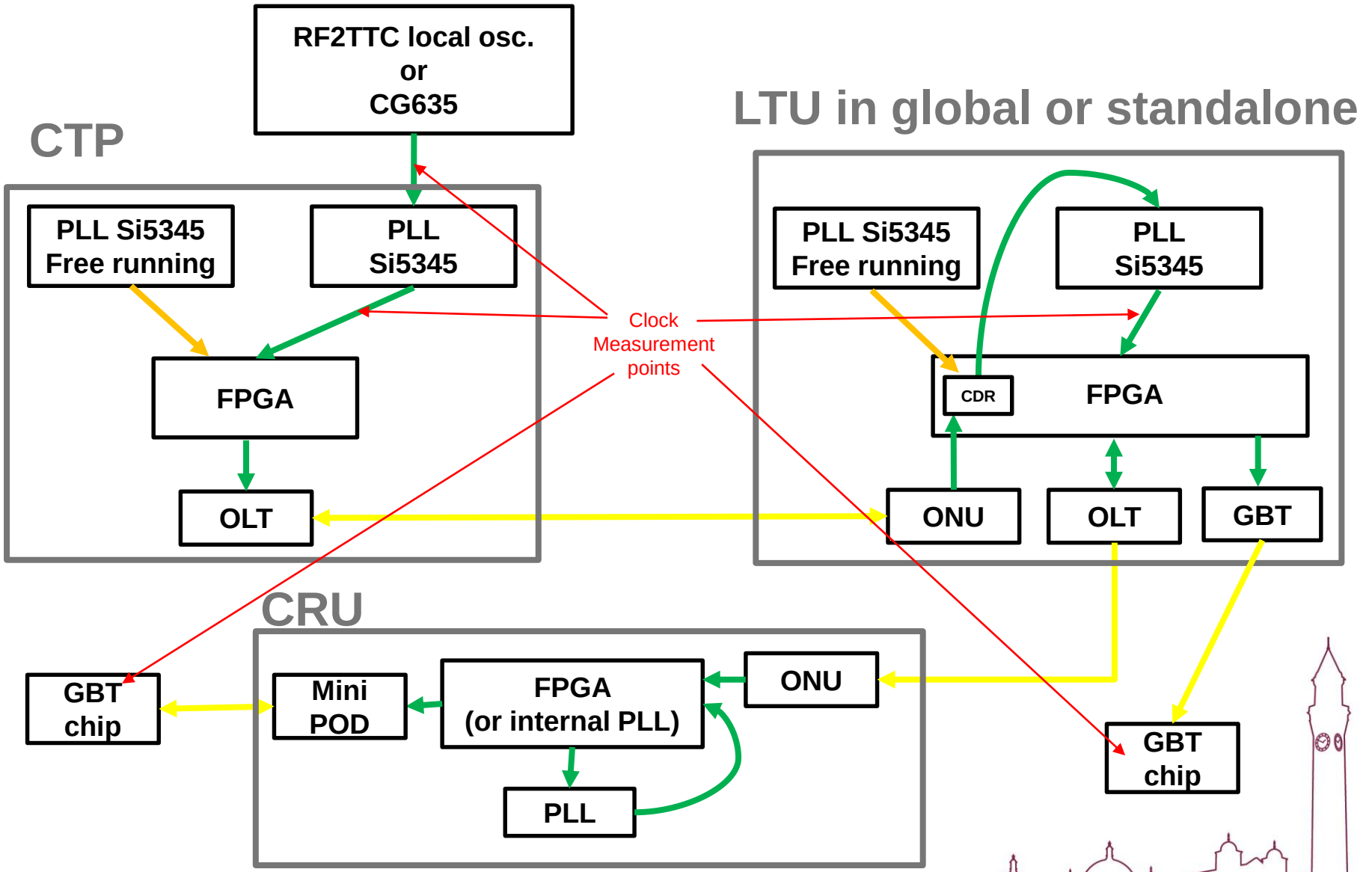
Implementation and test of TTC-PON for ALICE trigger system (CTP, LTU, CRU and VLDB boards)



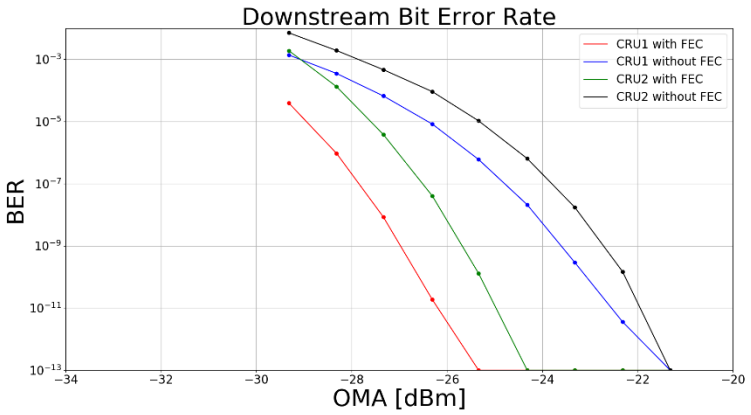
CTP-LTU-CRU-VLDB test setup

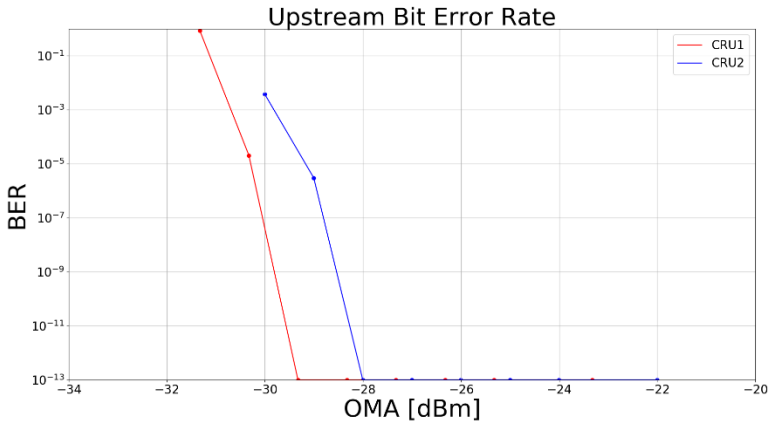


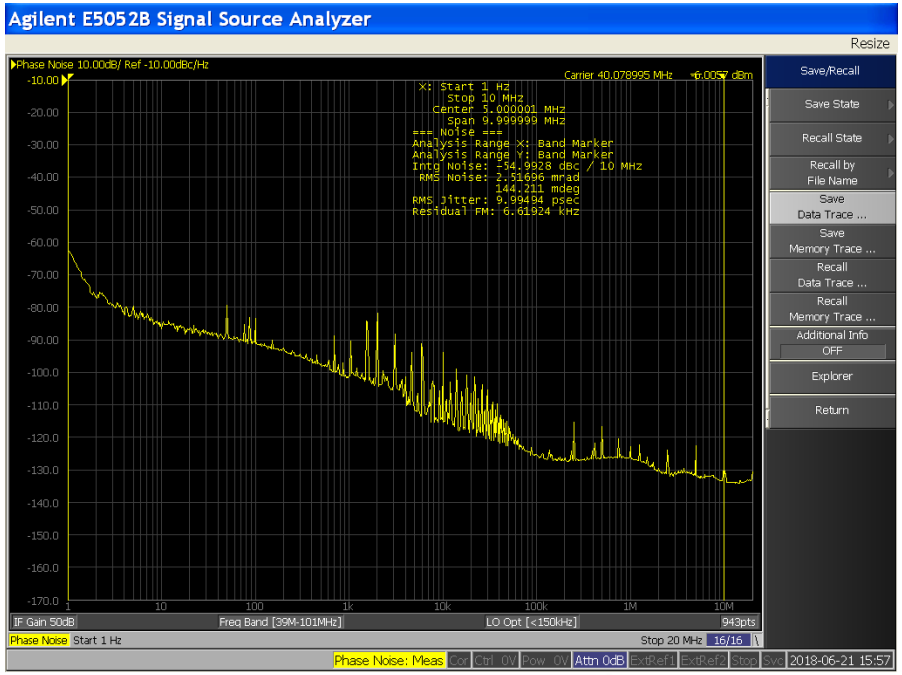
Overall clocking scheme



TTC-PON characterization using CTP, LTU, CRU and VLDB boards



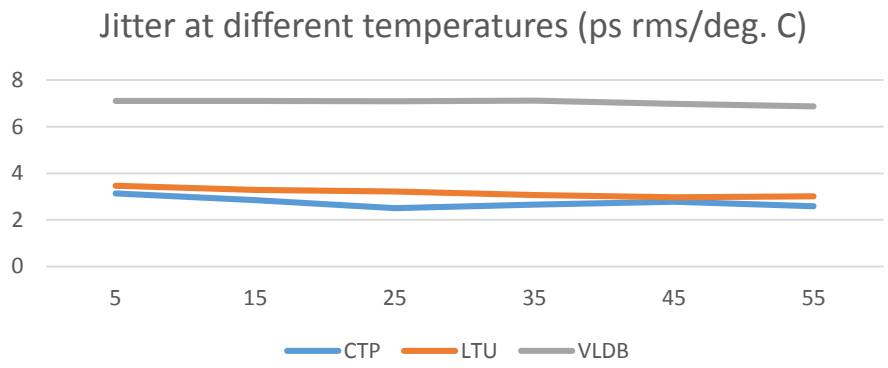




There is the optical margin ~8 dB
(using TTC-PON splitter 1:64)

Jitter measured on GBTx
(connection through CRU)
~ 10 ps rms

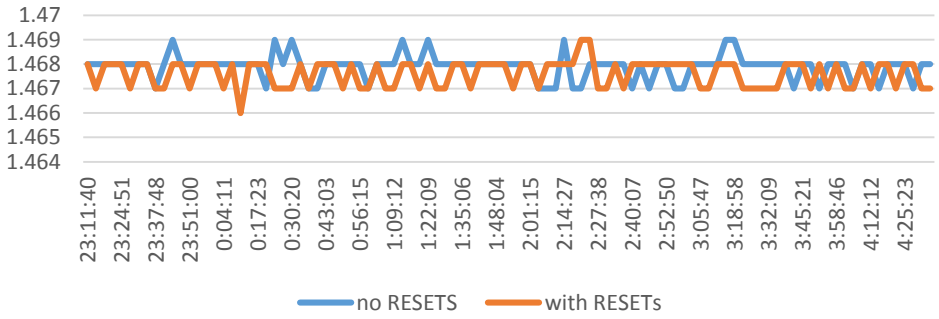
Jitter measurement on CTP, LTU and VLDB boards at different temperatures (only CTP and LTU inside the temperature chamber)



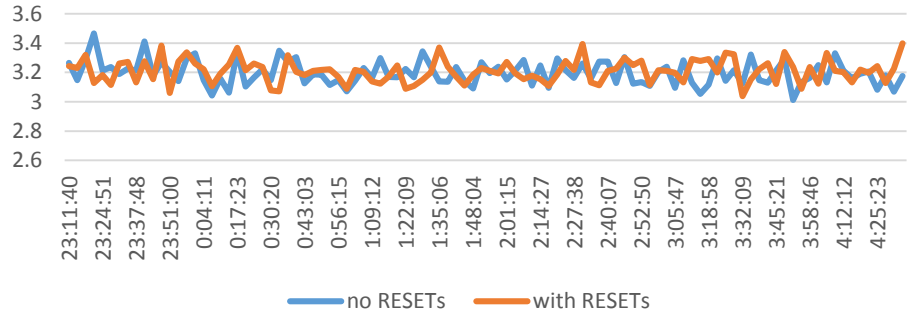
Jitter is stable in the temperature range 5-55 deg.C

Fixed clock phase measurement

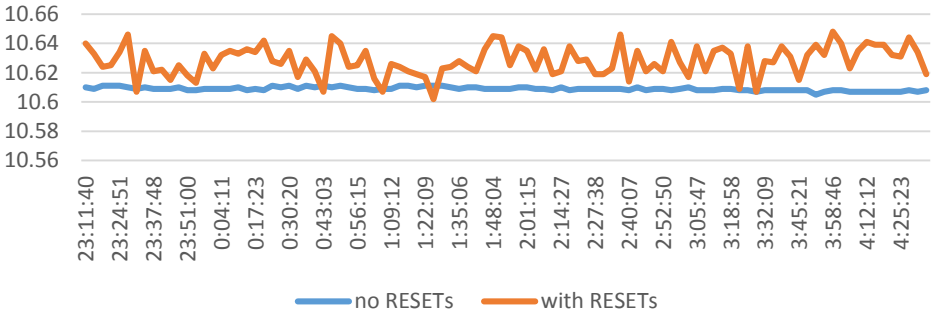
Means (ns) for REF->CTP skew at 35 deg. C



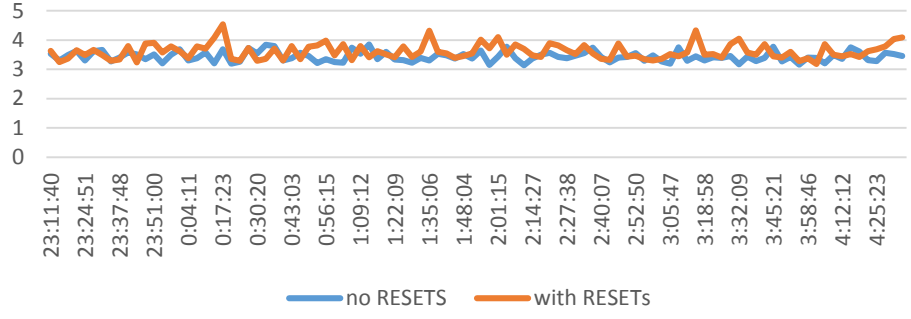
Standard deviatios (ps) for REF->CTP at 35 deg. C



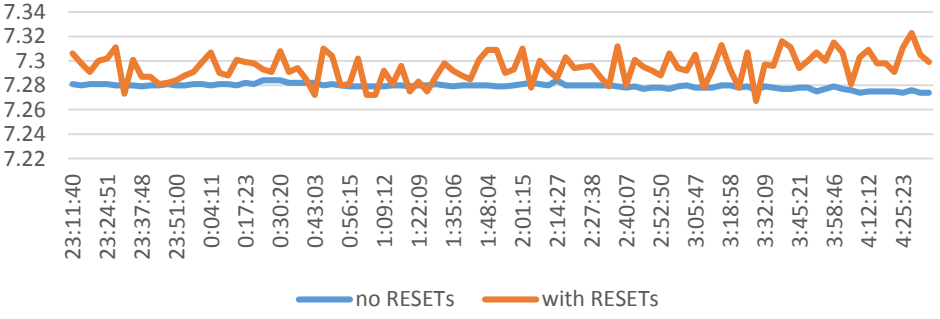
Means (ns) for REF->LTU skew at 35 deg. C



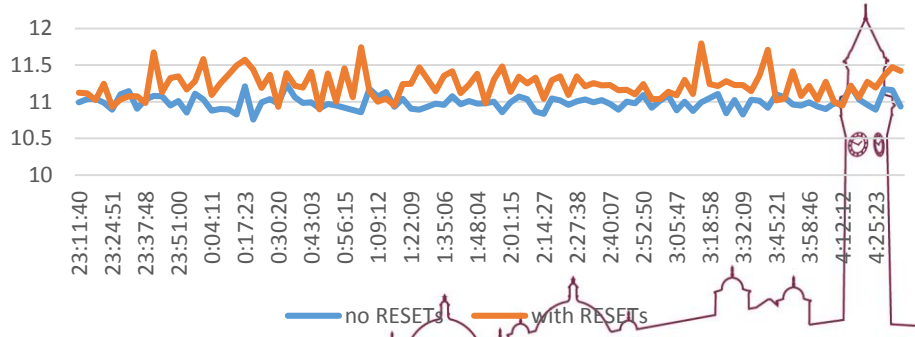
Standard deviations (ps) for REF->LTU at 35 deg. C



Means (ns) for REF->GBTx skew at 35 deg. C



Standard deviations (ps) for REF->GBTx at 35 deg. C



Fixed clock phase measurement

We took ~500k measurements between RESETs of whole chain (CTP PLL, CTP OLT, LTU ONU, LTU PLL, LTU OLT, LTU GBT).

Measurement at 35 deg. C:

- REF-CTP skew
  - Means range 2 ps -> 3 ps
  - Standard deviations range 3 - 3.5 ps -> 3 - 3.5 ps
- REF-LTU skew
  - Means range 3 ps -> 50 ps
  - Standard deviation range 3.1 - 3.8 ps -> 3.2 - 4.5 ps
- REF-GBTx skew
  - Means range 10 ps -> 60 ps
  - Standard deviation range 10.75 - 11.2 -> 10.9 – 11.8 ps

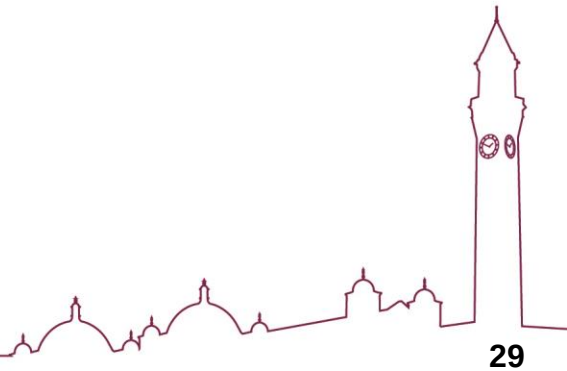
Test summary

- Board tests:
  - Voltage-ripple measurement for high speed banks of FPGA
  - All interfaces tested (IPbus, DDR4, Flash, PLL, …)
  - Temperature measurements with all types of SFP/SFP+ plug-in modules
  - IBERT+ measurement
  - Stress test (temperature cycling)
- System tests
  - TTC-PON -> OLT to 23 x ONUs
  - Full system chain
  - Clock-quality measurement (jitter, fixed clock phase stability)
- All tests passed requirements

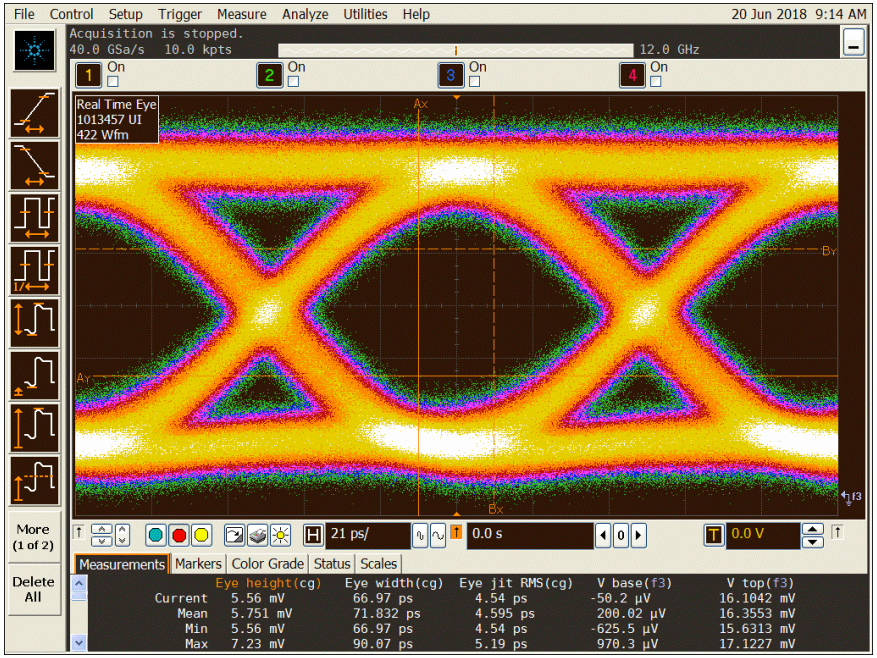
Summary

- ALICE Trigger Upgrade will keep
  - concept of Central Trigger Processor (CTP) and Local Trigger Units (LTUs) for each sub-detector
- Design centred around universal CTP/LTU board
  - using Xilinx Kintex-Ultrascale FPGA
- New TTC-PON system fully qualified for trigger distribution
- 1st production batch completed – 23 CTP/LTU boards
- Intensive testing has shown no design faults
- 2nd batch of production will start very soon – 31 CTP/LTU boards
- Integration test with sub-detectors has started
- Overall project on schedule

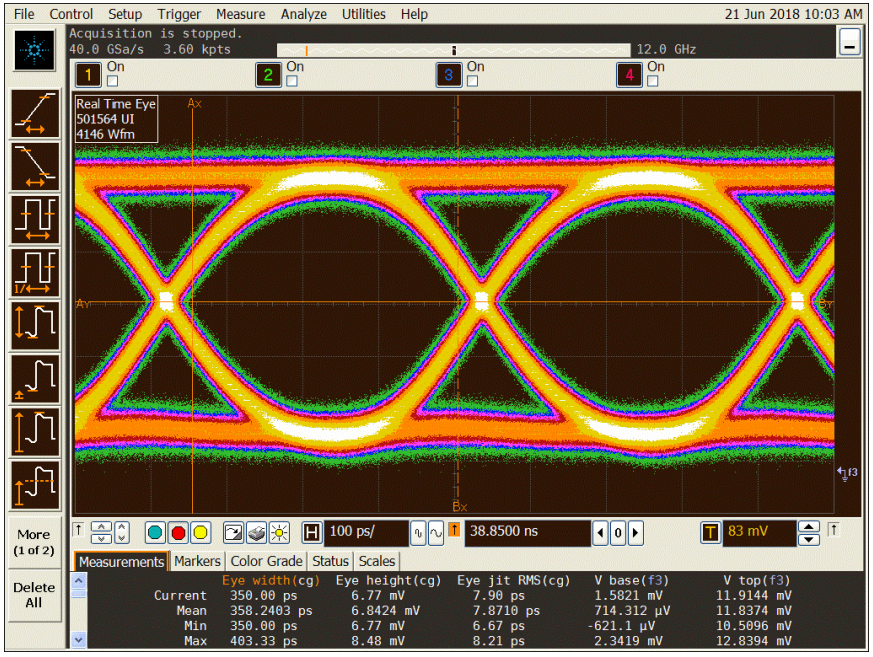
Back-up slides



TTC-PON characterization using CTP, LTU, CRU and VLDB boards



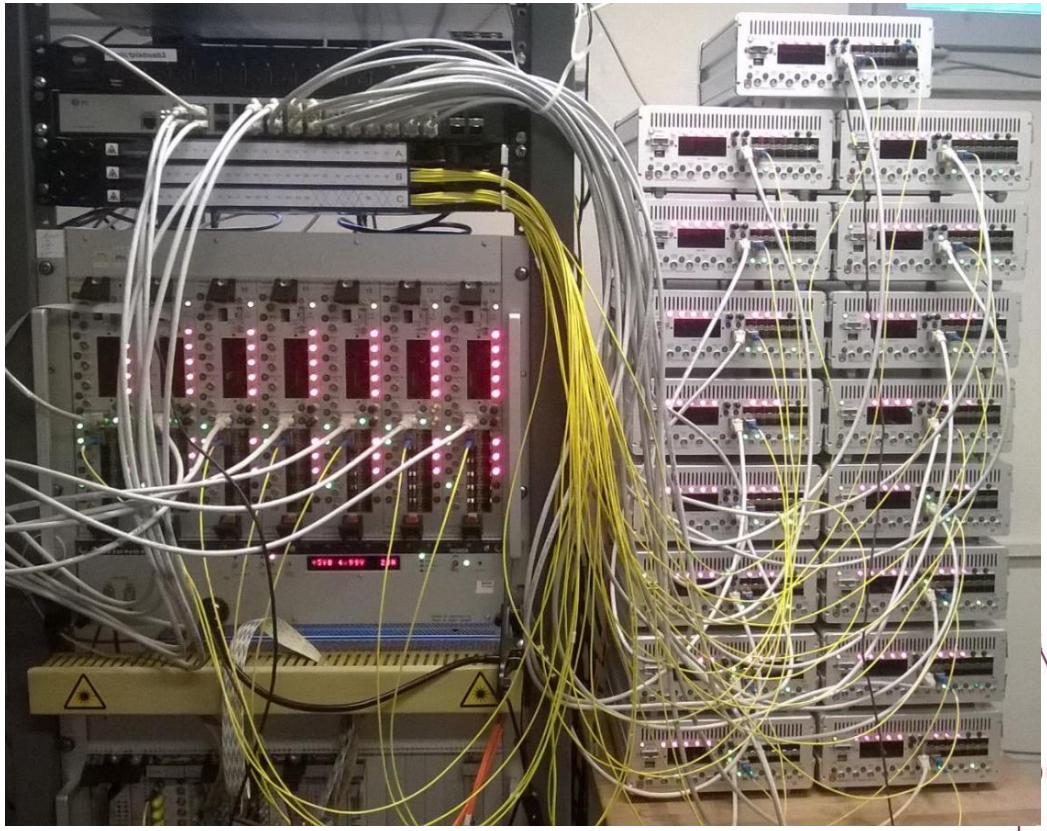
Downstream Eye diagram (serial data measured by optical probe)



Upstream Eye diagram (serial data measured by optical probe)

TTC-PON: OLT to 23 ONU test

- Verification of:
  - TTC-PON calibration sequence with max. possible number of ONUs
  - System stability
  - Downstream BER
  - Upstream BER



Power for CTP/LTU board

- 2 x power sequencer UCD90120A
- DCS monitoring of V,I and T via Fusion Digital Power Designer command line (PMbus connector on the front panel)
- All PGOOD signals connected to log. OR for PGOOD LED on the front panel