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ALICE trigger system for LHC Run 3

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The ALICE Central Trigger Processor (CTP) will be upgraded for LHC Run 3 with completely new hardware and a new Trigger and Timing System (TTS) based on a Passive Optical Network (PON) system. A new universal trigger board was designed which can function as a CTP or as a LTU. It is based on the Xilinx Kintex Ultrascale FPGA and upgraded TTC-PON. The new trigger system and the results of the tests and verification of the first 23 boards, produced at the beginning of 2018, will be presented.

Summary

In LHC Run 3 the interaction rates in ALICE at point 2 will increase to 50 kHz for Pb-Pb, and 200 kHz for pp and p-A. In addition, where feasible a safety margin of two is applied in the system design. The aim of the ALICE trigger system is to select essentially all of these interactions. The new ALICE CTP will be based on 3 trigger latencies (LM at 650 ns, L0 at 900 ns and L1 at 6.5 μs) with regular "Heartbeat"(HB) triggers for detectors running in continuous mode. The trigger system must also cope with detectors that still have dead-time during the readout. It is based on the Xilinx Kintex Ultrascale FPGA and it has several interfaces: upgraded TTC-PON, GBT, IPbus, I2C, SPI and also the original TTC. The board is equipped with 2 DDR4 memories (each 1 GB) and it can be equipped with a maximum of 20 SFP+ modules. A complex power system on the board is controlled by a UCD90120A power sequencer and is monitored via PMbus. The main interface between the LTU and the CRU (Common Readout Unit) will be TTC-PON, but the ITS and MFT detectors will also receive triggers directly at their FEE via GBT (in parallel to CRU via TTC-PON) due to trigger latency constraints. The interface between the CTP and the LTU is also based on TTC-PON. The LTU will collect all BUSY signals (TTC-PON time multiplexed upstream) from the detectors and forward these to the CTP where an overall BUSY mask will be built.
In the first production phase 6 VME boards and 17 ELMA boxes are produced. Two types of firmware and software are developed for testing. The first type of firmware is dedicated for the test of high-speed links (20 SFP+ modules) and it is based on Xilinx IBERT design extended by GT debugger with associated VIVADO TCL script for BER estimation using data sample 10E9. The second type of firmware and software are used to test the functionality of all components connected to Xilinx Kintex Ultrascale FPGA (upgraded TTC-PON, GBT, IPbus, I2C, SPI, the original TTC and all components on the front panel). The basic version of CTP emulator including TTC-PON interface are tested by verification of a snapshot memory (DDR4 memory 1 GB) on a transmitter and receiver side. Cascaded TTC PON similar to the Alice trigger system for LHC Run 3, is built and will be used to verify the system functionality. Afterwards the boards will be given to the detector' s laboratories with appropriate firmware and software and will be used to integrate these into their systems. The second production phase will be initiated in autumn of this year.

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