Jets and topological trigger selection performed with the last generation Xilinx FPGA
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ATLAS trigger system

Introduction

**jFEX**

**L1Topo**

ATLAS trigger system

- **Preprocessor**: \( \text{aMC@NLO} \)
- **Level-1 calorimeter**
  - Electron/Tau: CMMX
  - Jet/Energy: CMMX
  - \( g/e/j/FEX \)
- **Central trigger**
- **Tile calorimeter D-layer**
- **Muon detectors including NSW**
- **Endcap sector logic**
- **Barrel sector logic**
- **MUCTPI**
- **Topology**
- **CTP**
  - **CTPCORE**
  - **CTPOUT**
- **Output**
  - FE
  - ROD
  - ROD

**Level-1 (\(< 2.5 \mu s)\)**

**Regions Of Interest**

**High Level Trigger**
- **FTK**: Fast TracKer

**DataFlow**
- **Data Collection Network**
- **Event building**
  - 6.5 kHz: 10 GB/s
  - 12 kHz: 29 GB/s

**SubFarm Output**
- 600 Hz: 960 MB/s
- 1 kHz: 2.4 GB/s

**Fig. 1**: Block diagram of the trigger and data acquisition system in 2016
- post Long Shutdown 1, Phase 0, Run-2 2015-2018 existing hardware
- post Long Shutdown 2, Phase 1, Run-3 2020-2022 hardware

**New conditions and requirements driving upgrade:**

- luminosity up to \( 2.5 \times 10^{34} \text{cm}^{-2}\text{s}^{-1} \)
- number of interactions per bunch crossing from \( \sim 40 \) up to \( \sim 60 \)
- increase of the trigger rates
- improve selection

**Fig. 2**: CERN facility
L1Calo Phase I upgrade

Fig. 3: Upgraded trigger system for Run-3

HUB - routes data produced locally in an ATCA shelf to the ROD
ROD - formats packets and sends them further to a FELIX system*

New possibilities
- unprecedented processing power located on FEX systems
  - dozens of Ultrascale and Ultrascale+ devices
- finer-granularity input from LAr Calorimeter
- more complex and efficient algorithms

*"FELIX: developing a new detector interface for ATLAS trigger and readout", Gokhan Unel, Th. 14:50
jFEX ATCA blade architecture requirements

- cope with data amounting to ≈ 3.1 Tbps
- incorporate 240 Gbit receivers - 24 MiniPODs: 20 RX and 4 TX optical lines
- 4 Xilinx Ultrascale+ FPGA devices: XCVU9PXCVU9P -2FLGA2577E
- modular design - each FPGA has symmetric PCB layout but high speed lanes are not crossing each other to maintain signal integrity
- two mezzanine cards for control and power

Fig. 4: jFEX ATCA blade block diagram

Fig. 5: jFEX final prototype has a 24 layer MEGTRON6 PCB
90 fs RMS Si5345 jitter cleaner chip located on control mezzanine card
- measurements done with spectrum analyser
- measured jitters values are within Xilinx specifications

Fig. 6: jFEX clock distribution

Fig. 7: jFEX clock distribution quality measurement

<table>
<thead>
<tr>
<th>frequency</th>
<th>Xilinx Specs</th>
<th>Measurement</th>
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<tbody>
<tr>
<td>10 kHz</td>
<td>-112 dBc/Hz</td>
<td>-137.14 dBc/Hz</td>
</tr>
<tr>
<td>100 kHz</td>
<td>-128 dBc/Hz</td>
<td>-143.83 dBc/Hz</td>
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<tr>
<td>1 MHz</td>
<td>-145 dBc/Hz</td>
<td>-147.62 dBc/Hz</td>
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</table>
Power supply - features

- Power mezzanine cards equipped with iJX series TDK Lambda devices
- iJXA and iJXB series can deliver up to 35/60 A respectively
- One mezzanine power card per FPGA plus one board mezzanine
- PMB bus to control and monitor
- LTC1696 over-voltage protection chip
- Additional linear regulators for VCC Aux and MGT VCC Aux are used directly on jFEX board
- Power sequencing is controlled by CPLD
**Power supply - ripple voltage and jFEX power consumption**

- ripple voltage within Xilinx specifications - should be less than 10mV
- total power consumption below 300W when 120 MGTs enabled at 11.2 Gb/s
- MGTYAVCC and MGTYAVTT properly estimated by Vivado tool but not VCCINT
- jFEX FPGAs cores temperature in average $\sim 70^\circ$, well below allowed. This is when 120 MGTs were enabled with loop-back mode

<table>
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<tr>
<th>FPGA</th>
<th>MGTAVTT (V pk-pk mean)</th>
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<tbody>
<tr>
<td>U1</td>
<td>1.63291 mV</td>
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<tr>
<td>U2</td>
<td>2.9927 mV</td>
</tr>
<tr>
<td>U3</td>
<td>4.0223 mV</td>
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<tr>
<td>U4</td>
<td>4.072 mV</td>
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</table>

<table>
<thead>
<tr>
<th>FPGA</th>
<th>MGTAVCC (V pk-pk mean)</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1</td>
<td>1.5149 mV</td>
</tr>
<tr>
<td>U2</td>
<td>2.9019 mV</td>
</tr>
<tr>
<td>U3</td>
<td>3.1719 mV</td>
</tr>
<tr>
<td>U4</td>
<td>2.7942 mV</td>
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</table>

**Fig. 9:** jFEX ripple voltage within Xilinx specification

**Fig. 10:** jFEX power consumption

**Fig. 11:** jFEX temperature, fan speed equals 11 (max. is 15)
Gbit transmission lines validation

- **FEX Test Modules** used to generate all data streams
- LHC clock delivered by FTM module via backplane
- BER $< 15 \cdot 10^{-15}$ at 11.2 Gbit/s, PRBS31 data

**Fig. 12:** jFEX eye diagram, left/right one best/worst case

**Fig. 13:** jFEX Gbit transmission lines test setup

**Fig. 14:** jFEX eye diagram area scan at 11.2 Gbit/s
all firmware blocks are implemented - still require thorough tests and integration

FPGA resource usage is on the safe side - below 50%

six jFEX boards are required to cover whole available $\eta$ and $\phi$ range

Fig. 15: jFEX data flows from MGTs to Real Time Data Path (RTDP) where it is de-serialized, de-skewed and aligned. After this stage it can be used by algorithms where Trigger Objects (TOB) representing jet candidates are formed. Next input data or algorithms results are sent either to read-out or to be processed by L1Topo ATCA blades.
All basic versions of algorithms are also implemented and LUT resource usage is below 20% for central region of calorimeter.

Fig. 16: Algorithm firmware infrastructure. Data is delivered from calorimeters with $0.1 \times 0.1$ granularity in $\eta$ and $\phi$ coordinates.
**L1Topo algorithms already used in Run 2**

**Topological calculations based on TOBs**

- select events based on the geometric and kinematic relationships between trigger objects identified in earlier stages
- cuts on angular distributions - $\Phi, \eta, \Delta \Phi, \Delta \eta, \Delta R = \sqrt{\Delta \eta^2 + \Delta \Phi^2}$
- missing, invariant and transverse mass calculations
- compound triggers - $e/\gamma, jets, \mu, \tau, E_T^{miss}$
- combining information both from calorimeter and muon system
- dozens of triggers created by L1Topo which initiates hundreds of different trigger chains
- **Topo system was commissioned, validated and used for physics data taking**

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**Fig. 17:** Level 1 rates before prescale versus instantaneous luminosity for L1 di-tau chains. All chains require two isolated hadronic taus with $E_T > 20,12$ GeV. With L1Topo it was possible to use $\Delta R$ relation between tau candidates and additional condition on jet not overlapping with those candidates. It reduces trigger rate without loss in the signal efficiency.
L1Topo algorithms and hardware for Run3

- L1Topo hardware based on the jFEX design - copied modular parts
- 118 inputs and 20 outputs per blade
- since these boards incorporate two Ultrascale+ devices PCB has only 20 layers
- additional electrical and optical connection to Central Trigger Processor
- for Run 3 there will be three L1Topo ATCA blades in use
- algorithms and firmware from Run 2 will be re-used for Run 3
- receiving additional types of TOBs like large area jets
- much lower fraction of FPGA resource usage - it was up to 78%. Now for the same algorithms used in Run 2 but new Ultrascale+ devices it is below 25%
Summary

- ATLAS jFEX trigger boards are fully tested and ready for final production.
- Firmware for jFex and L1Topo boards is in a very advanced stage and selected FPGA devices will satisfy hardware and firmware needs.
- Modular design copied from jFEX to L1Topo gives us confidence that L1Topo hardware tests will soon be successfully completed.

We plan to start hardware and firmware commissioning with other trigger subsystems this year.