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Jets and topological trigger selection performed with the last generation Xilinx FPGA

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For LHC Run3, ATLAS is planning a major detector and trigger upgrade. The new Feature EXtractors (FEXs) system will allow to reconstruct different physics objects for the Level-1 calorimeter trigger selection. This includes a Jet FEX, which will identify small/large area jets and MET.
An upgraded L1 Topological Processor will allow to select interesting physics events applying topological constraints.
To achieve up to ˜3 Tb/s input bandwidth and substantial processing power with tight latency budget of <390 ns, the trigger boards host up to four Ultrascale+ FPGAs. Design and test results of full-scale prototypes from integrated tests will be reported.

Summary

To cope with the enhanced luminosity at the Large Hadron Collider (LHC) in 2021, the ATLAS collaboration is planning a major detector upgrade to be installed during the Long shutdown 2 (LS2). As a part of this, the Level 1 trigger, based on calorimeter data, will be upgraded to exploit the fine granularity readout using a new system of Feature EXtractors (FEX), which each reconstruct different physics objects for the trigger selection and a new Topological Processor (L1Topo) that will process the Trigger Objects (TOBs) send by FEXs and select interesting physics events by applying kinematic and angular requirements on electromagnetic clusters, jets and total energy.
The jet Feature Extractor (jFEX) will identify small/large area jets and global variables exploiting a granularity of 0.1 x 0.1 in (η,ϕ) sent at 11.2 Gb/s from the calorimeters and will process the data and sort the TOBs using dedicated VHDL algorithms. The TOBs will be transmitted then at 12.8 Gb/s to the Topological Processor via optical links.
The L1Topo system has been introduced in Run 2 to improve the trigger performance by correlating trigger objects, such as electromagnetic clusters, jets and muons, and global quantities. The system performs topological calculations on the first trigger stage, for example invariant or transverse mass cuts, angular cuts on Δphi or Δ R or jet energy sums and fat jet clustering. During LS2, upgraded L1Topo modules will be installed benefiting for a larger processing power available for the implemented VHDL algorithms.
The jFEX and L1Topo modules exploit the latest generation of the Xilinx Ultrascale+ FPGA, XCVU9P-2FLGA2577E, characterised by large input bandwidth, up to ˜ 3Tb/s per module, and large processing power. Both boards have stringent latency requirements, < 390 ns, and significant density of high speed signals.
The contribution focuses on the design challenges and solutions of the two ATCA board designs reporting on the simulation studies performed in parallel to the design to optimise signal integrity, power, current and thermal distribution. The material used for the PCB is MEGTRON6, which is required to transmit signals at speeds higher than 10 Gb/s. The jFEX stack-up consists of 24 layers, symmetric distribution and micro-vias connecting the layers with high speed signals, while the L1Topo consists of 20 layers due to the smaller number of mounted FPGAs. Results of test campaigns in house and at integrated tests at CERN of final full-scale prototypes will be presented. The full system will be produced by early 2019 to allow for completion of installation and commissioning before LHC restarts in March 2021.

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