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A high integration and low power ASIC with TOT front-end and waveform sampling for MRPC applications

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FEEWAVE is an ASIC designed for Multi-gap Resistive Plate Chamber (MRPC) for good time resolution. As a highly integrated chip, the ASIC includes front-end circuit, waveform sampler, and analog-digital conversion. The chip implements Time over Threshold (TOT) function and waveform digitization. It has high speed sampling rate (5 GS/s) and high trigger rate capability (50 kHz). The ASIC is fabricated with 0.18 μm CMOS technology. In this paper, the design details of the chip will be given.

Summary

Multi-gap Resistive Plate Chamber (MRPC) is a gaseous detector working in avalanche mode with an excellent time resolution and a high detecting efficiency. It has been widely used as a particles identification detector in high energy physics experiments. One of the example is the endcap time-of-flight (ETOF) of Beijing Spectrometer III (BESIII). In order to achieve an overall time resolution of about 80 ps and higher integration for the detector upgrade, an ASIC is needed. The FEEWAVE ASIC discussed in this paper implements Time over Threshold (TOT) function and waveform digitization. By the TOT circuit, output pulse width is proportional to input charge. Furthermore, the waveform sampling function improves time resolution with calibration algorithm on the charge information from TOT output. The proposed ASIC has 4 channels. Each channel is integrated with a front-end circuit, an analogue memory with 256 cells, Wilkinson ADCs for every cell, and an output serializer. The front-end circuit consists of three parts, input stage, amplification stage and common mode feedback. By a common gate differential circuit, the input stage converts the current to voltage. Following by 5 differential amplifiers with low gain and high bandwidth, the output of the input stage is saturatedly amplified, while the output width is proportional to the input charge, therefore the TOT function is realized. The common mode feedback part is used to ensure correct biasing and implement threshold adjustment. The waveform digitizer can perform sampling with a high speed frequency of 5 GS/s and a depth of 256 points. Firstly, front-end circuit output waveform is sampled and held sequentially on a switch capacitance array with 256 cells. A 5 GHz Delay Lock Loop (DLL) provides a series of sampling clock. The A/D conversion is carried out in the Wilkinson ADC style. When a trigger comes, a common ramp is distributed to every cell and compared with the held voltage. At the meantime, a clock that is generated from a voltage controlled oscillator (VCO), is counted in each cell. When the ramp exceeds the held voltage, a stop signal is generated and the time stamp is latched. In this way, all the sampled voltage can be A/D conversion simultaneously and then the data will be read out by a high speed serializer with a clock of 200 MHz. Therefore, the dead time can be decreased and trigger rate can be as high as 50 kHz. Test setup has been designed for the chip measurement, and preliminary test results have been achieved.

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