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Prototype Front-end ASIC for Silicon-strip Detectors of J-PARC Muon g-2/EDM Experiment

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We report on the development of a front-end ASIC for silicon-strip detectors of the J-PARC Muon g-2/EDM experiment. This experiment aims to measure the muon anomalous magnetic moment and electric dipole moment precisely to exploit new physics beyond the Standard Model. The readout ASIC is required to tolerate a high hit rate of 1.4 MHz per strip and to have deep memory for the period of 40 us with 5 ns time resolution. In order to satisfy the experimental requirements, a new prototype ASIC was designed with 180 nm CMOS. The design and performance of the ASIC will be discussed.

Summary

The muon anomalous magnetic moment (g-2) and the electric dipole moment (EDM) are sensitive to new physics beyond the Standard Model. A precise measurement is currently in preparation at the Japan Proton Accelerator Research Complex (J-PARC) with completely different techniques from the past measurements, used at BNL and Fermilab. Muons are stored by the 3-T solenoid magnet, following the orbital cyclotron motion with a diameter of 0.66 m. To detect circular position tracks from the muon decay, fast response silicon strip (single-sided p-on-n type) detectors with high granularity are placed radially in the storage magnet.
The front-end ASIC is required to tolerate a high hit-rate of 1.4 MHz per strip and to have stability during the change of hit-rate by a factor of 1/150. Since the basic functionarity has been demonstrated with a full scale chip in the previous study, we focused on analog performance improvement in this study. Experimental requirements to the updated ASIC are as follows: (1) the time-walk of less than 5 ns for an input signal range of 0.5—4 MIPs, (2) the equivalent noise level of ˜1800 e- with a detector capacitance of 30 pF, and (3) the layout constraint of ˜7 mm on a chip width, including 128 channels, i.e., y=˜50 um for one channel if we consider including the peripheral bias circuits, while a another chip width is not strictly constrained at this stage.
To achieve all specifications, a prototype front-end was designed with Silterra 180 nm CMOS technology. In addition to the conventional second-order CR-RC shaper, we have newly implemented a differential circuit after the CR-RC shaper. By using the timing of the differential's zero-cross and trailing edge of the CR-RC shaper, we succeeded to meet the time-walk specification with 4.8 ns for required input range in the measurement. The ENC is also estimated as 1789 e- with the input capacitance of 30 pF. These encouraging results drive us to submit a second full scale ASIC in the next submission. In this presentation, we discuss a detector concept of the experiment, ASIC design details, and the measurement results.

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