Contribution ID: **160** Type: **Poster**

A Capacitor DAC for Charge Redistribution Analog to Digital Converter with Successive Approximation

Tuesday 18 September 2018 18:35 (15 minutes)

Recent analog to digital converters with the successive approximation (SAR ADC) are popular for high speed, low power operation, and accuracy. SAR ADC demands a precise internal digital to analog converter (DAC) which is mostly made using capacitors. This article presents two new approaches how to design the capacitor DAC in 180 nm SOI technology. The first is 10-bit split DAC and the second is 8-bit binary-scaled DAC. Layout styles for each of capacitor DAC are shown. Simulations confirm that both of capacitor array have nonlinearities under the magnitude of the least significant bit without a calibration scheme.

Summary

The performance of the SAR ADC depends among others on the quality of a capacitive DAC (CDAC). In some designs are CDAC nonlinearities alleviated using a calibration scheme. However, calibration schemes significantly increase a circuit complexity and deteriorate speed. To guarantee acceptable linearity of capacitive DAC it is important to properly size the unit capacitor and keep a proper layout style. The split capacitor allows low power operation and small layout area. However, it suffers from low SAR ADC speed because of the large unit capacitor in order to suppress sufficiently parasitic capacitances. Generally, a Metal Insulator Metal (MIM) capacitors are used for the split capacitor DAC. The binary scaled capacitor array allows low unit capacitance and high speed. However, it needs larger layout area. The binary scaled CDAC can be implemented using Metal oxide Metal (MoM) capacitor which allows a higher speed of entire converter. This MoM capacitor can be customized as a box to alleviate parasitic capacitances. A box structure acting as a shield against to parasitic capacitances.

In existing literature, a lot of articles are dedicated to SAR ADC. However, a paper dedicated to CDAC is hard to find. This paper provides two new layout styles as a guideline how to design CDAC for SAR ADC taking considering size and types of capacitors, power consumption, layout area, speed, and nonlinearities.

In this paper, we propose a 10-bit split capacitor CDAC with MIM capacitors and an 8-bit binary scaled CDAC with customized MoM capacitor. The unit MIM capacitor size is 10x10 um with capacitance 106 fF. Overall capacitance of the split CDAC is 6.678 pF, size 57.5x236 um. The unit MoM capacitor has size 4.24x4.24 um and capacitance 4.5 fF. Overall capacitance the 8-bit binary scaled CDAC is 1.174 pF, size 57.5x196 um. By comparing total capacitances is apparent that the binary scaled CDAC can reach higher speed and better power consumption. The speed of SAR ADC with the binary scaled CDAC can reach up to 10 million samples per second. While the speed of SAR ADC with the proposed split CDAC is only 250 thousand sample per second. Layout styles are shown. Post-layout simulations proved that INL and DNL kept under the magnitude of the least significant bit. Both proposed CDAC designs were simulated in a 180 nm SOI technology are used in real SAR ADC for radiation imaging detector.

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Session Classification: Posters

Track Classification: ASIC