A 130 nm CMOS PLL for Phase-II ATLAS MDT-TDC

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ABSTRACT

The high luminosity and interaction rate expected from the planned High Luminosity-Large Hadron Collider (HL-LHC) upgrade require a replacement and improvement of the ATLAS Muon-Drift-Tube (MDT) read-out electronics. This paper presents a Phase Locked Loop (PLL) intended to be used inside the improved Time-to-Digital Converter (TDC), which digitizes the arrival time and charge amplitude information. Starting from a 40 MHz input clock, the PLL provides output clocks of 160 MHz and 320 MHz with a phase resolution of 11.25° and 22.5° respectively. The prototype, integrated in 130 nm CMOS technology, has 0.02 mm² of area and 1.2 V of supply voltage.

Global Project: Development of a TDC for ATLAS MDT Phase-II Upgrade

Features:
- Trigger-less and trigger mode
- Edge and pair modes
- Programmable output lines rates: 80 (legacy), 320, 640 Mbps
- Re-design in TSMC 130nm technology
  - Clock and phase generator (ePLL)
    - 4 clock phase time interpolator @320MHz → 3.125 ns/4 = 0.78ns LSB
    - TDC time-digitization unit (x24) and digital processing logics

PRELIMINARY MEASUREMENTS

ePLL FEATURES
- Input clock frequency of 40 MHz
- One copy of output clock @ 160 MHz
- Two copies of output clock @ 320 MHz
- Programmable output phases with
  - 11.25° of resolution for 160 MHz
  - 22.5° of resolution for 320 MHz
  - equivalent step delay = 195 ps
- Programmable loop filter bandwidth and charge pump current
  - PLL and PVT compensation

ePLL Layout

ePLL Test Board

ePLL160MHz output

ePLL320MHzA output

ePLL320MHzB output

ePLL160MHz delays vs bit

ePLL320MHzA delays vs bit

ePLL320MHzB delays vs bit

Trigger and readout scheme for the Phase-II MDT system

TDC block diagram

ePLL block diagram

ePLL block diagram

Leading
Trailing
CH ID
(1 b)
(5 b)
Chnls
(2 b)
(15 b)

12 Chnls

Leading
Trailing

CH ID

(5 b)

Leading
Trailing

CH ID

(1 b)

Leading
Trailing

CH ID

(5 b)

Leading
Trailing

CH ID

(1 b)