Contribution ID: **147** Type: **Poster**

A 130 nm CMOS PLL for Phase-II ATLAS-MDT TDC

Tuesday 18 September 2018 18:35 (15 minutes)

The high luminosity and interaction rate expected from the planned High Luminosity-Large Hadron Collider (HL-LHC) upgrade require a replacement and improvement of the ATLAS Muon-Drift-Tube (MDT) read-out electronics. This paper presents a Phase Locked Loop (PLL) intended to be used inside the improved Time-to-Digital Converter (TDC), which digitizes the arrival time and charge amplitude information. Starting from a 40 MHz input clock, the PLL provides output clocks of 160 MHz and 320 MHz with a phase resolution of 11.25° and 22.5°, respectively. The prototype, integrated in 130 nm CMOS technology, has 0.02mm2 of area and 1.2V of supply voltage.

Summary

The high event rate and large amount of data expected from the Phase II Upgrade of High-Luminosity LHC (HL-LHC) imposes challenging requirements for the detectors and the read-out electronics of ATLAS Muon-Drift-Tube (MDT) chambers. Moreover, ATLAS plans to use the MDT detector at the first-trigger level to improve the muon transverse momentum resolution and reduce the trigger rate. The new MDT trigger and readout system will have an output event rate of 1 MHz and a latency of 6 μs at the first-level trigger. Therefore, the read-out electronics must be improved in order to satisfy the new challenging requirements.

The electronic front-end performs amplification, shaping and discrimination through the ASD (Amplification-Shaper-Discriminator) blocks; then the ASD output binary differential signals are provided to a Time-to-Digital Converter (TDC), where the arrival times of leading and trailing edges are digitized in a time bin of 0.78 ns which leads to an RMS timing error of 0.25 ns. The pulse height is encoded as the time interval between the leading and trailing edges of the ASD output pulse.

The Phase Locked Loop (PLL) presented here has been designed for the fine time measurements part of the TDC. The hit signals coming from the ASD blocks are used to store the fine and coarse time measurements in channel buffers. The fine measurement should be obtained from taps along a chain of delay elements; for this purpose a self-calibrating loop as the here presented PLL is preferred, in order to have more stable and robust delay elements and a high resolution. In particular, the proposed PLL has been designed in 130nm CMOS technology, with 1.2V of supply voltage and a core area of 0.02mm2. It accepts a 40 MHz input clock and provides 160 MHz and 320 MHz output clocks, which can be programmed with a resolution of 11.25° and 22.5° respectively. In order to compensate temperature and process variations, the resistance and the capacitance of the loop filter can be tuned with 4-bits and 2-bits words respectively. Also the charge pump output current can be programmed with 4-bits current-output DAC, in order to adjust the PLL operation.

Post-layout simulations validate the design, with a total power consumption of 12mW. A first PLL prototype has been integrated in order to verify through specific measurements the PLL operation and to include this design in the next upgraded TDC version.

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Session Classification: Posters

Track Classification: ASIC