This paper presents a Fast-Tracker front-end (FTfe) for ATLAS small-diameter Muon Drift Tube (sMDT) detectors of the Phase-II Upgrade HL-LHC. This design addresses the higher rate capability required by sMDT and reduces the dead-time below the maximum drift time, further increasing the efficiency. The front-end ensures a fast baseline restoration with a reset interval of maximum 160 ns, so that the secondary spurious pulses are avoided and the successive muon signals can be detected soon and correctly. The device has been designed in 1V-28nm-CMOS technology; outstanding 4.7mV/fC sensitivity and 0.24fC ENC are achieved with a core area of 0.03mm^2.

**Abstract**

This paper presents a Fast-Tracker front-end (FTfe) for ATLAS small-diameter Muon Drift Tube (sMDT) detectors of the Phase-II Upgrade HL-LHC. This design addresses the higher rate capability required by sMDT and reduces the dead-time below the maximum drift time, further increasing the efficiency. The front-end ensures a fast baseline restoration with a reset interval of maximum 160 ns, so that the secondary spurious pulses are avoided and the successive muon signals can be detected soon and correctly. The device has been designed in 1V-28nm-CMOS technology; outstanding 4.7mV/fC sensitivity and 0.24fC ENC are achieved with a core area of 0.03mm^2.

**Issues & Requirements**

- **Phase-II Upgrade HL-LHC**
  - Higher luminosity and interaction rate
  - Higher speed and resolution requirements for the front-end
- **Improved sMDT detectors**
  - >15 mm instead of 30 mm diameter drift tubes
  - >10 times higher rate capability in terms of spatial resolution and muon efficiency
  - 4 times shorter maximum drift time (180 ns instead of 500 ns)
  - Small dead-times
  - Increased pile-up effect of muon signals on top of the bipolar undershoots of preceding background pulses
- **Current read-out front-end for muon detection**
  - Amplifier-Shaper-Discriminator (ASD) chain
  - Charge arrival time and ToT extracted through a discriminator stage
  - Charge amplitude information recovered through a proper Charge ADC
  - Secondary spurious pulses (SSPs) cause multiple threshold crossings for each muon track and too much data to be stored
  - Bipolar shaping & long dead-times required

**FTfe Characteristics**

- **Integrated in 28nm-bulk-CMOS technology**
  - One of the first devices for this application in this node
  - Higher performance can be achieved
  - Intrinsic radiation hardness
- **Detection only for the primary hit**
  - Arrival time information through a first threshold crossing
  - Charge amplitude information as time difference using a second threshold crossing
- **Front-end reset** after charge measurements and blind to other incoming hits for minimum required time interval (max 160 ns instead of 500 ns)
  - SSPs not processed by the front-end and no pile-up
- **Programmable capacitors** used both in CSP and Shaper to control the FTfe performance vs technology PVT (Process-Voltage-Temperature) variations

**FTfe Specifications**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input charge Q(s)</td>
<td>5-100 fC</td>
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<tr>
<td>Detector capacitance</td>
<td>10 pF</td>
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<tr>
<td>Peaking time delay</td>
<td>28 ns</td>
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<tr>
<td>Sensitivity</td>
<td>&gt;4 mV/fC</td>
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<tr>
<td>ENC</td>
<td>&lt;0.5 fC</td>
</tr>
</tbody>
</table>

**Performance**

- **CMOS Technology**
  - 28 nm
- **Supply Voltage**
  - 1 V
- **Area**
  - 0.03 mm^2
- **Power consumption**
  - 2.6 mW
- **Input charge**
  - 5-100 fC
- **Sensitivity**
  - 4.7 mV/fC
- **ENC**
  - 0.24 fC
- **SNR**
  - 23.3 dB

**FTfe layout**

CSP, Shaper, Comparators and Reset signals at 5fC and 100fC input charge

**CSP and Shaper output signals for different input charges**

**Post-layout result with more pulses**

**Preliminary measurement**

Simplified comparison between classical read-out behavior without reset (left) and the proposed FTfe behavior (right)