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An UVM-based verification environment for the lpGBT 10 Gbps transceiver ASIC

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The lpGBT is a 10 Gbps transceiver ASIC meant to be used in High Luminosity LHC detectors. It provides a variety of communication interfaces, including multi-mode high-speed serial interfaces, I2C, and parallel IO. The Universal Verification Methodology had been selected to verify chips design and implementation. This paper discusses the strategies used to verify all the chip functionalities, including not standard serial interfaces. Moreover, structures of the developed UVM test benches together with performance metrics are presented.

Summary

Future detectors for experiments on the High Luminosity LHC will produce an unprecedented amount of data. The lpGBT chip is currently under development to support a common interface for data and clock transmission. In order to serve a multitude of applications, the ASIC can operate in several modes (Simplex Receiver/Transmitter, Transceiver) at various data rates (5 or 10 Gbps). It offers two FEC encoding schemes which will enable the end users to optimize their system with respect to the data bandwidth and immunity to Single Event Effects. Moreover, it will also provide slow control features (like I2C master/slave interfaces, parallel IO, ADC, DAC) which were previously part of dedicated ASICs. Given the nature of the chip, its many interfaces and high level of configurability, the Universal Verification Methodology (UVM) was selected to streamline the verification process of all its features. It allowed to ease the verification of standard interfaces, such as I2C, for which commercially available verification IP could be used. However, given that the lpGBT high-speed interfaces are data and protocol agnostic, with no clear transaction model, some concepts of the UVM methodology had to be adapted. Moreover, given the complexity of clock and data recovery circuits, as well as the complex and multi-stage initialization sequence, the simulation time was very long, which also presented an additional challenge. In the paper, an overview of the chip functionality is presented, together with the motivation for the use of the UVM methodology, and a description of how it was adapted to our non-standard test ecosystem. The way how the chip functionalities were clustered among the different tests, and how they are related to the structure and components of our UVM environment, is also detailed in the paper.

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