A high speed transmitter circuit for the ATLAS/CMS HL-LHC pixel readout chip

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Introduction

The substantially increased instantaneous luminosity after the phase-2 upgrade of LHC (High-Luminosity LHC), together with a higher trigger rate (1 - 4 MHz), calls for a much higher output bandwidth for the pixel front-end chip. Therefore, a high speed transmitter circuit, running at the nominal speed of 1.28 Gbps, was designed and integrated into the RD53A demonstrator chip[1] for the ATLAS/CMS HL-LHC pixel detector, which has been fabricated in a 65 nm CMOS technology. Combing four output data lanes, each RD53A chip offers the maximum output data rate of 5.12 Gbps. This work presents the design and preliminary test results of the RD53A transmitter circuit.

Architecture

- A clock and data recovery (CDR) circuit recovers clock from the 160 Mbps chip input command, and provides an 1.28 GHz clock to the output data link.
- The 20-bit data words from the on chip data encoding logic are serialized, and sent off chip by the cable driver.
- The output driver can compensate the high frequency propagation loss of low mass cable with pre-emphasis.
- Max. output bandwidth is 4 × 1.28 Gbps

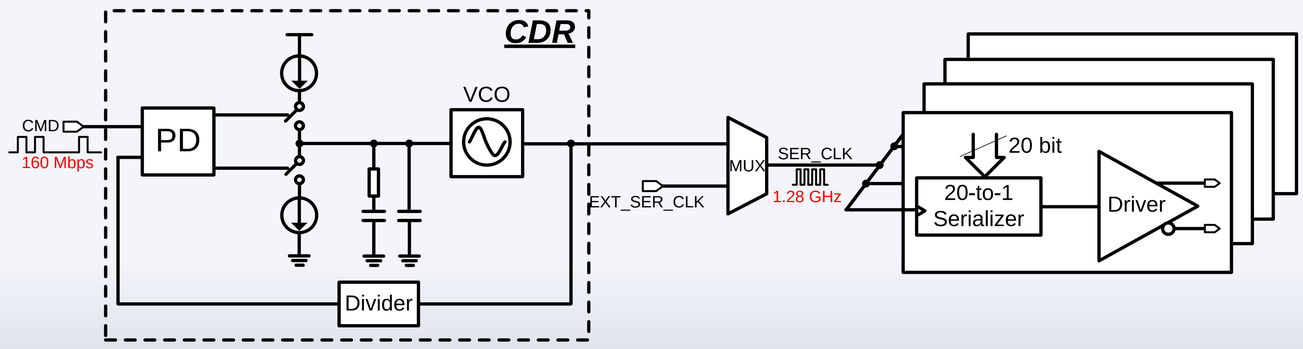

Fig. 1 Block diagram of the full data link

Circuit design

- *Serializer*
  - 20-to-1 double data rate structure

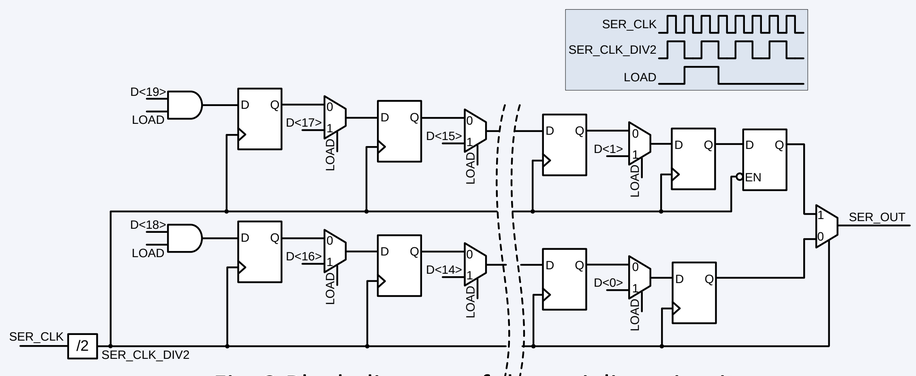

Fig. 2 Block diagram of the serializer circuit

- *Cable driver*
  - 3-tap current mode logic (CML) driver
  - Current for each tap adjusted independently by 10-bit DACs
  - The polarity and activation of tap 1&2 can be configured

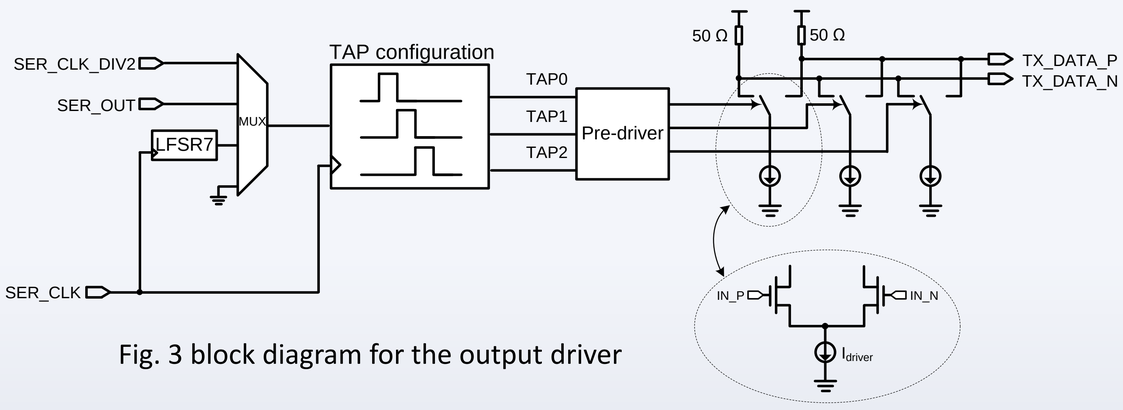

Fig. 3 block diagram for the output driver

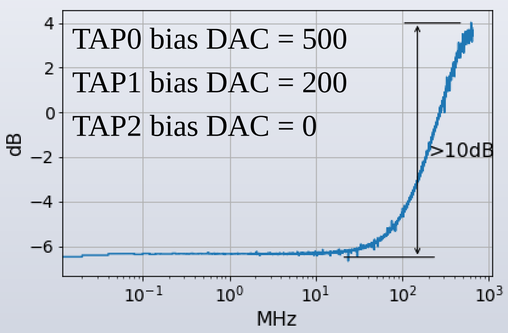

Fig. 4 Frequency response of the pre-emphasis filter

- The frequency response of the pre-emphasis filter is calculated with circuit simulation data
- 10 dB emphasis at half symbol rate (640 MHz) with two-tap configuration

Preliminary test results

- Chip tested with BDAQ53 data acquisition system[2]

Fig. 5 BDAQ53 board (left) and single chip card (right)

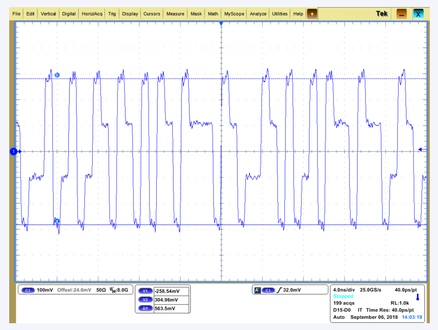

Fig. 6 Differential output with pre-emphasis on

- Eye diagram measured with LFSR7 data pattern @ 1.28 Gbps
  - Pre-emphasis off, TAP0 bias DAC = 500
  - Low jitter (<2ps) ext. clock vs. clock recovered by CDR circuit

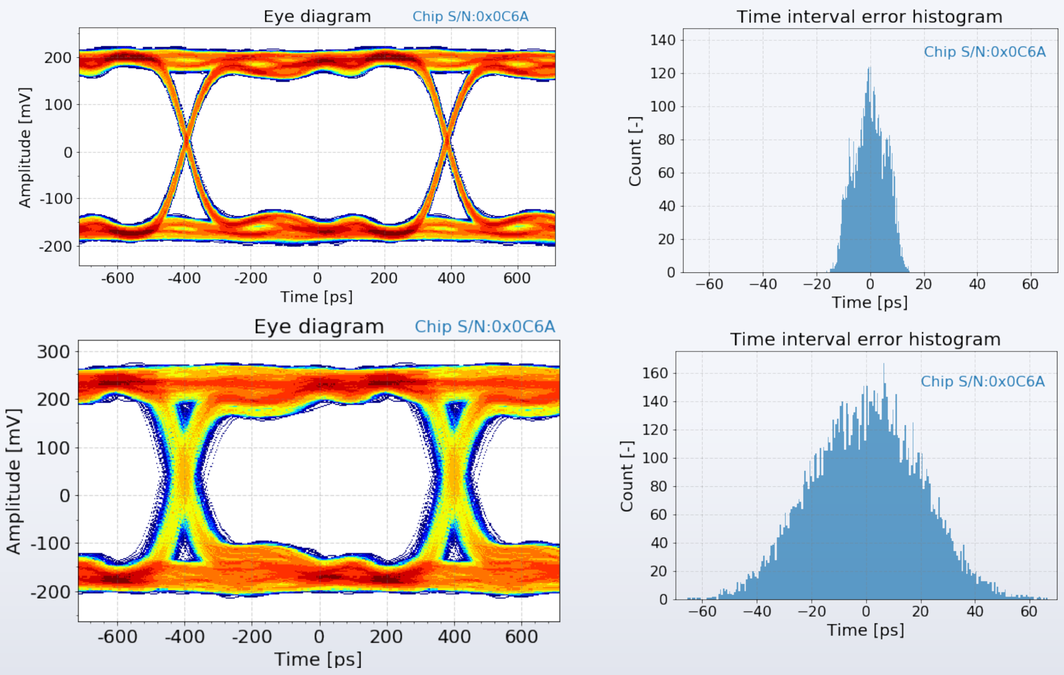

Fig. 7 Eye diagram with ext. clock (upper) and clock from CDR (lower)

	TIE (rms)	Eye height	Eye width
Ext. clock	5.8 ps	305 mV	738 ps
CDR clock	19.9 ps	301 mV	557 ps

Summary

- Full functionality of the RD53A high speed transmitter circuit has been tested.
- The output jitter is ~ 20 ps. A prototype with improved CDR design has been submitted, in order to reduce the clock jitter.
- Chip sample irradiated by X-ray up to 500 Mrad will be measured.

Acknowledgement

This work was done within the RD53 collaboration

Reference

1. RD53 Collaboration, The RD53A Integrated Circuit, CERN-RD53-PUB-17-001 (2017).
2. M. Vogt, et al., PoS (TWEPP-17) 084

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