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Design and characterization of a high speed transmitter circuit for the ATLAS/CMS HL-LHC pixel readout chip

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In order to satisfy the high output bandwidth requirement imposed by the HL-LHC, a high speed transmitter circuit was designed and integrated into the RD53A demonstrator chip for the HL-LHC pixel detector. A CDR/PLL circuit recovers clock from the 160 Mbps incoming data, and provides high speed clock to the serializer, where the 1.28 Gbps output stream is formed. The output stage employs a three-tap current-mode logic driver with adjustable tap coefficient for optimal pre-emphasis. Each RD53A chip includes four output lanes, offering in total 5.12 Gbps output bandwidth. The circuit topology as well as measurement results will be presented.

Summary

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